ApproSync: Approximate State Synchronization for Programmable Networks

Paper#241, 16 pages

ABSTRACT

Programmable switches empower stateful packet processing, in which incoming packets continuously update states in the data plane, while applications in the control plane read and/or write states. However, as the data plane and control plane are separated, a consistent view of states in both planes is required for stateful packet processing. Existing approaches suffer from either high latency or low accuracy. In this paper, we propose ApproSync, a framework that offers *approximate* state synchronization with low latency and high accuracy. To achieve low latency, ApproSync directly transfers states between switch ASICs and the control plane without involving switch operating systems. To achieve high accuracy, ApproSync fully utilizes the resources in the switch ASIC to realize rate control in state synchronization, such that it avoids potential state loss. It also bounds the divergence between the states in the data plane and that in the control plane into a negligible level. Thereby, it achieves maximum possible accuracy under limited link capacity. In particular, ApproSync employs two different approximate synchronization strategies for two types of operations, i.e., state read and state write. We prototype ApproSync on a Barefoot Tofino switch. The experimental results indicate that compared to existing approaches, ApproSync achieves order-of-magnitude latency reduction while maintaining high accuracy.

1 INTRODUCTION

Recent advances in programmable networks empower network administrators to customize the packet processing logic of network devices. For example, with the P4 language [20], administrators are able to define new network protocols and specify packet processing behaviors of programmable switches. Programmable switches often expose a collection of stateful memory (e.g., registers), which can be leveraged to store the *state* of packet processing. State is a set of historical packet processing values (e.g., packet counts) that influence future processing decisions. By manipulating state values, administrators can build *stateful* network management applications, such as real-time traffic monitoring [51, 52] and network function redundancy [30, 32, 67].

However, the separation of the data plane and control plane raises the problem of state synchronization. On the one hand, data plane packets continuously update the state maintained by each switch at line rate. On the other hand, applications manipulate states via the control plane. Thus, it is indispensable to keep a consistent view of states in both planes. In particular, given the huge volume and high speed of state updates, it requires to synchronize states within ultra-low latency to meet the requirements raised by latency-sensitive applications. For example, UDP flood mitigation [27] needs to collect thousands of state values from switches within a few microseconds so as to rapidly detect attacks. Also, state synchronization should be as accurate as possible so that applications can work on correct information.

Unfortunately, it remains a void to *efficiently* and *accurately* realize state synchronization in programmable networks. Today, state synchronization is achieved via an operating system (switch OS) installed atop every switch. The switch OS manipulates state values in its underlying switch ASIC via PCIe channels, and connects to the control plane via TCP-based protocols [1, 4, 11, 54]. Both PCIe channels and TCP connections could be the bottleneck to keep pace with state updates incurred by high-speed traffic [56, 61]. Our experiments indicate that the OS-based approach even spends several seconds to transfer a state with a normal size of 2^{16} values, which is slow and unacceptable (see §2.2). Some approaches [58, 61, 73] bypass the switch OS via traffic mirroring, which directly transfers state updates between the switch ASIC and the control plane, to achieve low latency. However, traffic mirroring fails to achieve high reliability like rate control and loss recovery. Thus, it suffers from serious state loss when traffic rate exceeds link capacity.

In this paper, we propose ApproSync, a low-latency and accurate state synchronization framework. To achieve low latency, ApproSync bypasses the switch OS to eliminate the performance overhead. However, it is challenging to entirely handle state loss in the switch ASIC due to switch resource restrictions. In response, ApproSync incorporates approximate strategies to achieve high accuracy. The notion behind is that many applications tolerate a small divergence between the state in the data plane and that in the control plane, i.e., *state divergence*. Thus, ApproSync allows a *small* state divergence and *eventually* makes the states in both planes consistent. Such design significantly alleviates resource requirements, making ApproSync readily deployable in switch ASICs.

Specifically, ApproSync adopts two approximate strategies to support two types of state operations, *state read* and *state write*, respectively. For state read, ApproSync monitors the

state divergence in the switch ASIC and synchronizes state updates only when the state divergence exceeds a threshold. In particular, ApproSync adaptively tunes the threshold based on incoming traffic rate: (1) When incoming traffic rate is low, it pushes every state update to the control plane, making synchronization error-free; (2) When incoming traffic rate is high and massive state updates need to be synchronized in a short time, it *selectively* pushes state updates to bound the state divergence into a negligible level. Thus, it achieves the maximum possible accuracy under link capacity. For state write, ApproSync retries all failed operations to eliminate state loss. It ensures the atomicity of state write by preventing all the new state updates in the data plane from updating the state during state write. To do this, it recirculates the new state updates, and eventually performs them when state write ends. Here, the recirculation drops accuracy because of making a few state updates out-of-order. However, the accuracy drop is small and acceptable for most applications.

In summary, we make the following contributions.

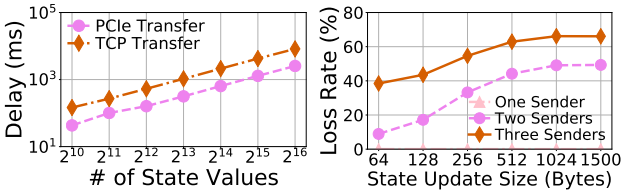
- We investigate the limitations of existing approaches, and study their implications on application-level accuracy.
- We design ApproSync based on approximate techniques to offer low-latency and accurate state synchronization.
- We implement a prototype of ApproSync with Barefoot Tofino switches [2] and commodity servers. We extensively evaluate ApproSync with 16 stateful P4 applications. The experimental results indicate that ApproSync achieves order-of-magnitude latency reduction against existing approaches and maintains high accuracy.

2 MOTIVATION

2.1 Problem

This paper targets state synchronization for programmable networks (e.g., data center networks [29, 51, 68]), where the data plane and control plane are separated. In the data plane, each programmable switch maintains a collection of values referred as *state* and continuously updates its state during packet processing. The control plane holds a copy of the state of each switch. Applications make decisions based on states and perform control actions by modifying the states in the data plane. For instance, stateful firewall [31] requires to efficiently collect state values from switches to rapidly detect attacks. Also, it dynamically updates the detection threshold recorded in switches to adjust to traffic dynamics.

Such distributed processing motivates a state synchronization mechanism to keep a consistent view of states in both planes. In the bottom-up direction, state updates incurred by data plane packets must be synchronized to the control plane. In the top-down direction, state modifications in the control plane should also be reflected in the data plane. In particular,



(a) High latency of OS-based approach. **(b) State loss rate of traffic mirroring.**

Figure 1: Benchmark of existing state transfers.

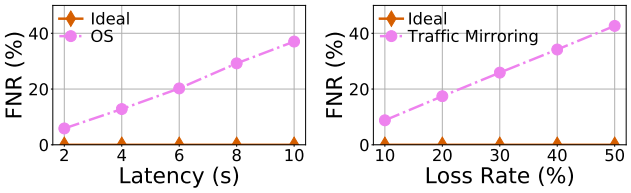
applications require state synchronization to achieve both *low latency* and *high accuracy*.

- **Low latency**. We aim to minimize the latency of state synchronization in both directions (i.e., from data plane to control plane and vice versa). This is critical to keep pace with high-speed network traffic and meet the tight latency requirements raised by applications. For example, network anomaly detection requires to rapidly detect and react to suspect events [23, 40, 42, 66].
- **High accuracy**. We aim to minimize the state divergence between the data plane and control plane, which guarantees the correctness of application operations. For instance, the attack detector may raise a false alarm if received states are highly noisy. Moreover, if a state modification is not properly synchronized to the data plane, switch behaviors may be wild (e.g., a firewall policy fails).

2.2 Limitations of Existing Approaches

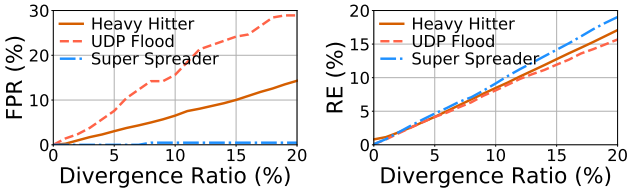
Existing approaches synchronize states via either the switch OS or traffic mirroring. However, none of these approaches can achieve both low latency and high accuracy.

High latency in OS-based approach. The OS-based approach utilizes the switch OS to transfer the state between the switch ASIC and the control plane. For the switch ASIC, the OS manipulates the state via PCIe channels. For the control plane, the OS establishes TCP connections [1, 4, 11, 54] to transfer the state. However, this approach incurs high latency in two aspects. First, due to limited bandwidth, PCIe channels could be the performance bottleneck [61]. Second, TCP connections incur high latency in TCP stacks and reliable transmission. Figure 1(a) measures the two types of latency when synchronizing up to 2^{16} 64-bit state values in a Barefoot Tofino switch [2]. We observe that both PCIe transfer and TCP-based transfer incur a latency of hundreds of milliseconds, e.g., synchronizing 2^{16} state values takes even several seconds. Such high latency compromises many applications that require sub-second state collection (e.g., network measurement [25, 40, 63], attack mitigation [41, 45, 76], and data center network management [44, 59, 77]).



(a) High latency. (b) High loss rate.

Figure 2: Impact on applications.



(a) False positive rate. (b) Relative error.

Figure 3: Impact of small state divergence.

State loss in traffic mirroring. To achieve low latency, the approaches based on traffic mirroring directly mirror state updates from the switch ASIC to the control plane via a few mirroring ports [61, 73, 75, 86]. However, these approaches suffer from serious state loss when the emitted rate of state updates exceeds link capacity [61]. In Figure 1(b), we measure the loss rate in a Tofino switch. We allocate one 40-Gbps mirroring port and vary the number of traffic ports. We inject traffic to each traffic port to reach 40 Gbps. We see that with only one traffic port, there is almost no state loss. However, the loss rate rapidly rises as the number of traffic ports increases. It reaches 60% when using three traffic ports. With such a high loss rate, most state values cannot be synchronized so that the state divergence is extremely high. As a result, applications work on inaccurate states and fail to perform correct operations. Although allocating more mirroring ports can alleviate state loss, doing so unavoidably sacrifices overall switch throughput and affects normal processing.

Impact on applications. We study the impact of existing approaches by considering an example of heavy hitter detection [57]. We define a heavy hitter as a 2-tuple flow whose number of packets exceeds 1K, and set the time interval of collecting flow records to 1s. First, we study the impact of the OS-based approach, which spends several seconds to pull states from switch ASICs. Figure 2(a) shows that false negative rate (FNR) significantly increases as the latency spent by the OS-based approach increases. Second, we evaluate the impact of traffic mirroring, which suffers from high loss rate. In Figure 2(b), false negative rate rapidly increases as the loss rate increases. To summarize, due to high latency or serious state loss, existing approaches significantly drop application-level accuracy.

3 APPROSYNC DESIGN

We design ApproSync to provide timely and accurate state synchronization. For low latency, ApproSync realizes synchronization entirely in the switch ASIC to bypass the switch OS. For high accuracy, ApproSync utilizes the resources of switch ASICs to avoid state loss.

Challenge. There have been many solutions in the literature that can be used to handle state loss during state synchronization, e.g., timeout and retransmission mechanisms [14, 64]. Unfortunately, it is infeasible to realize these solutions in switch ASICs due to switch restrictions. Specifically, existing programmable switches typically employ specific architectures (e.g., PISA [21]) to achieve high throughput and ultra-low latency. Such architectures impose several restrictions on their resource models due to the concern of chip footprints and heat consumptions. Here, we summarize three types of restrictions [21, 69]: (1) each switch is equipped with few memory (at most 10 MB [21, 55]); (2) a switch allows limited memory access (e.g., a few read-write operations for each packet); (3) a switch does not support complex operations (e.g., loop and buffering). Given these restrictions, it is challenging to entirely avoid state loss in switch ASICs.

Observation. Although large errors seriously degrade application accuracy as shown in §2.2, we observe that it is acceptable for many applications to maintain a small and bounded state divergence. In fact, many applications are already built on approximate algorithms such as sampling [10, 26, 34, 61, 65, 84] and sketches [38, 40, 52, 82]. Thus, a small divergence is tolerable for these applications in practice. To justify this, we evaluate the impact of state divergence on the accuracy of three applications, heavy hitter detection [57], UDP flood mitigation [27], and super-spreader detection [57]. We vary the relative divergence from 0% to 20%. Figure 3 shows that the application-level error is negligible when the divergence is small, which validates our observation. Note that different from the benchmarks shown in Figure 2, where we measure high state divergence (10%∼50%), Figure 3 addresses application accuracy under small divergence (<5%).

Key idea. According to our observation, we design ApproSync with *approximate state synchronization* that exploits approximate techniques to achieve high accuracy and low resource consumption. ApproSync allows a small state divergence but bounds the state divergence into a negligible level with respect to switch restrictions. Such approximate synchronization brings two-fold benefits. First, it greatly relaxes the

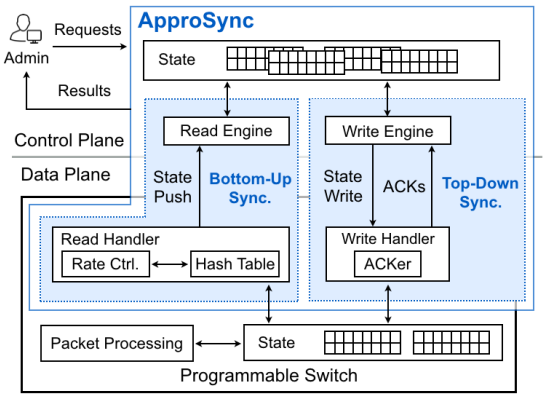


Figure 4: Overview of ApproSync framework.

resource requirement, which mitigates the aforementioned challenge and makes ApproSync readily deployable. Second, the approximate design imposes an upper bound on the state divergence, in which applications still remain high accuracy.

Note that approximate techniques have been widely adopted in distributed systems (see §7 for details). Although ApproSync follows similar ideas, it carefully identifies the specific challenges of adopting approximation in state synchronization for programmable networks. Also, it offers customized solutions to address the identified challenges rather than simply bundling existing techniques.

Architecture. As shown in Figure 4, ApproSync synchronizes state in two directions, i.e., from the data plane to control plane and vice versa, which correspond to two types of operations, *state read* and *state write*, respectively. It offers two strategies, *bottom-up synchronization* for state read, and *top-down synchronization* for state write. Each strategy is realized by a handler in the switch ASIC and an engine in the control plane, which collectively synchronize states.

- **Bottom-up synchronization (§3.1)**. This strategy makes read operations keep pace with the state updates incurred by data plane packets. The read handler in the switch ASIC monitors every state update and *selectively* pushes state updates to the read engine, which extracts state values from received updates in the control plane. To mitigate state loss, the read handler offers a hash table that aggregates state updates for each memory location and monitors the state divergence. Once the state divergence exceeds a threshold, it emits aggregated updates to make the state in both planes consistent. It adaptively tunes the threshold to keep the emitted rate of state updates smaller than link capacity rather than direct mirroring. Such rate control (1) offers error-free state read when incoming traffic rate is low, and (2) bounds the state divergence even with high incoming traffic rate. Further, the state divergence will be provisioned such that users can examine the quality of states.
- **Top-down synchronization (§3.2):** This strategy writes the state modifications raised by applications to programmable switches. The write engine exploits an acknowledgement mechanism to eliminate state loss since write operations are not invoked so frequently. Also, ApproSync enables atomicity of state write. Specifically, the write handler suspends the state updates incurred by data plane packets: it recirculates new state updates for a second-pass processing. These updates are eventually performed after state write. This makes some state updates out-of-order. However, this strategy incurs no data loss while greatly improving the overall resource efficiency.

Algorithm 1 Read handler.

Input: state update (l, v)
Variables: hash table H, threshold t

```
1:  function Process_Update(l, v)
2:      Position p = hash(l)
3:      if H[p] is empty then ▷ Assume initial state value as zero
4:          H[p].loc = l, H[p].val = v, H[p].old = 0   ▷ Insert H[p]
5:      else if H[p].loc == l then
6:          Update H[p].val = v
7:          Divergence D = |v − H[p].old|
8:          if D ≥ t then
9:              Push (H[p], t) to the control plane
10:             Update H[p].old = v
11:         end if
12:     else                                          ▷ H[p].loc ≠ l
13:         Push (H[p], t) to the control plane
14:         H[p].loc = l, H[p].val = v, H[p].old = 0
15:     end if
16: end function
```

3.1 Bottom-Up Synchronization for State Read

For bottom-up state read, ApproSync realizes a hash table in the switch ASIC to process state updates. The hash table monitors the state divergence and selectively pushes state updates when the state divergence exceeds a threshold. Moreover, ApproSync provides a rate controller in the switch OS. The rate controller adaptively tunes the threshold with respect to incoming traffic rate. In doing so it bounds the state divergence and achieves the maximum possible accuracy under link capacity. It also enables applications to utilize the state divergence on demand. Moreover, ApproSync monitors the time that each entry resides in the hash table, and pushes expired entries to the control plane to reduce accuracy drop.

Data structure. The read handler maintains a hash table H to monitor the state divergence. H uses counter indexes in the state as keys. Every entry $H[p]$ has three fields: (1)

$H[p].loc$ is the state location (i.e., hash key) associated with this entry, (2) $H[p].val$ denotes the current state value in location $H[p].loc$, and (3) $H[p].old$ records the corresponding state value in the control plane. Since the switch memory is scarce, we restrict the size of H. Here, a size of 2^{16} entries is sufficient for most applications to retain high accuracy with a small portion of switch resources. Moreover, when hash collisions happen, H evicts the old entries to the control plane so as to make room for new keys. Here, one concern is that frequent hash collisions could exhaust link bandwidth. However, in real-world workloads, most traffic is contributed by a small portion of flows due to the skewness of network traffic [43]. Thus, most state updates are incurred by a few flows, making the probability of hash collisions small in practice. For instance, when using 2^{16} entries, the probability of hash collisions is below 5% for a one-hour CAIDA trace. This leads to a peak emitted rate of 0.92 Mpps, which is small and acceptable.

Algorithm. Algorithm 1 details how the read handler processes state updates. It is invoked with respect to every tuple (l, v), which indicates that the value in location l has been updated to v. The read handler first hashes l to calculate its position p in H (line 2). If $H[p]$ is empty (line 3), it directly inserts (l, v) (line 4). Otherwise, it compares l with existing stored location $H[p].loc$ (line 5). If the two positions are the same, the read handler updates the state value (line 6). Then it computes the divergence between current state value v and that in the control plane recorded by $H[p].old$ (line 7). If the divergence exceeds a pre-defined threshold t, both the entry $H[p]$ and t are emitted to the control plane (lines 8-9). Here, the value of t represents the maximum tolerable divergence between a state value recorded in the switch ASIC and that in the control plane. Moreover, $H[p].old$ is changed to reflect the updated control plane value (line 10). If the stored location is different from the new location (line 12), indicating a hash collision, the read handler pushes the existing entry and the threshold t to the control plane (line 13), and then modifies the entry to store the new one (line 14).

Example. Suppose that the threshold t is four and the hash table H has two buckets, and there are six state updates (Figure 5(a)). For the first two updates p_0 and p_1, H directly inserts them and initials $H[p].old$ to zero (Figure 5(b)). For p_2, H maps it to the first bucket, which already stores a state update with the same location of p_2. H calculates the divergence $D = 2 < t$. Thus, H does not send p_2 to the control plane (Figure 5(c)). H processes p_3 similarly to p_2. After processing p_3, $H[p].val$ of the first bucket is three (Figure 5(d)). When p_4 arrives, H calculates the divergence D, which now reaches the threshold t (Figure 5(e)). Thus, H sends p_4 and t to the control plane and updates $H[p].old$ with $H[p].val$ (Figure 5(f)). Finally, p_5 comes in, H hashes it to the second

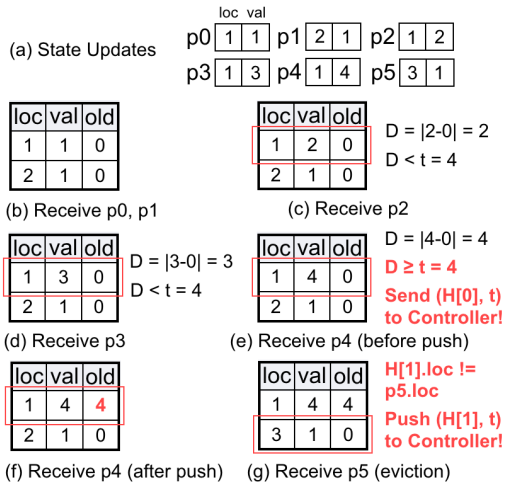


Figure 5: Example of hash table in the read handler.

bucket. It finds that the location of p_5 does not match the location stored in the bucket. Thus, H sends the old entry and t to the control plane and inserts p_5 (Figure 5(g)).

Rate control. The threshold t controls the trade-off between accuracy and bandwidth consumption. Our intuition is that we can employ a small threshold to minimize the state divergence as long as link capacity is not exhausted. With that in mind, we design a rate controller in the switch OS that adaptively tunes t instead of specifying a fixed one.

Specifically, the rate controller reads the total change Δ of all state values within a time window w. It employs a dedicated 64-bit counter in the switch ASIC to count the number of state updates. It reads the value change of the counter as the estimate of Δ. Such design is low-overhead, e.g., given a time window w = 1ms, the rate controller consumes 6.4×10^{-2} Mbps to read Δ, which is negligible compared to Gbps-level switch bandwidth. Moreover, w is determined by applications. For instance, the detection of low-rate TCP denial-of-service attacks [48, 51] needs to detect microbursts that happen in a few milliseconds, so a reasonable w is 1 ms. Given Δ and w, the emitted rate of state updates is then calculated as $\frac{\Delta}{w}$. Also, the maximum emitted rate $M = \frac{c}{s}$ supported by a link can be calculated based on link capacity c and the size s of each state update (l, v), which are known a priori. Note that $\frac{\Delta}{w}$ is a metric that reflects incoming traffic rate: when incoming traffic rate is low, Δ is small, making $\frac{\Delta}{w}$ small; otherwise, the reverse holds true.

Thereafter, the rate controller determines whether $\frac{\Delta}{w} \leqslant M$. If so, which indicates that link capacity is sufficient to support the emitted rate of state updates, the rate controller sets t to zero to send every state update to the control plane. Otherwise, the emitted rate will exceed link capacity so that the rate controller needs to set a non-zero t for the sake of avoiding link saturation. In this case, a state update is emitted

when a state value is changed by t. Thus, the emitted rate of state updates can be estimated as $\frac{\Delta}{wt}$. To avoid link saturation, the rate controller tunes t to keep the emitted rate $\frac{\Delta}{wt}$ just less than M, implying $t = \left\lceil \frac{\Delta}{wM} \right\rceil$. In practice, the rate controller sets a $t = \left\lceil \beta \frac{\Delta}{wM} \right\rceil$ for some $\beta \geq 1$ to handle unexpected traffic bursts. Our experience is that a small β closed to one is sufficient for most applications. We summarize how the rate controller sets t as follows.

$$t = \begin{cases} 0, \text{ if } \frac{\Delta}{w} \leqslant M \\ \left\lceil \beta \frac{\Delta}{wM} \right\rceil, \text{ otherwise.} \end{cases}$$

We further illustrate the rate control of ApproSync via an example. We assume that (1) ApproSync uses a 10-Gbps link to transfer 16-byte state updates so that link capacity $c = 10^{10}$ bps and the size of a state value $s = 128$ bits; (2) the time interval $w = 1$ ms; (3) no microbursts happen so a $\beta = 1$ is sufficient. Thus, M is calculated as $M = \frac{c}{s} = 7.8125 \times 10^7$ pps. Suppose that $\Delta = 10^4$ in the first time interval. Since $\frac{\Delta}{w} = 10^7 \leqslant M$, the read controller sets the threshold t to zero, such that every state update can be transfered to the control plane without exhausting link capacity. In the second time interval, Δ is changed to 10^5, making $\frac{\Delta}{w} > M$. In this case, the rate controller sets $t = \left\lceil \beta \frac{\Delta}{wM} \right\rceil = 2$. Thus, the maximum emitted rate of state updates is $\frac{\Delta}{wt} \approx 5 \times 10^7$ pps $< M$, which avoids link saturation and state loss.

Utilization of state divergence. As the threshold t dynamically changes, the read handler sends the current t with each state update to the control plane (Line 9 in Algorithm 1). Applications can utilize t to quantify the accuracy of the state. To illustrate, we use an example of Count-Min (CM) [24] sketch, which maintains several counter arrays to estimate flow sizes. In the data plane, a packet selects one counter in each array based on its flow ID, and then increments selected counters. Thus, every counter serves as an estimate for the packet count of the flow. When using ApproSync to collect counter values, the difference between the collected counter values and the latest counter values recorded in the data plane, i.e., the state divergence, unavoidably affects the accuracy of CM sketch. However, ApproSync guarantees that the state divergence will not exceed the threshold t. Thus, we can fix the lower bound and upper bound of error of CM sketch with the threshold t, as shown in Lemma 1.

Lemma 1. Consider a CM sketch with r rows and w counters in each row. Let T_f and E_f denote the true value and estimated value of a flow f, respectively. When deployed in ApproSync, the CM sketch guarantees that: (1) $E_f \geq T_f - t$, and (2) $E_f \leq T_f + \frac{2U}{w} - t$ with a probability at least $1 - \frac{1}{2^r}$, where U is the total value of all flows.

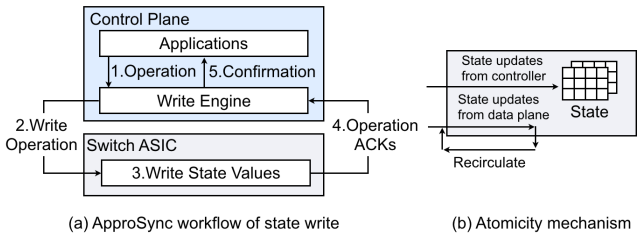


Figure 6: State write mechanism.

Proof. The original CM sketch guarantees that $T_f \leq E_f \leq T_f + \frac{2U}{w}$ with a probability larger than $1 - \frac{1}{2^r}$ (Theorem 1 in [24]). With ApproSync, the counter in the control plane is smaller than that in the data plane by at most t because the value has not been synchronized yet. Thus, the lower bound and upper bound of E_f become $T_f - t$ and $T_f + \frac{2U}{w} - t$, respectively. The results follow. □

Timeout monitor. As ApproSync records state updates in a hash table, one concern may be that some state updates can stay in the hash table for a long time when no evictions happen, which may affect accuracy. To this end, we design the hash table to timely detect expired entries. Specifically, when the time that an entry resides in the hash table exceeds a timeout value (e.g., a few seconds [78]) set by applications, the hash table raises a timeout signal to notify the switch OS. The switch OS then orders the hash table to immediately send the expired entry to the control plane. In this way, ApproSync alleviates the above concern. Note that we involve the switch OS because the logic of receiving timeout signals cannot be implemented in the switch ASIC due to switch restrictions. However, unlike the OS-based approach that brings high latency overhead, ApproSync adopts the switch OS to only receive and react to timeout signals rather than transfer state values. Doing so neither incur high bandwidth consumption nor affect the timeliness of state synchronization.

3.2 Top-Down Synchronization for State Write

For state write, ApproSync offers top-down synchronization driven by the control plane. The write engine acknowledges every write operation to mitigate state loss. For atomicity, it suspends the state updates incurred by data plane packets during state write, and eventually performs them after state write. As a compromise, a few state updates are out-of-order, leading to accuracy drop. However, such accuracy drop is negligible and acceptable for most applications.

Write acknowledgment. As shown in Figure 6(a), applications issue a write operation comprising a set of state updates to the write engine. The write engine encapsulates these updates in several packets. For each packet, it allocates a dedicated timer and waits to receive an ACK after sending

the packet to the destination switch ASIC. The write handler in the switch ASIC conforms every packet sent by the write engine. Specifically, it performs the state updates to modify state values, and then sends an ACK back. If a timer raises a timeout, which indicates the loss of a packet, the write engine immediately retransmits the packet. After all the ACKs of sent packets are received, it notifies applications with write success and informs the write handler of termination.

Atomicity mechanism. At times, applications need to simultaneously write multiple state values, which requires *atomicity* to avoid unpredictable results. For instance, before starting a new time interval, network measurement applications need to reset the entire counter array in the switch ASIC to prevent legacy traffic statistics from disturbing ongoing measurement [49, 85]. However, during state write, data plane packets also continuously update the state in the switch ASIC, which harms atomicity. One strawman solution is to involve concurrency control methods [16, 35, 83] to avoid conflicts between state write and new state updates incurred by data plane packets. However, existing concurrency control methods cannot be implemented on programmable switches. The reason is that these methods either need excessive memory (e.g., 2PL [17], timestamp ordering [17], optimistic concurrency control [47], 2PC [70], and 3PC [71]) or require complicated queue scheduling (e.g., deterministic system [62]).

To this end, ApproSync offers a hardware-compatible atomicity mechanism. As depicted in Figure 6(b), the basic idea is to lock the *entire* state in the data plane and suspend new state updates during state write. It handles the suspended updates by means of the *recirculation* mechanism in switches. Specifically, packets arriving during state write are normally forwarded. However, the new state updates incurred by these packets are recirculated for a second-pass processing, which eventually performs state updates. The recirculation continues until state write is fully completed and the lock is free.

The motivation behind is three-fold: (1) For most applications, the priority of state write is higher than data plane updates. This is because state write raised by applications usually changes processing strategies (e.g., reset a data structure or modify control policies after observing a specific event). Thus, by prioritizing state write, ApproSync guarantees that merely using one lock is sufficient for resolving concurrency conflicts. It also naturally avoids deadlocks since only state write can obtain the lock; (2) ApproSync does not involve complicated operations or require excessive memory, such that it can be easily implemented in the switch ASIC; (3) ApproSync bypasses the switch OS to achieve low latency. Thus, the number of recirculated state updates is small, making the overhead on performance and accuracy negligible. The limitation of ApproSync is that the recirculation makes a few state updates out-of-order. However, most applications (e.g., measurement [51, 52] and load balancing [55]) are insensitive to such reordering.

4 USE CASES

In this section, we present three cases that enhance real applications via the state synchronization of ApproSync.

4.1 Sketch Collector

Sketch is a family of algorithms that has been extensively adopted in network measurement to fit switch memory limitations [38, 40, 51, 52, 82]. A sketch algorithm maintains a compact data structure. Every packet updates several counters in the data structure. The control plane collects the data structure at the end of each time interval and obtains various statistics for network management such as anomaly detection. Backing by sound theoretical guarantees, sketch algorithms achieve both high resource efficiency and high accuracy. However, existing approaches collect sketch structures inefficiently. They utilize the switch OS to serialize the values of the counters used by sketches. This incurs high latency overhead and hinders fine-grained deployment (e.g., in tens of milliseconds) of sketch algorithms, which eventually hurts the responsiveness of network management.

To this end, we build a low-latency sketch collector on ApproSync. Its workflow contains two steps: (1) When a packet updates sketch values, the read handler inserts those updates to the hash table via Algorithm 1; (2) It monitors the divergence between the sketch values in the data plane and those in the control plane. When the divergence exceeds the threshold, it pushes latest sketch values to the control plane, which reconstructs sketch data structures. Our experiments show that the collector significantly reduces the collection latency while maintaining high accuracy (see Exp#8 in §6).

4.2 State Migration

State migration transfers state values from one switch to another. It forms building blocks of many management tasks ranging from network redundancy [30, 32, 46, 67] to scalable network functions [74, 79]. Existing state migration techniques, such as OpenNF [28] and P4NFV [36], interact with switches using TCP connections to migrate states in a loss-free manner. Take P4NFV as an example. It demands the source switch to collect state values from the switch ASIC to the switch OS via PCIe channels, and send them to the control plane via TCP. Then it sends state values to the switch OS of a destination switch, which updates the local state resided in the switch ASIC. However, P4NFV suffers from high latency overhead incurred by PCIe channels and TCP connections, which compromises migration timeliness.

In response, we build a fast state migration framework atop the low-latency and accurate state synchronization of ApproSync. The framework performs two steps: (1) The read engine continuously receives state updates from the source switch. It extracts values from state updates and records them in a state storage; (2) The write engine sends state updates to the write handler in the destination switch to update the state. The experimental results indicate that the state migration framework offers low-latency (a few milliseconds) and accurate (no state loss) state migration (see Exp#9 in §6).

4.3 UDP Flood Prevention

A UDP flood attack is a type of denial of service attacks. The attackers randomly generate numerous UDP packets that target random UDP ports of innocent hosts. In this way, they can easily exhaust the available resources in victims. Existing approaches use per-flow counters resided in switches to detect such attacks [15, 27]. They rely on the OS-based approach to transfer counter values to the control plane for attack detection and periodically reset counters to mitigate measurement errors. However, the OS-based approach incurs non-trivial latency overhead that delays attack detection. Also, due to the lack of atomicity, the reset operations will be affected by data plane packets, leading to false alarms.

To overcome the above problems, we develop an application, namely UDP flood prevention (UFP), based on ApproSync. UFP employs FlowRadar [51] on the switch ASIC to record flow statistics. At runtime, UFP uses a three-step procedure to detect attacks: (1) The read handler transfers values of FlowRadar counters to the control plane; (2) The read engine receives counter values and inputs them to UFP to extract flow statistics and detect attacks; (3) The write engine periodically resets FlowRadar counters with atomicity guarantees. Our experiments indicate that UFP can efficiently detect attacks with high accuracy (see Exp#10 in §6).

5 IMPLEMENTATION

We have implemented a prototype of ApproSync, which targets P4-compatible switches. We maintain state values in registers. Note that P4 also offers another two components, i.e., counters and meters, to support stateful processing. ApproSync only targets registers because registers can not only realize the functions of counters and meters, but also support customizable operations towards state values.

Protocol. Figure 7 shows the format of state transfer, which follows the Ethernet header with a reserved protocol type "0xFFFF". The first field *seqNum* is the sequence number used by the write engine to ensure operation reliability. The second field *FreeLock* indicates whether to release the write lock or not. Moreover, the third field *StateNum* records the total number of state updates appended in the packet header.

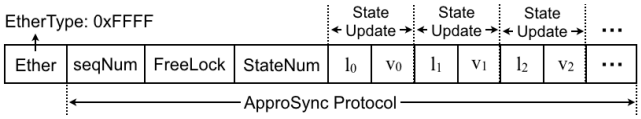


Figure 7: Protocol format of state transfer.

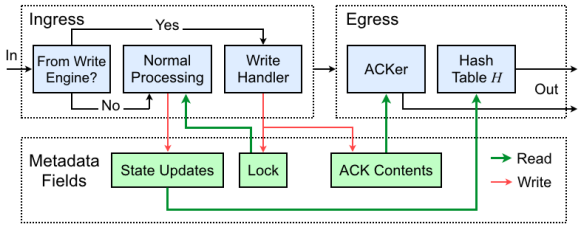


Figure 8: Workflow of the switch ASIC.

The remaining fields record state updates, each of which comprises a 16-bit location and a 64-bit state value. Here, 16 bits and 64 bits correspond to the maximum size of location and the maximum size of state value, respectively. Thus, such design can support arbitrary validate sizes of state updates.

Data plane handlers. Figure 8 details the P4 implementation of ApproSync handlers. For the read handler, ApproSync records every state update in metadata fields in the ingress pipeline. The updates are sent to the hash table resided in the egress pipeline. We implement the hash table with match-action tables (MATs) and registers. The egress pipeline reserves a dedicated port, which pushes state updates to the control plane based on the processing results of hash table. For the write handler, ApproSync employs an MAT in the start of the ingress pipeline to identify the type of each received packet. Normal packets are processed by the user program. Otherwise, when the packet indicates a write operation in the format as Figure 7, the write handler is invoked to handle it. We implement both state lock signal and ACK components with P4 metadata fields and registers.

Note that we use both an ingress pipeline and an egress pipeline rather than a single pipeline. This is because the ingress pipeline determines which egress port to forward packets based on state values, while the egress pipeline is binding to the port connected to the controller. Thus, we place the functions that access state values on the ingress pipeline, and put the functions that interact with the control plane on the egress pipeline.

Control plane engines. We implement both read engine and write engine in C. Our implementation provides the interfaces for both the data plane (southbound APIs) and applications (northbound APIs). We implement the southbound APIs with DPDK [6] to eliminate the latency incurred by kernel stacks. We employ Redis [9] as the state storage and use HiRedis [5] to manage the storage. For the northbound APIs, we design a suite of intuitive interfaces for applications to manage states stored in Redis.

Compiler. We implement a compiler to integrate ApproSync handlers into the user program written in $P4_{14}$ or $P4_{16}$. The compiler first inserts the P4 codes that implement ApproSync handlers to the user program. It then augments the user program to connect it with ApproSync handlers: (1) For the read handler, the compiler identifies each state update in the program and records the update in metadata fields, which are delivered to the read handler for further processing; (2) For the write handler, the compiler adds an additional logic that handles state updates via the write handler. Our compiler enables administrators to select registers to be synchronized. By default, it chooses to synchronize all registers.

6 EVALUATION

In this section, we conduct experiments to evaluate our ApproSync prototype. We highlight our results as follows.

- ApproSync incurs less than 15% usage of memory and computational resources in switches (Exp#1).
- Compared to the OS-based approach, ApproSync achieves order-of-magnitude latency reduction in state read (Exp#2).
- Compared to *Flow [73], ApproSync avoids link saturation and state loss via its rate control in state read (Exp#3).
- Even in a link with 80% loss rate, ApproSync writes 2^{16} updates within 10 ms, whereas the OS-based approach spends two orders of magnitude higher latency (Exp#4).
- The state write of ApproSync preserves high accuracy for applications (Exp#5).
- ApproSync does not degrade the throughput. It increases the latency of packet forwarding by less than 5% (Exp#6).
- ApproSync achieves ultra-low (at most 23 ms) state read and write latency for 16 real-world applications (Exp#7).
- ApproSync enables low-latency and accurate sketch collection (Exp#8).
- ApproSync completes loss-free state migration within 10 ms (Exp#9).
- ApproSync prevents UDP flood attacks in a timely and highly accurate manner (Exp#10).

6.1 Methodology

Platforms. We build a testbed comprising two 32×100 Gbps Barefoot Tofino switches [2] and six servers, each of which has 36-core Intel(R) Xeon(R) Gold 6240C CPU (2.60 GHz), 128GB RAM and a two-port 40 Gbps NIC. We run the control plane of ApproSync on a dedicated server. In the data plane, we connect the two switches to compose a linear topologic, while using the remaining five servers as traffic testers. In our testbed, the control plane and traffic testers are directly connected to the two switches via 40-Gbps ports.

Workloads. We select a one-hour CAIDA trace [3] with 38M packets. We use PktGen [8] to replay the trace. In addition to the applications in §4, we consider another 16 stateful P4 applications listed in Table 1. In each experiment, we present the average after 100 runs.

Table 1: Stateful P4 applications used in §6.

Name	P4 LoC	# of counters	Size[1]
Packet counter (PC) [7]	265	2^{16}	6
Flowlet switching (FL) [7]	251	2^{14}	10
Malicious DNS domain detection (MD) [15]	358	3×2^{16}	4
Snort flowbits (FB) [15]	296	3×2^{16}	4
Affine LB (AL) [15]	345	2^{17}	4
DNS TTL change tracking (TC) [19]	357	3×2^{16}	6
DNS tunnel detection (TD) [19]	530	3×2^{16}	4
Stateful firewall (FW) [57]	349	2^{17}	4
FTP monitoring (FM) [57]	303	2^{16}	4
Heavy hitter detection (HH) [57]	310	2^{17}	6
Super-spreader detection (SS) [57]	313	2^{17}	4
Sampling based on flow size (FS) [57]	560	5×2^{16}	4
SYN flood detection (SF) [27]	313	2^{17}	4
DNS amplification mitigation (AM) [27]	360	2^{16}	4
UDP flood mitigation (UF) [27]	309	2^{17}	4
Elephant flows detection (EF) [27]	553	5×2^{16}	4

Parameters. In our experiments, the hash table H has 2^{16} entries by default. We fix the time window w to 1 ms and use a $\beta = 1$, which are sufficient for all applications. For each application in Table 1, we obtain the size s of a state update and calculate the maximum emitted rate M as $\frac{c}{s}$, where c is a constant implying the capacity of a 40 Gbps link. Moreover, unless specified otherwise, ApproSync will automatically tune t to adapt to the rate of input traffic.

6.2 Microbenchmarks

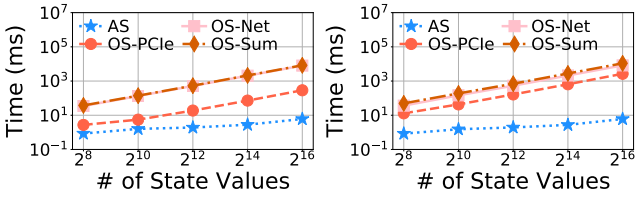
(Exp#1) Switch resource usage. This experiment measures the total usage of switch resources, including memory resources, computational resources, and match-action stages. Here, memory includes both SRAM and TCAM, while computational resources include meter ALUs (mALUs), stateful ALUs (sALUs), and very long instruction words (VLIWs). Note that ApproSync (AS) provides one primitive for state read, and one primitive for state write. We measure their resource consumption individually and the overall consumption of all primitives. Table 2 shows that ApproSync uses less than 15% resources even when using all the primitives in one switch. Moreover, ApproSync uses all the stages since interdependent MATs must be placed in different stages due to switch restrictions. Nevertheless, it uses limited resources and remains sufficient resources in each stage for other logics. We present more experimental results on Appendix A.

(Exp#2) Performance of state read. We measure the latency of state read. We vary the number of state values from 2^8 to 2^{16}. We employ two types of state: 16-bit state and 64-bit state, where 16-bit is widely used by applications and 64-bit is the largest size supported by our switches. We build the OS-based approach based on the interfaces exposed by our switches [2] and ZeroMQ [11]. We measure three types of latency in the OS-based approach: the latency of reading

[1] "size" indicates the size (in bytes) of a state update.

Table 2: (Exp#1) Switch resource usage of ApproSync.

Type	SRAM	TCAM	mALU	sALU	VLIW	Stage
Only Read	6.77%	0%	14.58%	0%	4.69%	91.6%
Only Write	2.40%	0%	0%	3.65%	3.82%	100%
Overall	9.17%	0%	14.58%	3.65%	5.21%	100%



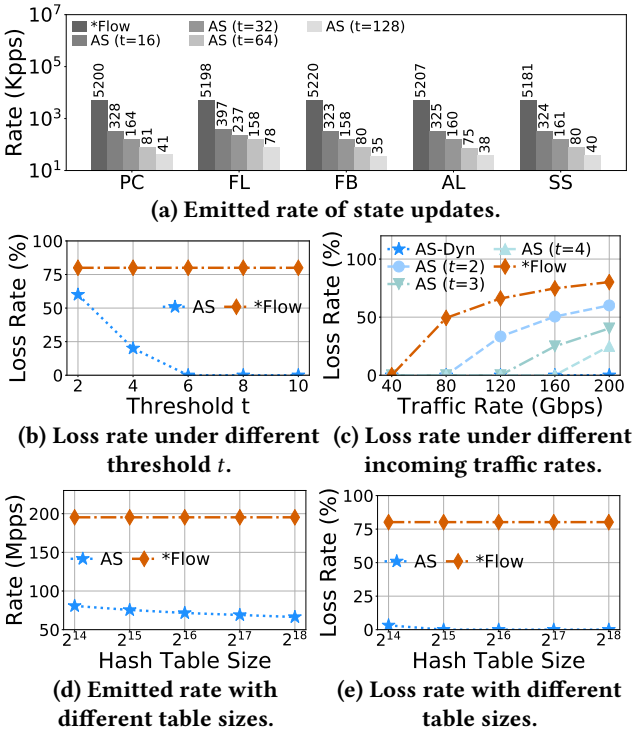
(a) 16-bit state value. **(b) 64-bit state value.**

Figure 9: (Exp#2) Performance of state read.

state values from the switch ASIC to the switch OS via PCIe channels (OS-PCIe), the latency of transferring state values via TCP connections (OS-Net), and the sum of the former two (OS-Sum). Figure 9 presents that the latency of OS-based approach exceeds one second when a state has 2^{16} values. When using 64-bit state, even reading state via PCIe channels takes at least tens of milliseconds. In contrast, the latency of ApproSync remains below 10 ms in all cases.

(Exp#3) Accuracy of state read. We evaluate the accuracy of ApproSync in state read. First, we validate that ApproSync can avoid link saturation via its rate control. Recall that a state update is transferred when the state divergence reaches the threshold t. We replay our trace at 40 Gbps and employ t ranging from 16 to 128. Since the emitted rate of state updates depends on how an application updates state, we select five applications, in which every packet triggers an update, from Table 1. We compare ApproSync with *Flow [73], a traffic mirroring-based system that uses an LRU cache for rate control. We configure the LRU cache with the same configuration as the hash table of ApproSync. Figure 10(a) shows that *Flow brings limited benefits because its LRU cache is frequently evicted given that the number of flows far exceeds the cache size. In contrast, ApproSync significantly reduces bandwidth consumption via its rate control. Its benefits increase as the growth of t. For example, it only incurs 35 Kpps for *Snort flowbits* (SF) [15] when t is 128.

Second, we validate that ApproSync can offer accurate state read via its rate control. We deploy *packet counter* (PC) that generates a state update for every packet. We inject traffic at 200 Gbps so that the emitted rate of state updates far exceeds link capacity. We manually configure the read handler by varying its threshold t from 2 to 10. Figure 10(b) shows that ApproSync gradually reduces emitted rate as t increases, and avoids state loss when t exceeds 5. Then we repeat the experiment without any manual settings. Figure 10(c) shows that ApproSync (AS-Dyn) offers loss-free state read because its read handler dynamically tunes t to



(a) Emitted rate of state updates.

(b) Loss rate under different threshold t. **(c) Loss rate under different incoming traffic rates.**

(d) Emitted rate with different table sizes. **(e) Loss rate with different table sizes.**

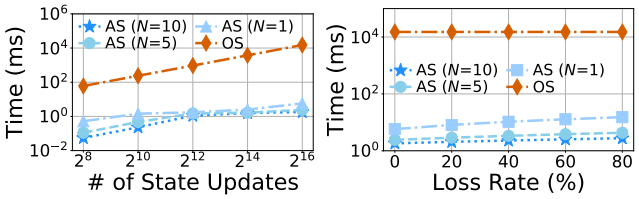
Figure 10: (Exp#3) Accuracy of state read.

adapt to incoming traffic rate. In contrast, ApproSync with fixed t ($t < 5$) and *Flow cannot guarantee no state loss, which emphasizes the importance of rate control.

Third, we study the impact of hash table size on accuracy. We vary the size from 2^{14} to 2^{18} entries. We conduct the same experiment as above. Figure 10(d)-(e) show that ApproSync loses a few state updates (3.22%) when using 2^{14} entries. This is because hash collisions happen frequently given the high traffic rate and relatively small table size. However, ApproSync remarkably alleviates this problem via its adaptive rate control. When using 2^{15} entries, the rate control of ApproSync ensures loss-free state read, while *Flow suffers from significant state loss. Note that such state loss can be totally avoided by setting a higher table size, e.g., 2^{16} entries are sufficient for ApproSync to avoid state loss for all the applications in Table 1 even with 200 Gbps traffic.

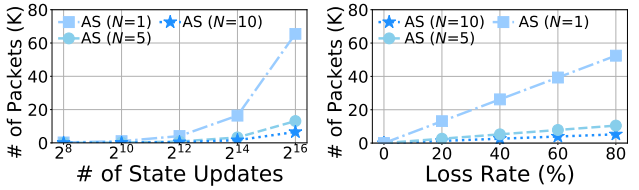
(Exp#4) Performance of state write. We measure the performance of state write. ApproSync splits a write operation into several partial operations, each of which is completed by a single packet. Thus, the performance of state write depends on the number N of state updates encapsulated in a packet. We set N to 1, 5, and 10, and vary the number of state updates from 2^8 to 2^{16}. Figure 11(a) shows that ApproSync reduces the latency by orders of magnitude even when N=1 by eliminating the overhead of switch OS.

We next study the robustness of state write in a congested link. In this case, ApproSync needs to retransmit dropped



(a) Latency of state write without state loss.

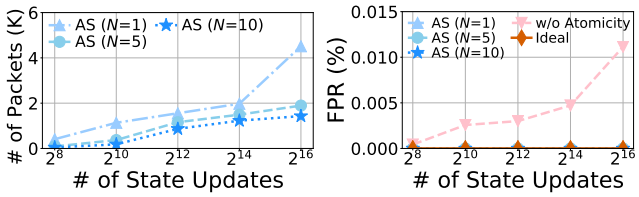
(b) Latency of state write with state loss.



(c) # of pkts for state write.

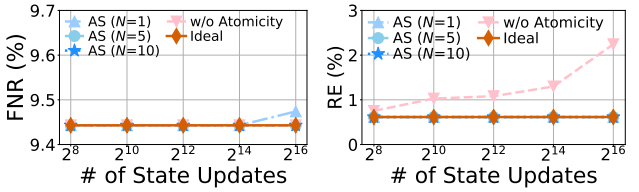
(d) # of retransmitted pkts.

Figure 11: (Exp#4) Performance of state write.



(a) # of out-of-order updates.

(b) Impact on false positive.



(c) Impact on false negative.

(d) Impact on relative error.

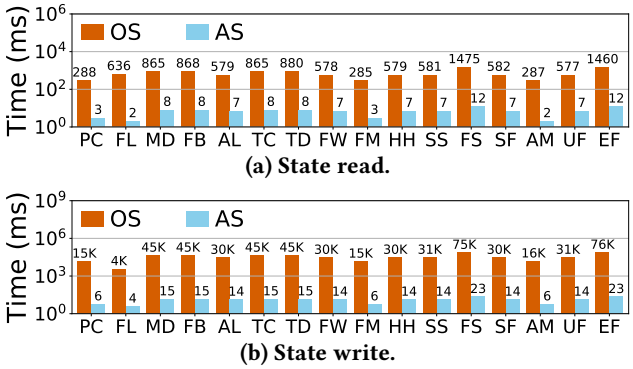
Figure 12: (Exp#5) Accuracy of state write.

Table 3: (Exp#6) Impact on packet forwarding.

Name	Thpt.	Latency	Thpt. cost	Latency cost
NoApproSync	39.99 Gbps	1073 ns	-	-
Only Read	39.99 Gbps	1123 ns	+0.0%	+4.6%
Only Write	39.99 Gbps	1101 ns	+0.0%	+2.6%
Overall	39.99 Gbps	1141 ns	+0.0%	+6.3%

state updates, which increases the latency. Here, we use ApproSync to write 2^{16} state updates and measure its latency when the state lose rate ranges from 0% to 80%. Figure 11(b) presents that even with 80% loss rate, ApproSync completes state write in a few milliseconds. In addition, we measure the bandwidth consumed by state write. Figure 11(c)-(d) present the number of packets for a write operation and that for retransmission under different loss rates. Even in the worst case, the number of generated packets is at most 65K, which is far below link capacity (e.g., 14.88 Mpps of a 10 Gbps link).

(Exp#5) Accuracy of state write. We measure the accuracy of ApproSync in state write. ApproSync recirculates



(a) State read.

(b) State write.

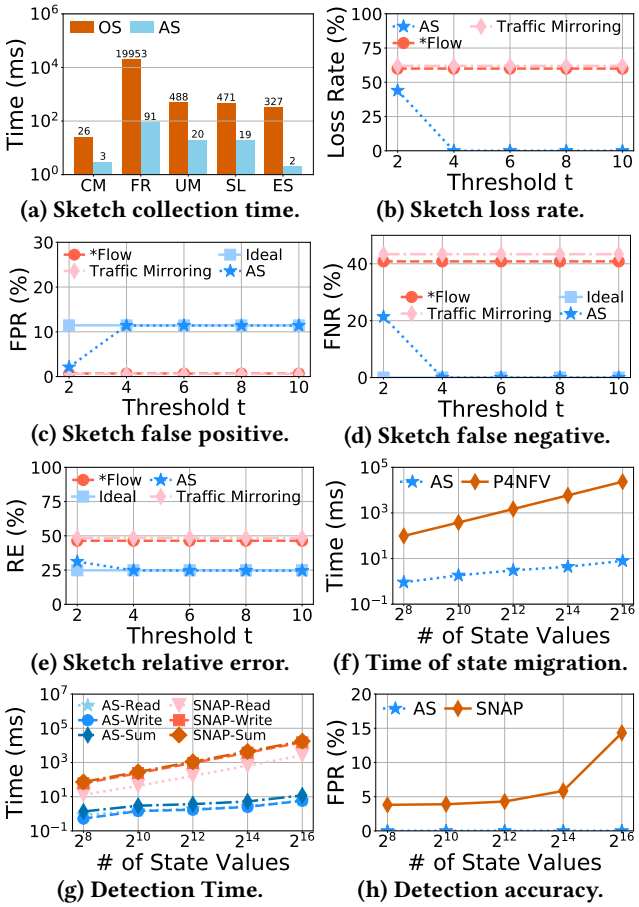
Figure 13: (Exp#7) Application-perceived latency.

state updates during state write to maintain atomicity, which brings two types of overheads: (1) the recirculation consumes a portion of switch bandwidth; (2) the recirculation affects the original order between state updates that may reduce accuracy. To quantify these overheads, we first count the number of out-of-order updates during state write. We deploy HashPipe [69], a heavy hitter detection algorithm, with 5K counters on a switch. The accuracy of HashPipe is associated with every state update so that it can accurately reflect the impact of state write. As shown in Figure 12(a), ApproSync affects at most 4.5K updates. Even in the worst case, it only consumes 300 Kpps bandwidth, which is far below Mpps-level switch bandwidth. This is because its state write is low-latency, so the number of affected updates and bandwidth consumption are small. Next, we examine the impact on HashPipe accuracy. Figure 12(b)-(d) show that: (1) the out-of-order updates only increase false negative rate and relative error by at most 0.2% and 0.03%, which is negligible; (2) compared to the OS-based approach, ApproSync offers highly accurate state write with atomicity guarantees.

(Exp#6) Impact on packet forwarding. Table 3 examines how ApproSync affects the throughput and per-packet latency. We consider four cases. (1) "NoApproSync" disables ApproSync and presents the original performance. (2) "Only read" presents the results when only the read handler is activated. (3) "Only write" shows the results of state write. (4) "Overall" enables full functionalities. We observe that ApproSync incurs nearly zero throughput drop while adding the per-packet processing latency by at most 6.3%.

6.3 Real Applications

(Exp#7) Latency for stateful P4 applications. This experiment measures the application-perceived latency of state read and write operations of ApproSync. We implement the 16 stateful P4 applications in Table 1 with various complexity, resource consumption and state management patterns in Table 1. We measure the time of ApproSync when reading states from the counters used by applications and resetting



(a) Sketch collection time. (b) Sketch loss rate.

(c) Sketch false positive. (d) Sketch false negative.

(e) Sketch relative error. (f) Time of state migration.

(g) Detection Time. (h) Detection accuracy.

Figure 14: (Exp#8-10) Trade-offs in real cases.

counters. We compare ApproSync with the OS-based approach. Figure 13(a) shows that ApproSync completes state read within 12 ms, while the OS-based approach takes at least 285 ms. ApproSync brings more benefits for state write, shown in Figure 13(b). It requires at most 23 ms, while the OS-based approach requires several seconds.

(Exp#8) Performance and accuracy of sketch collector. We evaluate the performance and accuracy of the sketch collector built atop ApproSync. We consider five sketch-based solutions, Count-Min (CM) [24], FlowRadar (FR) [51], UnivMon (UM) [52], SketchLearn (SL) [40] and ElasticSketch (ES) [82]. We deploy these solutions on a switch and use the sketch collector to periodically collect sketch values from the switch. Figure 14(a) indicates that compared to the OS-based approach, ApproSync reduces the collection time by orders of magnitude. This implies future deployment of sketch-based solutions to identify network events with ApproSync.

Next, we inject traffic at 120 Gbps to examine the loss rate of state updates. Figure 14(b) presents the loss rate with respect to the threshold t that determines the emitted rate of state updates. We compare ApproSync against traffic mirroring and *Flow. We observe that traffic mirroring and *Flow loss around 60% state updates due to the lack of a reasonable rate control. ApproSync also suffers from a high loss rate when its threshold $t = 2$. However, the state loss is completely eliminated as the threshold increases.

Finally, we qualify the accuracy of heavy hitter detection. In the interest of space, we only present the results of CM. We measure its false positive rate, false negative rate, and relative error in Figure 14(c)-(e), respectively. In addition to traffic mirroring and *Flow, we build an original version of CM without any state loss ("Ideal") as ground truth. We observe that traffic mirroring and *Flow achieve relatively small false positive rate. The reason is that false positives are caused by overestimating flows. Clearly, high loss rate mitigates overestimates so that traffic mirroring and *Flow have low false positive rate. However, state loss seriously improves false negative rate and relative error. In contrast, ApproSync achieves near-optimal accuracy closed to "Ideal".

(Exp#9) Performance and accuracy of state migration. We evaluate the state migration framework based on ApproSync. We measure the latency of migrating state values, the number of which varies from 2^8 to 2^{16}. Figure 14(f) compares our framework with P4NFV [36], which migrates states via the OS-based approach. We see that P4NFV takes nearly 23s for the migration of 2^{16} state values, while our framework completes within 10 ms. Also, ApproSync achieves loss-free state migration in all cases, which indicates its high accuracy.

(Exp#10) Performance and accuracy of UDP flood prevention. We evaluate UDP flood prevention (UFP) running on ApproSync. We vary the number of state values from 2^8 to 2^{16}, and measure the latency of collecting and resetting these values ("AS-Read" and "AS-Write") via UFP. We also quantify the accuracy of UFP by measuring its false positive rate. We set the detection threshold to 10^5, and compare UFP with the SNAP method [15] based on OS-based approach. Figure 14(g)-(h) shows that UFP achieves orders-of-magnitude latency reduction compared to SNAP. Moreover, with atomicity guarantees, it achieves zero false positive rate, while SNAP suffers from a few errors.

7 RELATED WORK

State read. To shed bandwidth consumption in state read, prior solutions employ sampling techniques [10, 26, 34, 61, 65, 84]. However, sampling techniques inevitably degrade accuracy. Some recent works exploit the line-rate speed of programmable switches to optimize state read. TurboFlow [72] treats state values as flow records, and then processes flow records in the switch OS. However, a switch OS fails to process multi-Tbps state updates and incurs high latency. In

contrast, ApproSync bypasses the switch OS to avoid performance overhead. Moreover, some solutions [18, 22] adopt traffic mirroring to realize realtime monitoring. However, these solutions suffer from serious state loss as revealed in §2. ApproSync mitigates state loss and outperforms these solutions with higher accuracy via its adaptive rate control. Marple [58] caches flow records in the switch ASIC before mirroring states to remote servers. However, it does not consider the actual impact of state updates. A state is evicted even its update is insignificant, seriously saturating link capacity (see Exp#3 in §6). ApproSync improves in-switch caching by adaptively controlling the trade-off between accuracy and bandwidth consumption. KeySight [85] aggregates packets based on packet processing behaviors to reduce overhead. Sonata [33] pre-processes packets in switches to reduce workloads in the control plane. ApproSync is orthogonal and complementary to these solutions by providing them with efficient and accurate state synchronization.

State write. Commodity controllers modify states via TCP-based protocols such as OpenFlow [54], Thrift [1] and gRPC [4], which require a switch OS for complicated processing. Applications built on these protocols (e.g., P4NFV [36]) suffer from high latency. Swing State [53] directly migrates state values in the data plane to achieve rapid state migration. P4State [37] takes a step further to only migrate essential state values to reduce migration overhead. However, the write operations issued by these solutions could be lost. Instead, ApproSync provides low-latency and loss-free state write.

Approximate systems. Approximation is a well-studied topic in distributed systems, including database [12], machine learning systems [50, 80, 81], and stream processing systems [13, 39, 60]. BlinkDB [12] samples a subset of data to dynamically estimate the response time and error of a database query. JetStream [60] uses data aggregation and adaptive filtering to achieve trade-offs between accuracy and resource efficiency. AF-Stream [39] provides approximate fault tolerance in the content of stream processing. On the contrary, ApproSync exploits approximate techniques to achieve low-latency and accurate state synchronization between programmable switches and control plane.

8 CONCLUSION

We propose ApproSync, a state synchronization framework, with a primary goal of achieving state consistency between the data plane and control plane. ApproSync exploits approximate techniques to alleviate resource consumption and bound errors during state synchronization. It offers two types of synchronization for state read and state write while achieving low latency and high accuracy. We implement a ApproSync prototype atop Barefoot Tofino switches. Experiments with real-world traces and stateful P4 applications indicate that ApproSync outperforms existing solutions with order-of-magnitude latency reduction and higher accuracy.

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APPENDIX A: MORE EXPERIMENTS

(Exp#11) Switch resource consumption of ApproSync. This experiment measures the resource consumption of ApproSync. We deploy the sixteen applications in Table 1 and the seven applications used by Exp#8-#10 in §6.3, including the sketches used by the sketch collector, the state migration framework (SM), and UDP flood prevention (UFP), on a programmable switch, respectively. We quantify the resource consumption of ApproSync by measuring the switch resource usage with and without ApproSync. As shown in Table 4, ApproSync consumes less than 15% computation resources and no more than 7% memory resources. This indicates that ApproSync is resource-efficient and adds negligible overheads to the deployment of data plane programs.

Table 4: (Exp#11) Resource usage of ApproSync applications.

Name	SRAM		TCAM		mALU	
	w/o ApproSync	w/ ApproSync	w/o ApproSync	w/ ApproSync	w/o ApproSync	w/ ApproSync
PC	1.88%	6.88% (+5%)	0%	0% (+0%)	2.08%	16.66% (+12.50%)
FL	0.94%	7.81% (+6.87%)	0%	0% (+0%)	2.08%	16.67% (+14.59%)
MD	2.81%	9.69% (+6.88%)	0%	0% (+0%)	6.25%	20.83% (+14.58%)
FB	1.88%	8.75% (+6.87%)	0%	0% (+0%)	4.17%	18.75% (+14.58%)
AL	1.88%	8.75% (+6.87%)	0%	0% (+0%)	4.17%	18.75% (+14.58%)
TC	3.65%	10.52% (+6.87%)	0%	0% (+0%)	6.25%	20.83% (+14.58%)
TD	2.81%	10.52% (+7.71%)	0%	0% (+0%)	6.25%	20.83% (+14.58%)
FW	1.04%	8.12% (+7.08%)	0%	0% (+0%)	4.17%	18.75% (+14.58%)
FM	0.94%	7.81% (+6.87%)	0%	0% (+0%)	2.08%	16.67% (+14.59%)
HH	1.88%	8.75% (+6.87%)	0%	0% (+0%)	4.17%	18.75% (+14.58%)
SS	1.88%	8.75% (+6.87%)	0%	0% (+0%)	4.17%	18.75% (+14.58%)
FS	4.69%	11.56% (+6.87%)	0%	0% (+0%)	10.42%	25.00% (+14.58%)
SF	1.88%	8.75% (+6.87%)	0%	0% (+0%)	4.17%	18.75% (+14.58%)
AM	0.94%	7.81% (+6.87%)	0%	0% (+0%)	2.08%	16.67% (+14.59%)
UF	1.88%	8.75% (+6.87%)	0%	0% (+0%)	4.17%	18.75% (+14.58%)
EF	2.81%	9.68% (+6.87%)	0%	0% (+0%)	6.25%	20.83% (+14.58%)
CM	0.31%	7.18% (+6.87%)	0%	0% (+0%)	2.08%	16.66% (+14.58%)
FR	39.38%	46.25% (+6.87%)	0%	0% (+0%)	50.00%	64.58% (+14.58%)
UM	38.85%	45.72% (+6.87%)	0%	0% (+0%)	68.75%	83.33% (+14.58%)
SL	38.85%	45.72% (+6.87%)	0%	0% (+0%)	68.75%	83.33% (+14.58%)
ES	1.98%	8.85% (+6.87%)	0%	0% (+0%)	18.75%	33.33% (+14.58%)
SM	2.81%	9.68% (+6.87%)	0.35%	0.35% (+0%)	4.17%	18.75% (+14.58%)
UFP	39.38%	46.25% (+6.87%)	0%	0% (+0%)	50.00%	64.58% (+14.58%)

Name	sALU		VLIW		Stage	
	w/o ApproSync	w/ ApproSync	w/o ApproSync	w/ ApproSync	w/o ApproSync	w/ ApproSync
PC	0%	0% (+0%)	0.52%	4.69% (+4.17%)	8.33%	100% (+91.67%)
FL	0%	0% (+0%)	0.52%	4.69% (+4.17%)	16.66%	100% (+83.34%)
MD	0%	0% (+0%)	1.30%	4.69% (+3.39%)	33.33%	100% (+66.67%)
FB	0%	0% (+0%)	0.78%	4.95% (+4.17%)	16.66%	100% (+83.34%)
AL	0%	0% (+0%)	1.30%	4.69% (+3.39%)	25%	100% (+75%)
TC	0%	0% (+0%)	1.30%	5.21% (+3.91%)	25%	100% (+75%)
TD	0%	0% (+0%)	2.86%	5.21% (+2.35%)	50%	100% (+50%)
FW	0%	0% (+0%)	1.56%	4.69% (+3.13%)	25%	100% (+75%)
FM	0%	0% (+0%)	0.26%	4.69% (+4.43%)	8.33%	100% (+91.67%)
HH	0%	0% (+0%)	0.78%	4.69% (+3.91%)	25%	100% (+75%)
SS	0%	0% (+0%)	0.78%	4.69% (+3.91%)	25%	100% (+75%)
FS	0%	0% (+0%)	3.65%	6.25% (+2.60%)	50%	100% (+50%)
SF	0%	0% (+0%)	0.78%	4.69% (+3.91%)	25%	100% (+75%)
AM	0%	0% (+0%)	1.82%	4.95% (+3.13%)	41.66%	100% (+58.34%)
UF	0%	0% (+0%)	1.04%	4.95% (+3.91%)	25%	100% (+75%)
EF	0%	0% (+0%)	2.60%	5.47% (+2.87%)	50%	100% (+50%)
CM	0%	0% (+0%)	1.04%	3.87% (+2.83%)	25%	100% (+75%)
FR	0%	0% (+0%)	3.12%	6.51% (+3.39%)	91.66%	100% (+8.34%)
UM	0%	0% (+0%)	3.39%	5.76% (+2.37%)	100%	100% (+0%)
SL	0%	0% (+0%)	3.39%	5.76% (+2.37%)	100%	100% (+0%)
ES	0%	0% (+0%)	3.91%	6.51% (+2.60%)	100%	100% (+0%)
SM	0%	0% (+0%)	2.34%	6.25% (+3.91%)	41.66%	100% (+58.34%)
UFP	0%	0% (+0%)	3.12%	6.51% (+3.39%)	91.66%	100% (+8.34%)