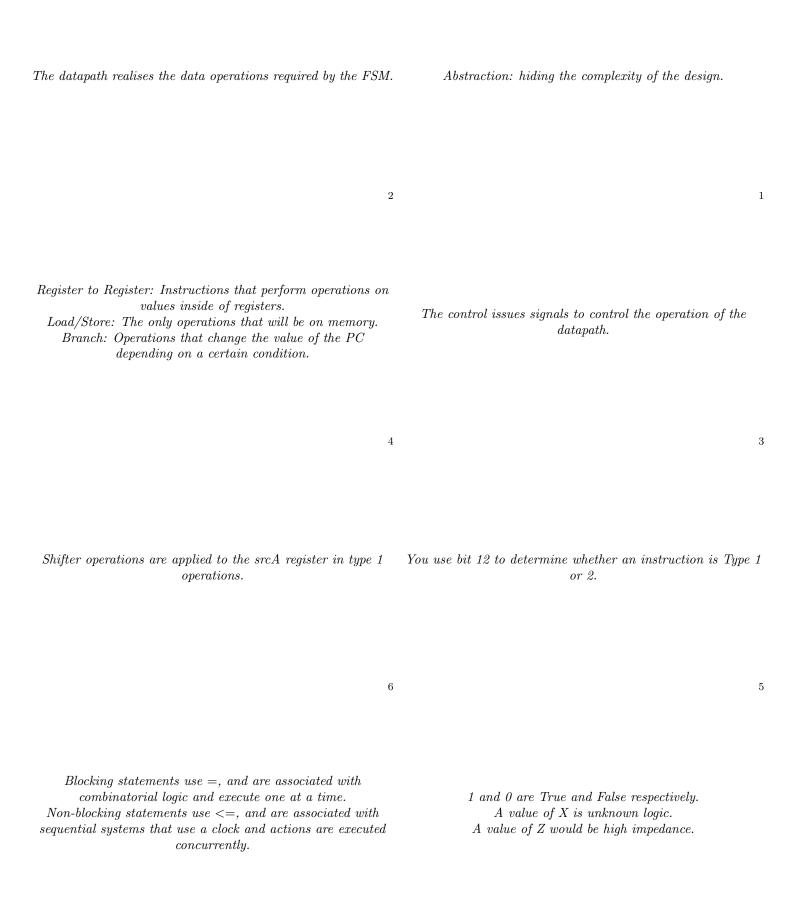
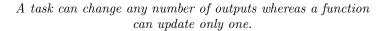
: hiding the complexity of the design.	The realises the data operations required by the FSM .
The issues signals to control the operation of the datapath.	A Reduced Instruction Set Computer (RISC) has three instruction types. What are they, and in brief what do they do?
You use bit to determine whether an instruction is Type 1 or 2.	Shifter operations are applied to the register in operations.
In Verilog, there are four options for a bit to be. 0, 1, X and Z . In brief, what does each one mean?	What type of circuits do you associate the use of i) blocking statements, and ii) non-blocking statements in Verilog code?



Do you have to use the default case in Verilog? When would you use it?	What is the difference between a Verilog task and a Verilog function?
9	10
Where would you locate a task or function in your Verilog code?	Why does Stump's R0 exist? Give some examples illustrating its use.
11	12
$What \ is \ a \ load/store \ architecture?$	How can pipelining accelerate performance of a processing system?
10	



Not necessarily. It is useful to cover cases not listed in the case statement, trapping any invalid states you shouldn't be in.

10

9

Allows you to enable further operations to be implemented that are not part of the ISA.

- MOV: ADD R3, R2, R0 - NOP: ADD R0, R0, R0 - CMP: SUBS R0, R3, R4 $\label{lem:lemondule} \begin{tabular}{ll} It needs to be within the module but outside any always/initial \\ blocks. \end{tabular}$

12

11

By introducing parallelism at a small cost. It allows more instruction throughput at a given clock rate than would traditionally be possible.

Data within registers will only be operated on, with results being written back to registers. LD/ST operations will be included for memory operations.