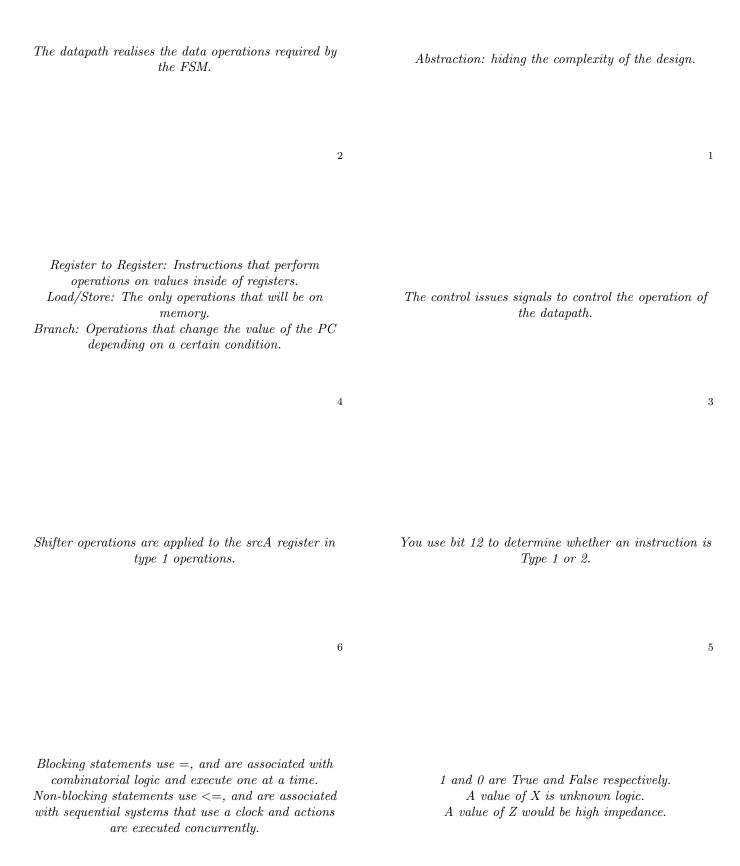
: hiding the complexity of the design.	The realises the data operations required by the FSM.
The issues signals to control the operation of the datapath.	A Reduced Instruction Set Computer (RISC) has three instruction types. What are they, and in brief what do they do? Hint: Stump is a RISC computer
You use bit to determine whether an instruction is Type 1 or 2.	Shifter operations are applied to the $\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \$
In Verilog, there are four options for a bit to be. 0, 1, X and Z. In brief, what does each one mean?	What type of circuits do you associate the use of i) blocking statements, and ii) non-blocking statements in Verilog code?



Do you have to use the default case in Verilog? When would you use it?	What is the difference between a Verilog task and a Verilog function ?
Where would you locate a task or function in your Verilog code?	Why does Stump's R0 exist? Give some examples illustrating its use.
What is a load/store architecture?	How would you setup a Stump FSM with the inputs clk, rst, a 16 bit ir and a 2 bit register for state?
How would you design a clock for a verilog test?	How would you instantiate a Stump_FSM with the inputs clk, rst, an ir and a state for testing?

A task can change any number of outputs whereas a function can update only one.

Not necessarily. It is useful to cover cases not listed in the case statement, trapping any invalid states you shouldn't be in.

10

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Allows you to enable further operations to be implemented that are not part of the ISA.

- MOV: ADD R3, R2, R0 - NOP: ADD R0, R0, R0 - CMP: SUBS R0, R3, R4 It needs to be within the module but outside any always/initial blocks.

12

11

```
module \ Stump\_FSM \ (input \ wire \ clk, \\ input \ wire \ rst, \\ input \ wire \ [15:0] \ ir, \\ output \ reg \ [1:0] \ state); \\ end module
```

Stump FSM

Data within registers will only be operated on, with results being written back to registers. LD/ST operations will be included for memory operations.

```
14
```

13

```
Stump\_FSM\ variableName\ (\\ .clk(var1),\ .rst(var2),\ .ir(var3),\ .state(var4)\\ );
```

Instantiated $Stump_FSM$

```
\begin{array}{c} always \\ begin \\ \#100 \ // \ Time \ per \ clock \ change \\ clock = !clock \\ end \end{array}
```

 $Clock\ example$

	_
In Stump, name the four flags and, when 'S' is appended to an instruction, how they go high.	The extends immediate values in Stump for Type 2 and Type 3 instructions.
The in stump performs shift operations on the srcA register on Type 1 instructions.	What are the differences between the Von Neuman architecture and the Harvard architecture?
Compare and contrast the ARM ISA's and the x86 ISA's techniques for branching to a subroutine.	(ISA) is the visible view of the processor (what is exposed to the programmer).
is the hardware view on a processor.	Name some ways that a processor can be made faster.

The Sign Extender extends immediate values in Stump for Type 2 and Type 3 instructions.

N - the negative flag is set if the ALU result is negative.

Z - the zero flag is set if the result is zero.

 $oldsymbol{V}$ - the overflow is set if the result from an addition/subtraction interpreted as a two's complement is wrong.

C - the carry flag is set if there is a carry out from the most significant bit of the result (bit 15).

Flags

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Von Neuman

- has one bus for both data transfers and instructions
- a single, unified cache, which stores both instructions and data.

Harvard

- has separate data and instruction busses, allowing transfers to be performed simultaneously on both
- separate caches for each bus, as a shared cache would be difficult to manage.

Von Neuman v.s. Harvard

20

The Shifter in stump performs shift operations on the srcA register on Type 1 instructions.

19

22

18

ARM

- Single register allows for less implementation cost.
- Any other branch call will overwrite value in link register.

x86

- Stack based system has greater implementation cost.
- Allows for branch calls within branches, without loss of address.

ARM ISA vs x86 ISA

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Instruction Set Architecture (ISA) is the visible view of the processor (what is exposed to the programmer).

Increase the clock rate

- As a consequence of Moore's Law
- Through circuit design
- Through microarchitectural design, e.g. more parallelism

Do more in each cycle

- Parallelism within instruction execution

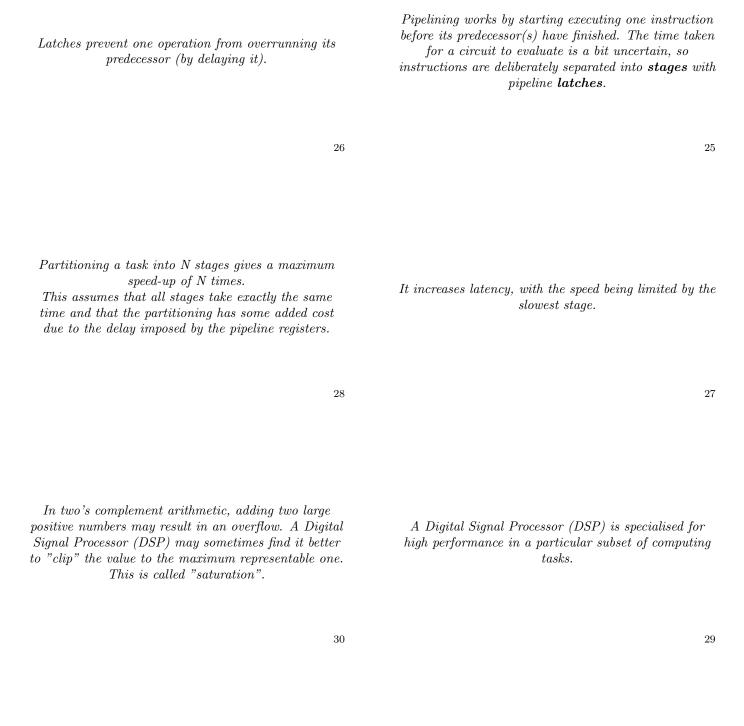
Do more in each instruction

- Somewhat limited by ISA as a completely new ISA is expensive.

Some possible ways of making a processor faster

Microarchitecture is the hardware view on a processor.

What are the basic principles of pipelining ?	prevent one operation from overrunning its predecessor (by delaying it).
25	26
How does pipelining effect latency?	What is the potential speed up of pipelining? Why isn't this always the case?
A (DSP) is specialised for high performance in a particular subset of computing tasks.	What is saturating arithmetic?
(SIMD) describes computers with multiple processing elements that perform the same operation on multiple data points simultaneously.	What are the two basic types of MOS-FETs (Metal-Oxide-Semiconductor Field Effect Transistors)?



Two types of MOS-FETs

open switch)

closed switch)

NMOS - with n-type channel (analogy to normally

PMOS - with p-type channel (analogy to normally

Single instruction, multiple data (SIMD) describes computers with multiple processing elements that perform the same operation on multiple data points simultaneously.

How do you calculate system performance?	When changing a functional design into a physical one, what is on the "wish list" of properties?
33	34

 $\begin{tabular}{ll} What does \it{PVT} stand for in the context of chip\\ design? \end{tabular}$

- Clock period (performance)
- Floorplan/pinout
- Area/density (cost)
 Using all the chip area for useful gates, but keeping the chip small to save cost.
- Power

Wish list of properties

 $time pertask = \\ clock period \times number of clock cycles pertask \\ performance \approx 1/(time pertask)$

34

- Manufacturing **Process** variation
- Varying operating $\emph{V}oltage$ $Typical\ voltage\ ranges\ my\ be\ \pm 10\%$
- $Different\ chip\ Temperature$

 $Typically, \ run \ simulation \ at \ extremes$