[redacted]: *hiding the complexity of the design.*

1

The [redacted] *realises the data operations required by the FSM.*

2

The [redacted] *issues signals to control the operation of the datapath.*

3

A Reduced Instruction Set Computer (RISC) has three instruction types. What are they, and in brief what do they do?

4

Shifter operations are applied to the [redacted] *register in* [redacted] *operations.*

5

In Verilog, there are four options for a bit to be. 0, 1, X and Z.
In brief, what does each one mean?

6

What type of circuits do you associate the use of
i) blocking statements, and
ii) non-blocking statements
in Verilog code?

7

Abstraction: hiding the complexity of the design.

1

The datapath realises the data operations required by the FSM.

2

The control issues signals to control the operation of the datapath.

3

Register to Register: Instructions that perform operations on values inside of registers.
Load/Store: The only operations that will be on memory.
Branch: Operations that change the value of the PC depending on a certain condition.

4

Shifter operations are applied to the srcA register in type 1 operations.

5

1 and 0 are True and False respectively.
A value of X is unknown logic.
A value of Z would be high impedance.

6

Blocking statements use =, and are associated with combinatorial logic and execute one at a time.
Non-blocking statements use <=, and are associated with sequential systems that use a clock and actions are executed concurrently.

7