: hiding the complexity of the design.

1

The realises the data operations required by the FSM.

2

The issues signals to control the operation of the datapath.

3

A Reduced Instruction Set Computer (RISC) has three instruction types. What are they, and in brief what do they do? ***Hint: Stump is a RISC computer***

4

You use bit to determine whether an instruction is Type 1 or 2.

5

Shifter operations are applied to the register in type operations.

6

In Verilog, there are four options for a bit to be. 0, 1, X and Z.
In brief, what does each one mean?

7

What type of circuits do you associate the use of
i) blocking statements, and
ii) non-blocking statements
in Verilog code?

8

The datapath realises the data operations required by the FSM.

2

Abstraction: hiding the complexity of the design.

1

Register to Register: Instructions that perform operations on values inside of registers.
Load/Store: The only operations that will be on memory.
Branch: Operations that change the value of the PC depending on a certain condition.

4

The control issues signals to control the operation of the datapath.

3

Shifter operations are applied to the srcA register in type 1 operations.

6

You use bit 12 to determine whether an instruction is Type 1 or 2.

5

Blocking statements use =, and are associated with combinatorial logic and execute one at a time.
Non-blocking statements use <=, and are associated with sequential systems that use a clock and actions are executed concurrently.

8

1 and 0 are True and False respectively.
A value of X is unknown logic.
A value of Z would be high impedance.

7

Do you have to use the default case in Verilog? When would you use it?

9

*What is the difference between a Verilog **task** and a Verilog **function**?*

10

*Where would you locate a **task** or **function** in your Verilog code?*

11

Why does Stump's R0 exist? Give some examples illustrating its use.

12

What is a load/store architecture?

13

How would you setup a Stump FSM with the inputs clk, rst, a 16 bit ir and a 2 bit register for state?

14

*How would you design a **clock** for a verilog test?*

15

How would you instantiate a Stump_FSM with the inputs clk, rst, an ir and a state for testing?

16

A task can change any number of outputs whereas a function can update only one.

10

Not necessarily. It is useful to cover cases not listed in the case statement, trapping any invalid states you shouldn't be in.

9

Allows you to enable further operations to be implemented that are not part of the ISA.

- *MOV: ADD R3, R2, R0*
- *NOP: ADD R0, R0, R0*
- *CMP: SUBS R0, R3, R4*

12

It needs to be within the module but outside any always/initial blocks.

11

```
module Stump_FSM (input wire clk,
        input wire rst,
        input wire [15:0] ir,
        output reg [ 1:0] state);
endmodule
```

Stump FSM

14

Data within registers will only be operated on, with results being written back to registers. LD/ST operations will be included for memory operations.

13

```
Stump_FSM variableName (
    .clk(var1), .rst(var2), .ir(var3), .state(var4)
);
```

Instantiated Stump_FSM

16

```
always
    begin
        #100 // Time per clock change
        clock = !clock
    end
```

Clock example

15

In Stump, name the four ***flags*** *and, when* ***'S'*** *is appended to an instruction, how they go high.*

17

The extends immediate values in Stump for Type 2 and Type 3 instructions.

18

The in stump performs shift operations on the srcA register on Type 1 instructions.

19

What are the differences between the ***Von Neuman*** *architecture and the* ***Harvard*** *architecture?*

20

Compare and contrast the ***ARM*** *ISA's and the* ***x86*** *ISA's techniques for branching to a subroutine.*

21

(ISA) is the visible view of the processor (what is exposed to the programmer).

22

is the hardware view on a processor.

23

Name some ways that a processor can be made faster.

24

The Sign Extender extends immediate values in Stump for Type 2 and Type 3 instructions.

18

N *- the negative flag is set if the ALU result is negative.*
Z *- the zero flag is set if the result is zero.*
V *- the overflow is set if the result from an addition/subtraction interpreted as a two's complement is wrong.*
C *- the carry flag is set if there is a carry out from the most significant bit of the result (bit 15).*

Flags

17

Von Neuman
- has one bus for both data transfers and instructions fetches.
- a single, unified cache, which stores both instructions and data.
Harvard
- has separate data and instruction busses, allowing transfers to be performed simultaneously on both busses.
- separate caches for each bus, as a shared cache would be difficult to manage.

Von Neuman *v.s.* ***Harvard***

20

The Shifter in stump performs shift operations on the srcA register on Type 1 instructions.

19

Instruction Set Architecture (ISA) is the visible view of the processor (what is exposed to the programmer).

22

ARM
- Single register allows for less implementation cost.
- Any other branch call will overwrite value in link register.
x86
- Stack based system has greater implementation cost.
- Allows for branch calls within branches, without loss of address.

ARM ISA vs x86 ISA

21

Increase the clock rate
- As a consequence of Moore's Law
- Through circuit design
- Through microarchitectural design, e.g. more parallelism
Do more in each cycle
- Parallelism within instruction execution
Do more in each instruction
- Somewhat limited by ISA as a completely new ISA is expensive.

Some possible ways of making a processor faster

24

Microarchitecture is the hardware view on a processor.

23

What are the basic principles of ***pipelining****?*

25

prevent one operation from overrunning its predecessor (by delaying it).

26

How does pipelining effect latency?

27

What is the potential speed up of pipelining? Why isn't this always the case?

28

A (DSP) is specialised for high performance in a particular subset of computing tasks.

29

What is saturating arithmetic?

30

(SIMD) describes computers with multiple processing elements that perform the same operation on multiple data points simultaneously.

31

What are the two basic types of ***MOS-FETs*** *(Metal-Oxide-Semiconductor Field Effect Transistors)?*

32

Latches prevent one operation from overrunning its predecessor (by delaying it).

26

*Pipelining works by starting executing one instruction before its predecessor(s) have finished. The time taken for a circuit to evaluate is a bit uncertain, so instructions are deliberately separated into **stages** with pipeline **latches**.*

25

Partitioning a task into N stages gives a maximum speed-up of N times.
This assumes that all stages take exactly the same time and that the partitioning has some added cost due to the delay imposed by the pipeline registers.

28

It increases latency, with the speed being limited by the slowest stage.

27

In two's complement arithmetic, adding two large positive numbers may result in an overflow. A Digital Signal Processor (DSP) may sometimes find it better to "clip" the value to the maximum representable one. This is called "saturation".

30

A Digital Signal Processor (DSP) is specialised for high performance in a particular subset of computing tasks.

29

***NMOS** - with n-type channel (analogy to normally open switch)*
***PMOS** - with p-type channel (analogy to normally closed switch)*

Two types of MOS-FETs

32

Single instruction, multiple data (SIMD) describes computers with multiple processing elements that perform the same operation on multiple data points simultaneously.

31

How do you calculate system performance?

33

When changing a functional design into a physical one, what is on the "wish list" of properties?

34

*What does **PVT** stand for in the context of chip design?*

35

$$timepertask = \\ clockperiod \times numberofclockcyclespertask \\ performance \approx 1/(timepertask)$$

- Clock period (performance)
- Floorplan/pinout
- Area/density (cost)
Using all the chip area for useful gates, but keeping the chip small to save cost.
- Power

Wish list of properties

*- Manufacturing **P**rocess variation*
*- Varying operating **V**oltage*
Typical voltage ranges my be $\pm 10\%$
*- Different chip **T**emperature*

Typically, run simulation at extremes