What does a fully associative cache store?

1

How does the CPU locate an item in a fully associative cache?

2

What is temporal locality?

3

What is spatial locality?

4

What are the three common cache replacement algorithms?

5

Explain the write-through cache write strategy.

6

Explain the copy-back cache write strategy.

7

Why does a direct mapped cache usually use static RAM?

8

Addresses and their corresponding data

1

Hardware compares the input address with all stored addresses (in parallel)
If we get a match we have a hit
If no match we must go to main memory

2

The principle that if you use an address once, you may use it again soon e.g. loops

3

The principle that if you use an address once, you are also likely to use addresses nearby e.g. arrays

4

Least Recently Used (LRU)
Round Robin
Random

5

Whenever a write is done to the cache, the write is also done to main memory

6

When a cache line is replaced, if the dirty bit is set, the modified value is written to main memory

7

It is a lot faster than dynamic RAM

8

How many transistors do DRAM and SRAM use per bit?

9

Briefly explain what a set associative cache consists of.

10

What is the advantage of using a set associative cache?

11

What two control bits are usually used in cache entries?

12

Explain what a compulsory cache miss is?

13

Explain what a capacity cache miss is?

14

Explain what a conflict cache miss is?

15

A number of directly mapped caches operating in parallel

10

1 and 6.

9

Valid bit and dirty bit

12

We have more flexible cache replacement strategies as we could choose any one of the caches to replace from

11

Since the cache is limited in size, we cant contain all of the pages for a program, so if an address is evicted from the cache to make more space, but is then requested after, then it will be a capacity miss.

14

When we first start the computer, the cache is empty, so until the cache is populated, we're going to have a lot of misses (or whenever the cache hasn't seen an address before).

13

In a direct mapped or set associative cache, there is competition between memory locations for places in the cache. If the cache was fully associative, then misses due to this wouldnt occur.

15