



School of Electronics and Communication Engineering

Senior Design Project VII semester

Team members:

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Overview

- Introduction
- Problem statement
- Objectives
- Blocks Involved in 4th Order Modulator
- Demonstration of results
- Conclusion
- References

Introduction

- High-performance analog circuit layout generation is a challenging and time-consuming operation with a significant impact on circuit performance.
- The different parasitics introduced during layout design has the potential to seriously degrade the performance of the circuit.
- The possible precision of circuits is fundamentally constrained by device mismatch and heat effects.
- Since it is impossible to completely eliminate these parasitics, one of the primary goals of analog layout is to manage, forecast, and ensure that the circuit continues to operate according to specifications after designing.

Problem statement

To implement the Physical Design of fully-differential OPAMP, Comparator and DAC and further integrating them to form the 4th-Order Sigma Delta Modulator, and also compare the schematic and Post-Layout Simulation results.

Objectives

The main objective of "Physical Design of Fully-differential Opamp, Comparator and DAC to form a 4th-Order Sigma-Delta Modulator" is to design the layout of the subblocks and integrate them further to form the Fourth-Order Sigma-Delta Modulator.

Blocks Involved in 4th Order Modulator

- Fully Differential Opamp
- Comparator
- Integrator using Transmission Gates
- Digital to Analog Converter
- N-diff Opamp as a Buffer
- P-Diff Opamp
- Current Reference
- Band-Gap Reference

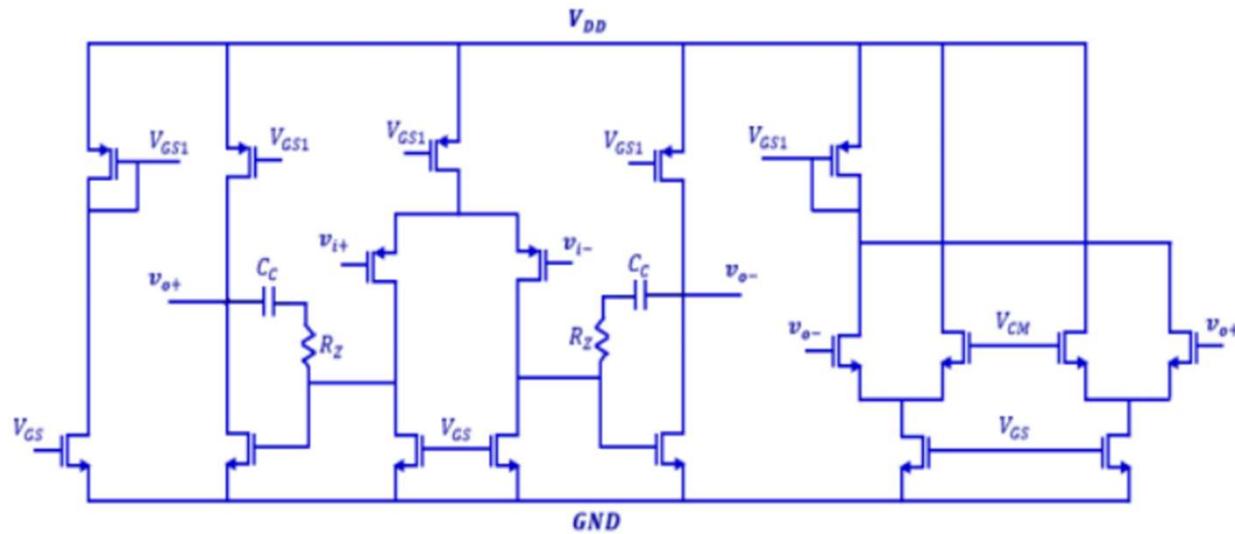
Blocks Involved in 4th Order Modulator

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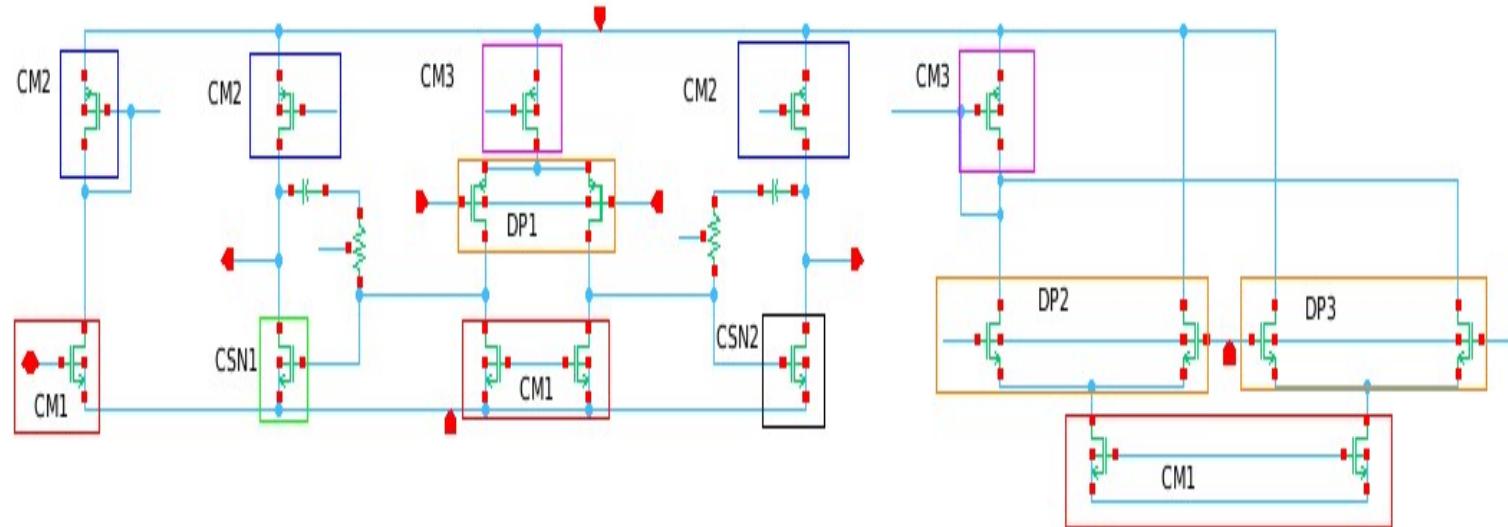
Proposed Methodology/Stages for designing the Layout

- 1.Understanding the Circuit and identifying the transistors to be matched.
- 2.Floor Plan
- 3.Matching
- 4.Guard Ring
- 5.Routing
- 6.Cleaning DRC and LVS Checks
- 7.RC Extraction and Post Layout Simulation
- 8.Integration of all the Subblocks to form a 4th-order Sigma-Delta Modulator

1.Fully-Differential Op-Amp Schematic

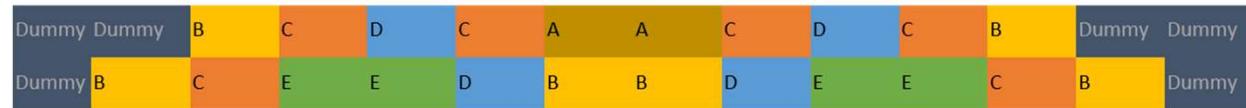


Fully-Differential Op-Amp Matching Pairs Identified

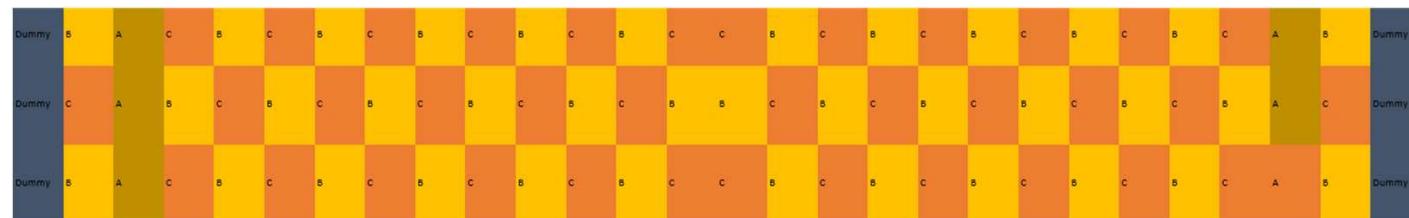


Fully-Differential Op-Amp Matching Pattern

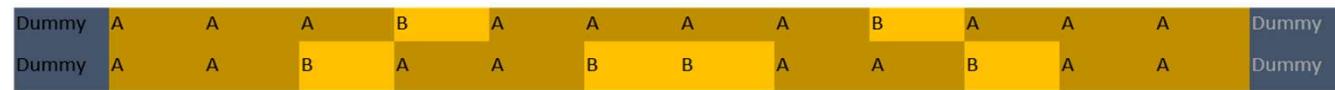
- Current Mirror-1



- Current Mirror-2

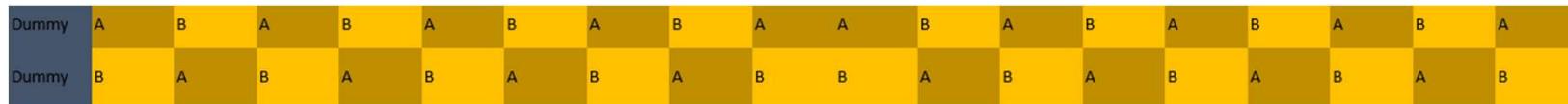


- Current Mirror-3



Fully-Differential Op-Amp Matching Pattern Contd..

- Differential Pair-1



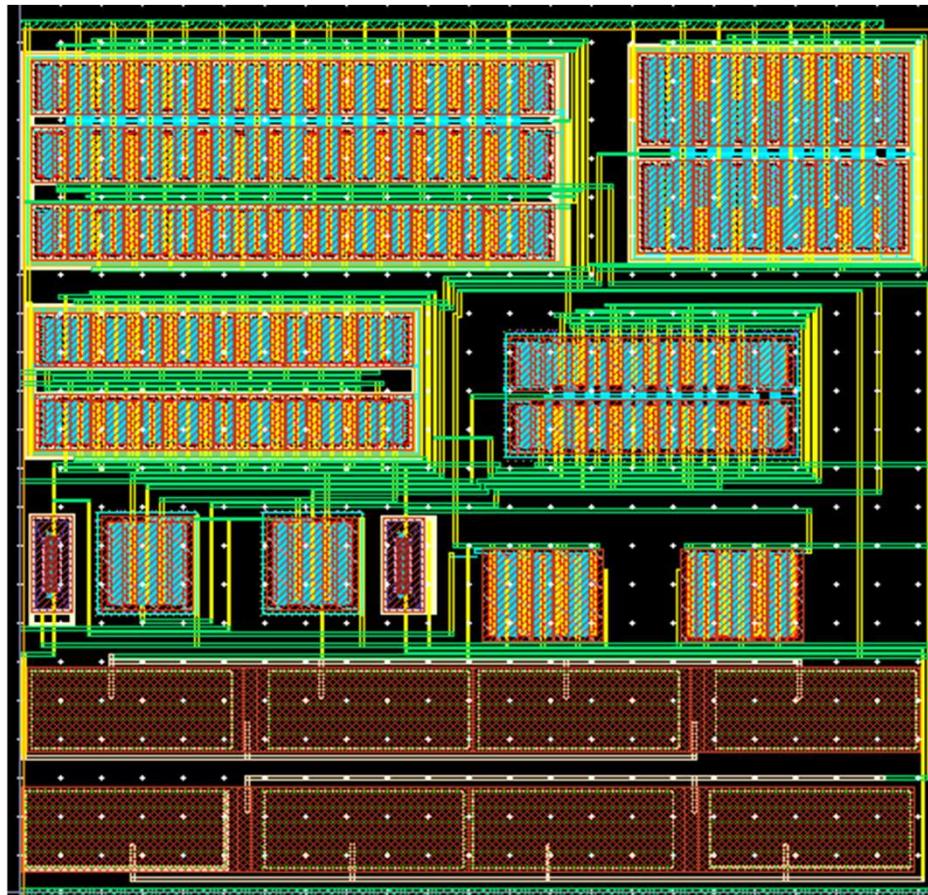
- Differential Pair-2



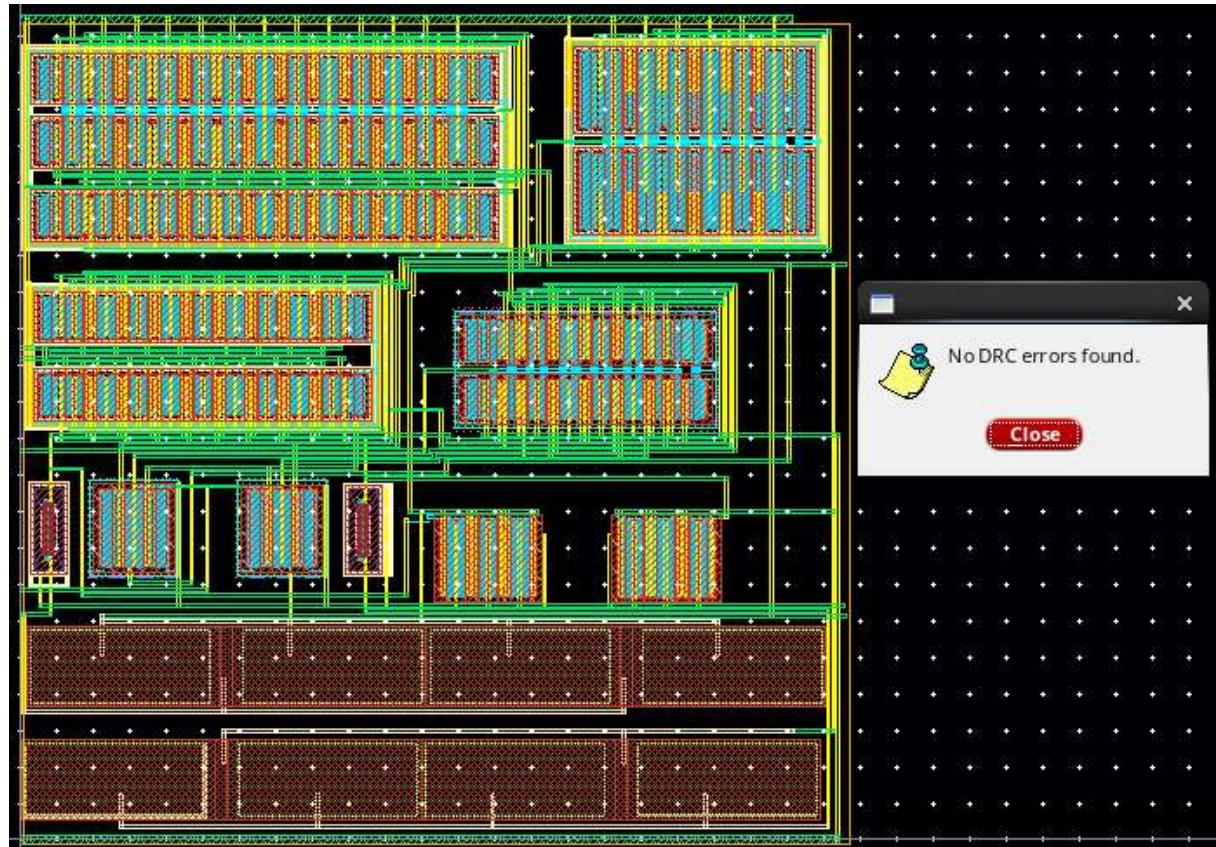
- Differential Pair-3



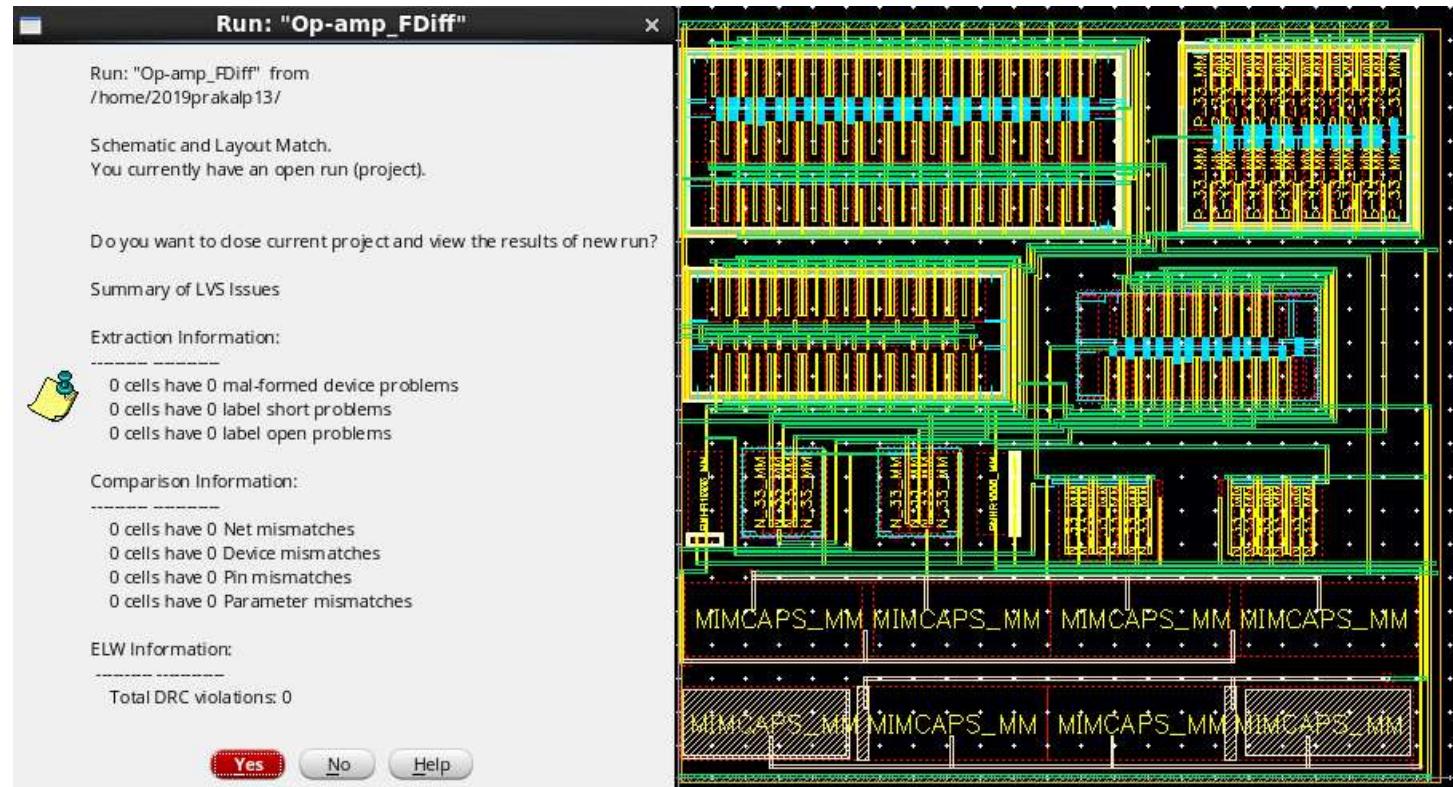
Fully-Differential Op-Amp Layout



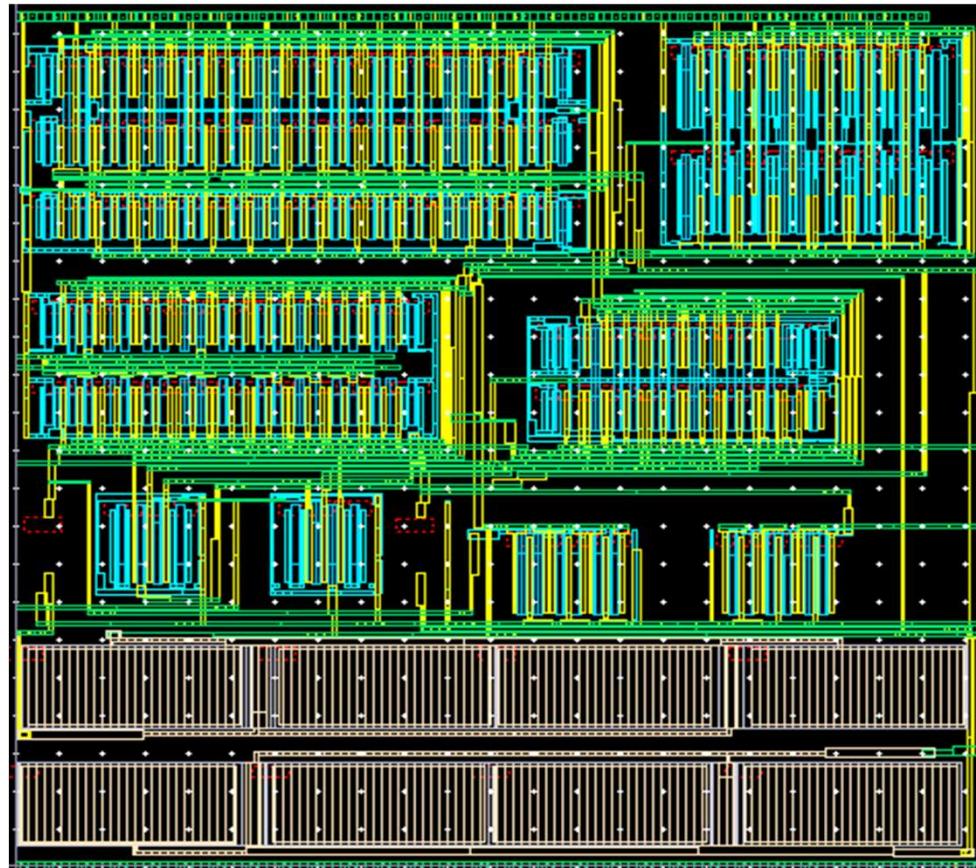
Fully-Differential Op-Amp Layout–DRC Results



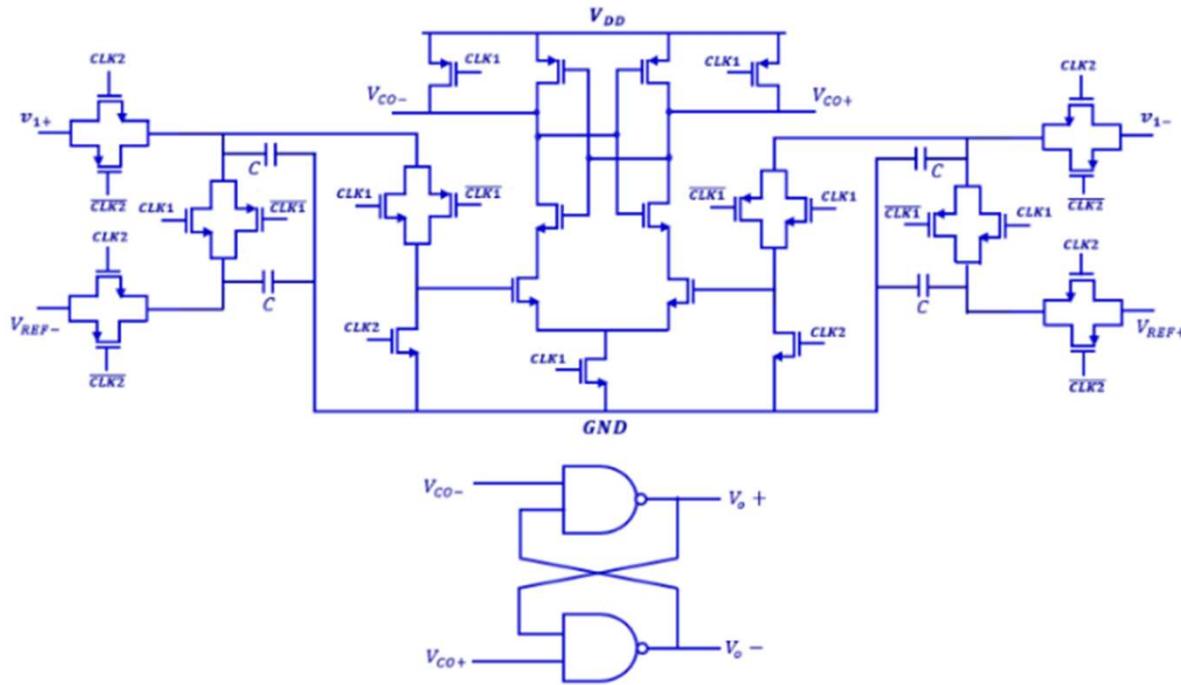
Fully-Differential Op-Amp Layout-LVS Results



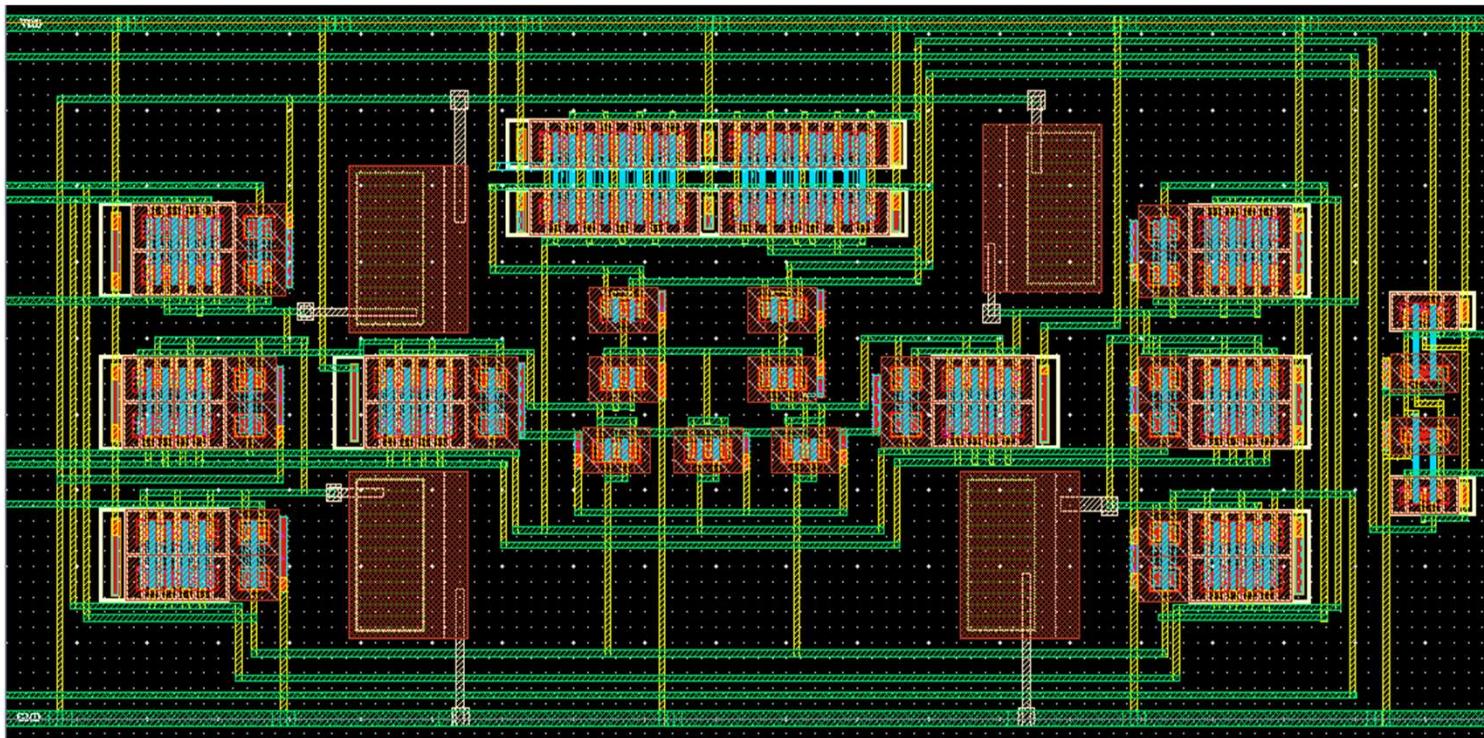
Fully-Differential Op-Amp Layout–RC Extraction Results



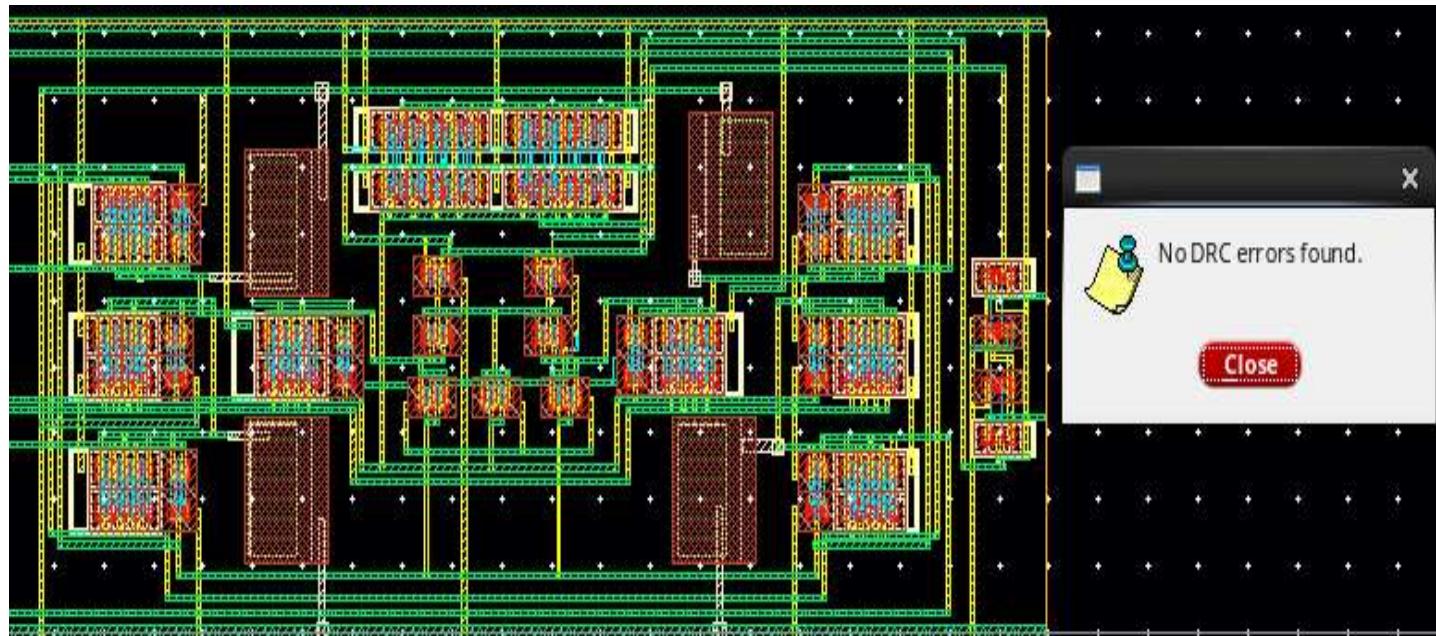
2. Dynamic Comparator Schematic



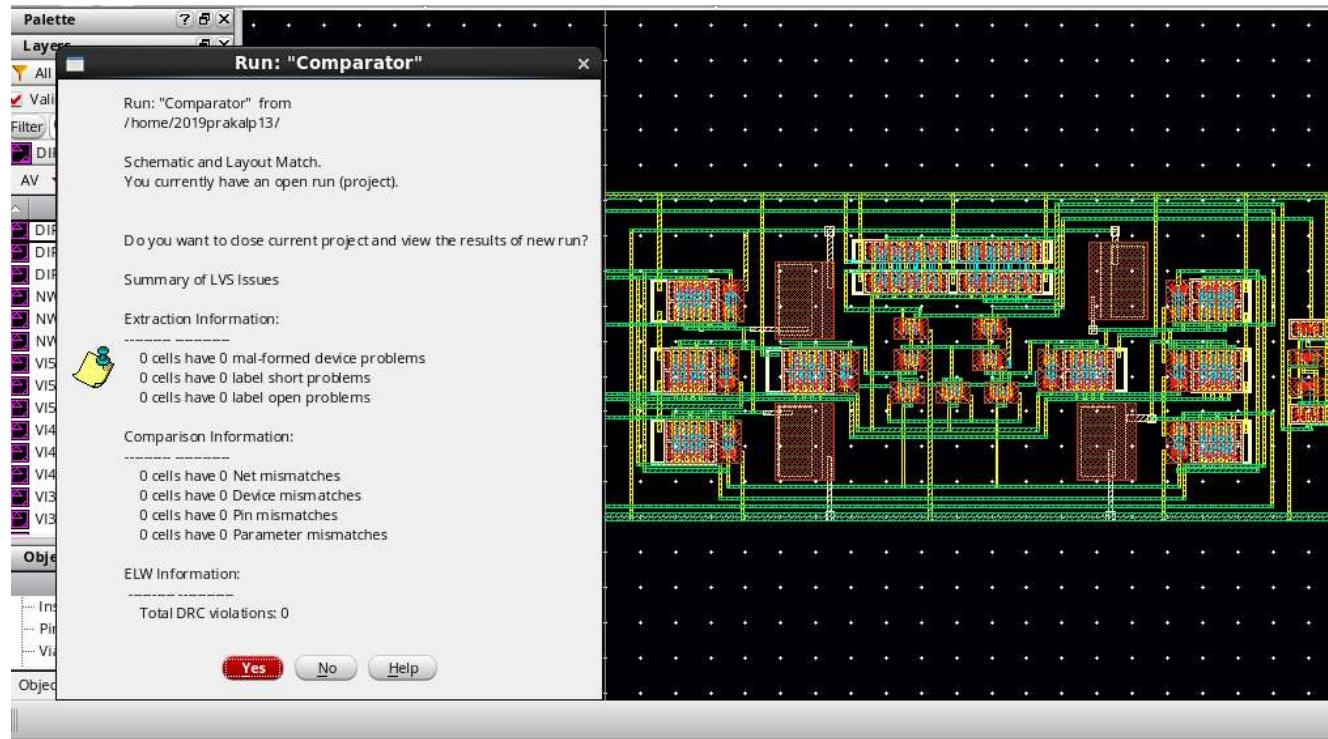
Dynamic Comparator Layout



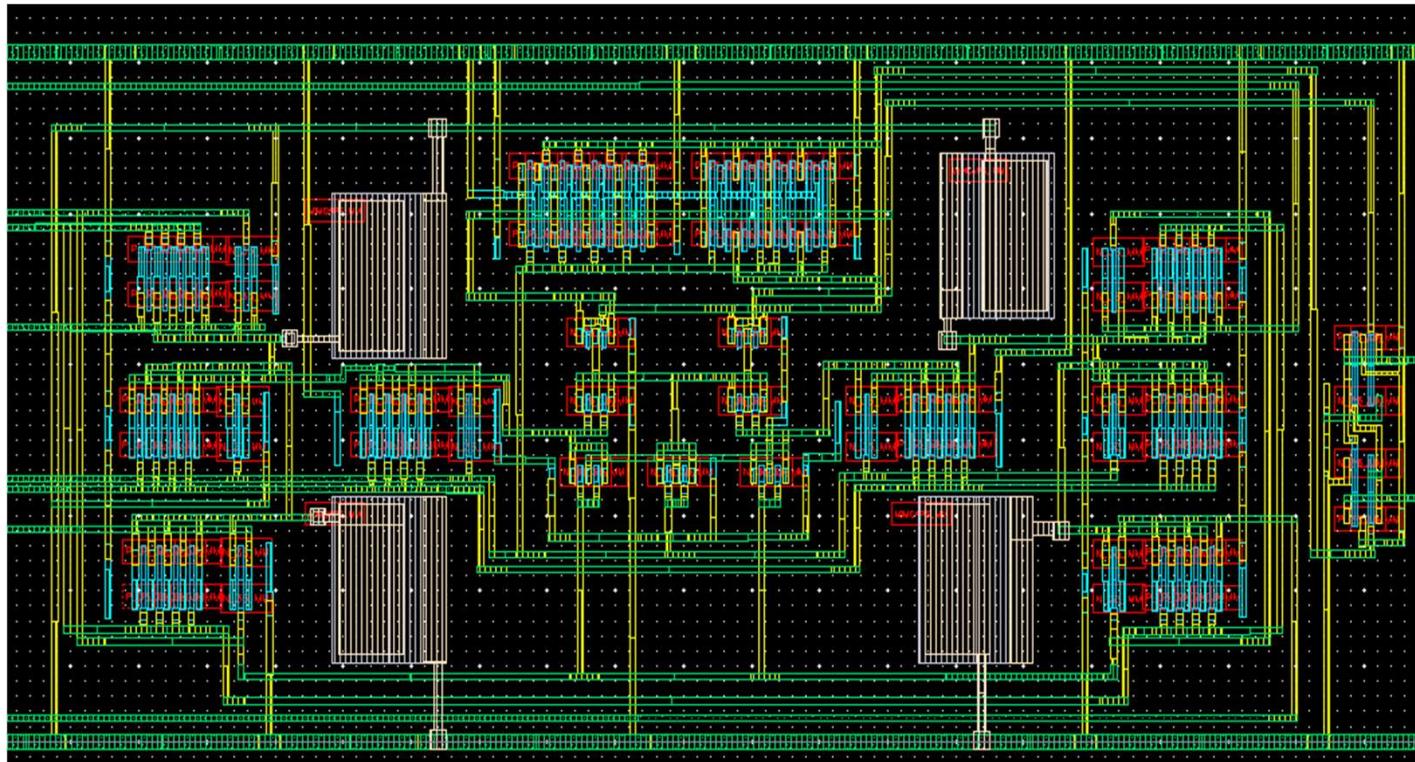
Dynamic Comparator Layout-DRC Results



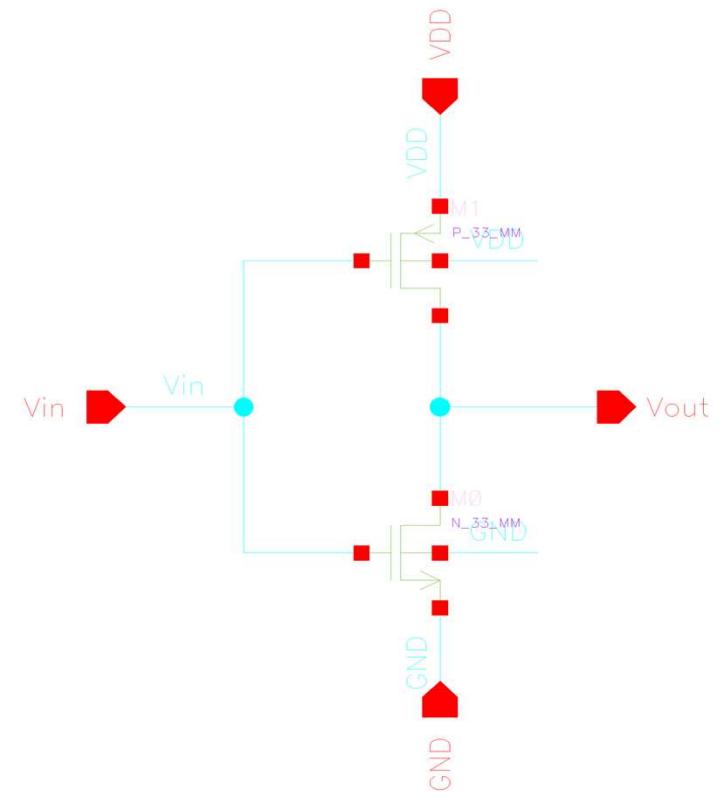
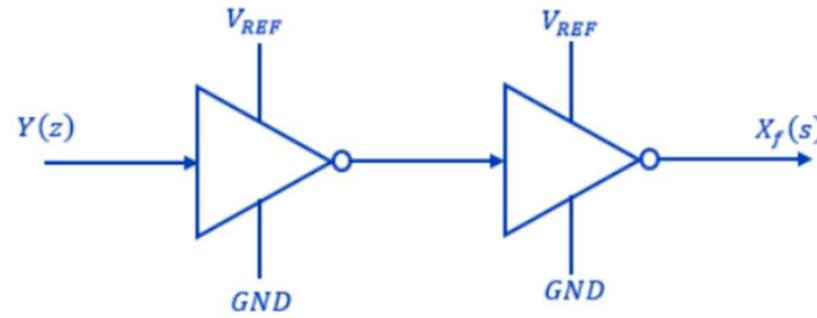
Dynamic Comparator Layout-LVS Results



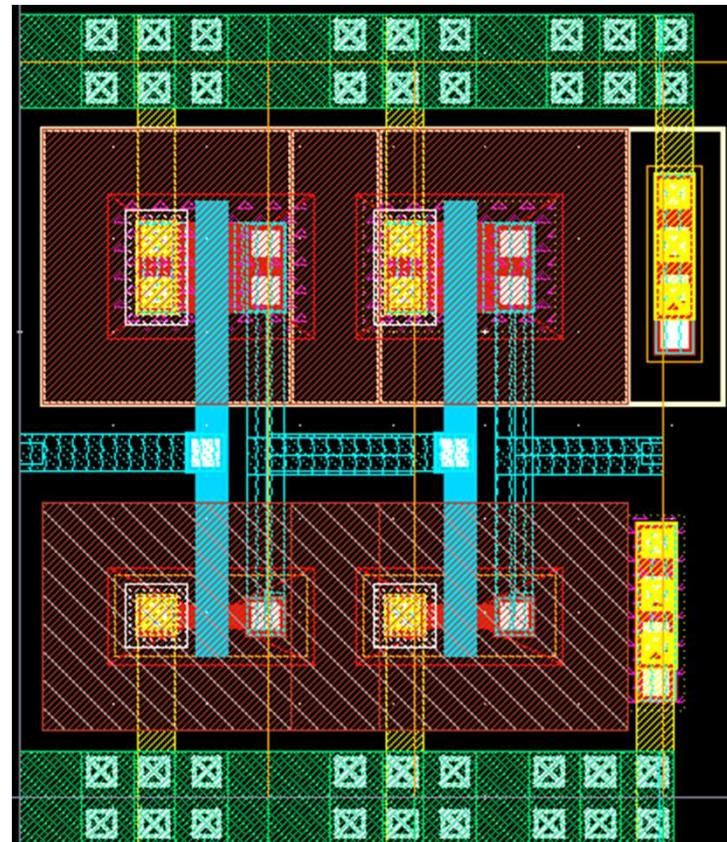
Dynamic Comparator Layout–RC Extraction Results



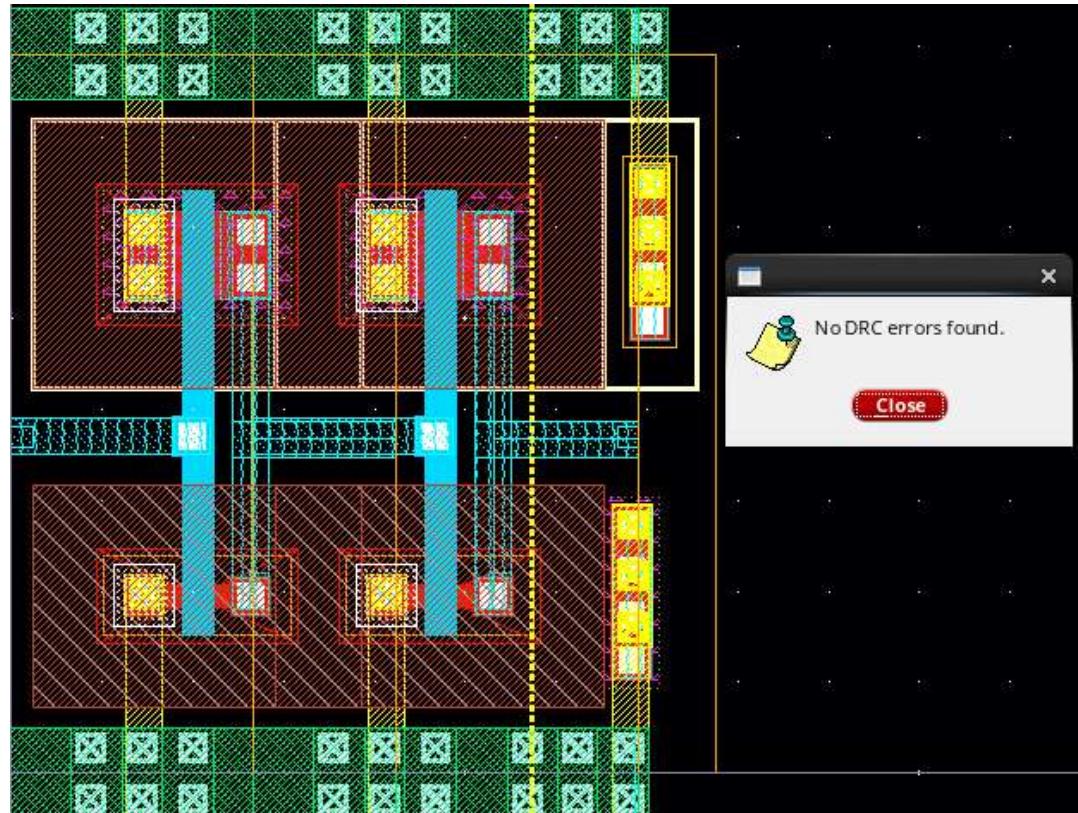
3. DAC Schematic



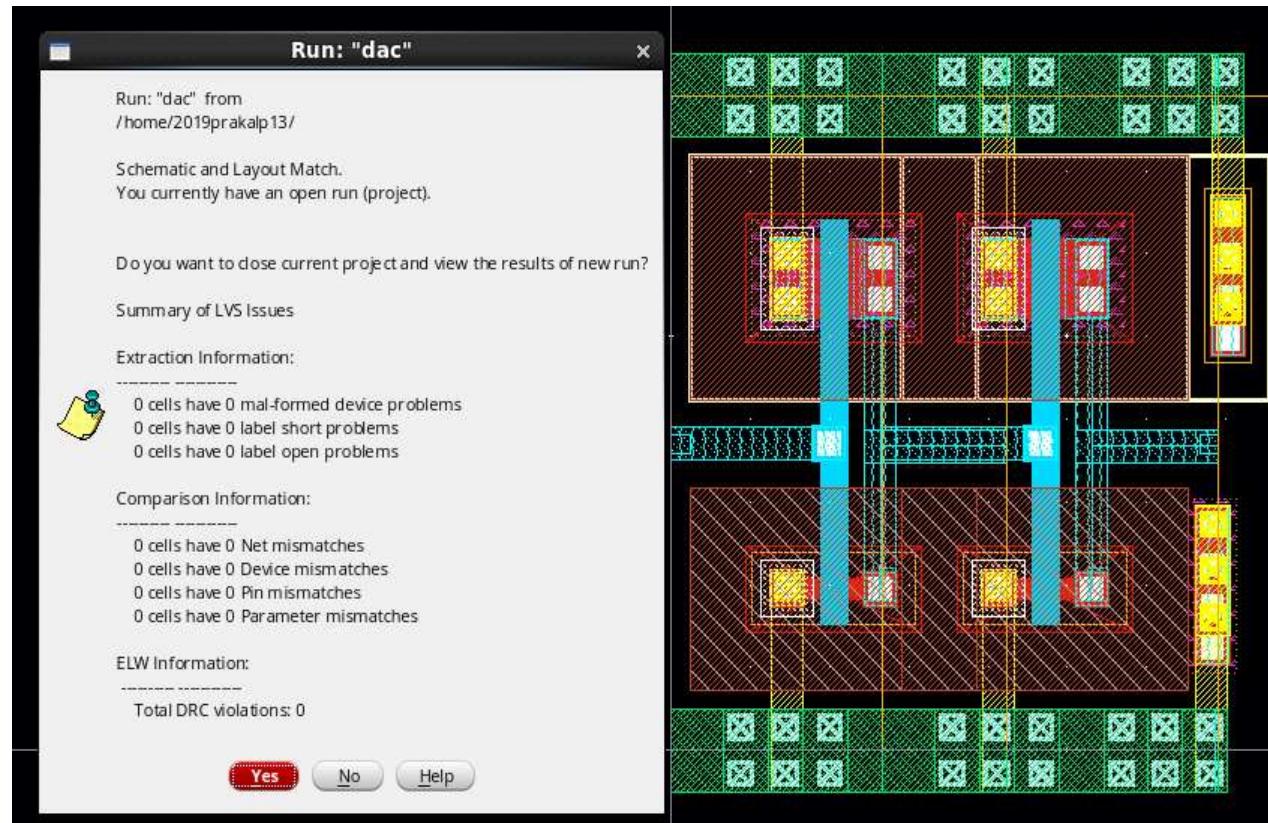
DAC Layout



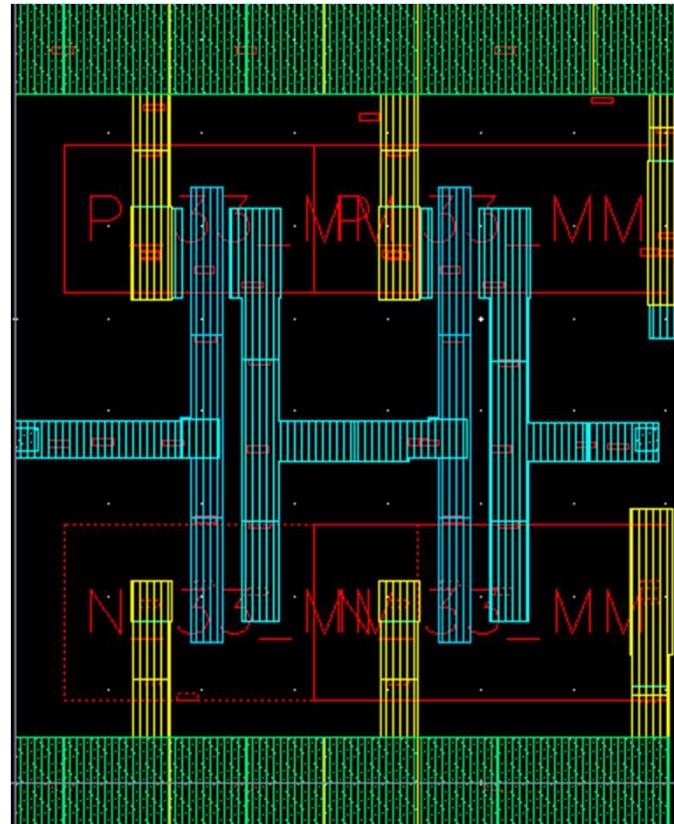
DAC Layout-DRC Results



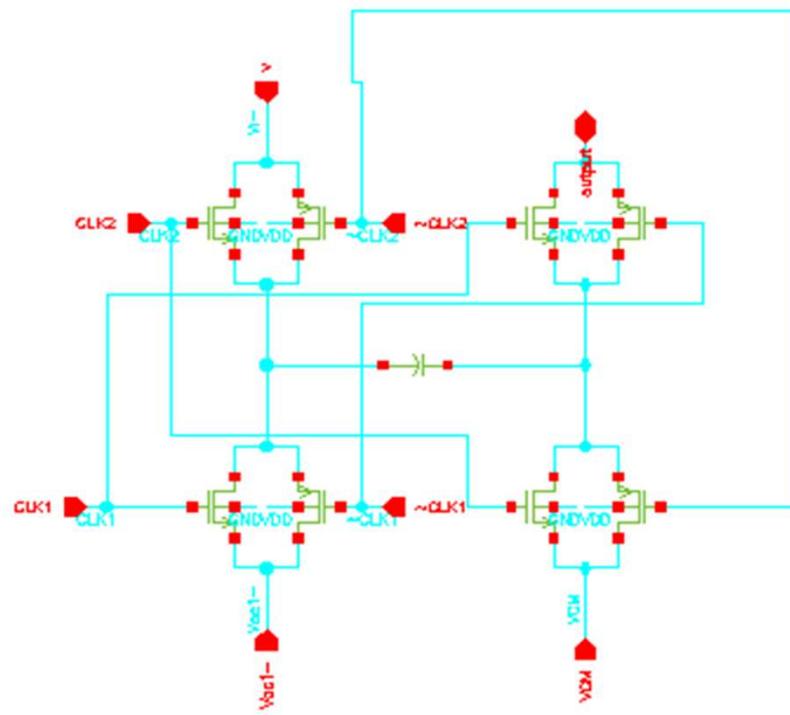
DAC Layout-LVS Results



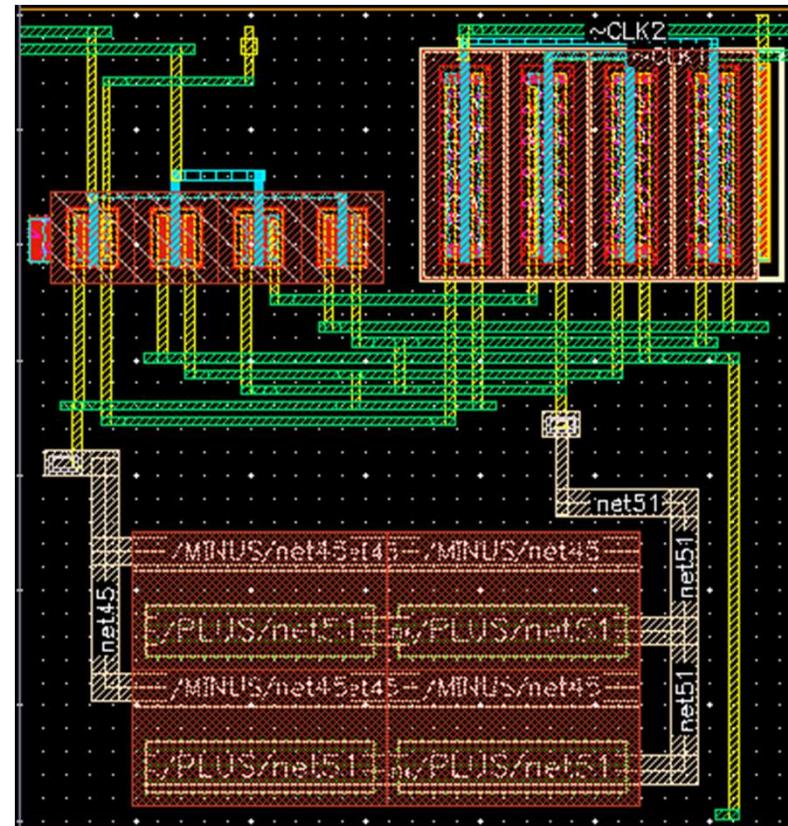
DAC Layout–RC Extraction Results



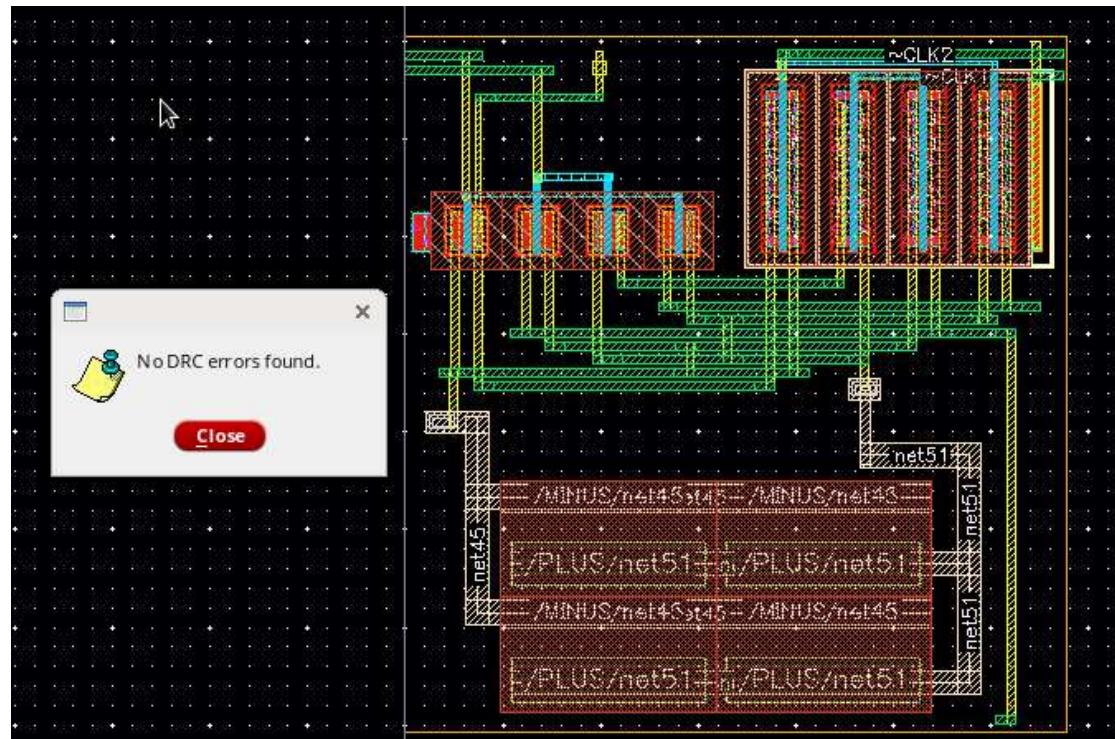
4. Transmission Gates Schematic



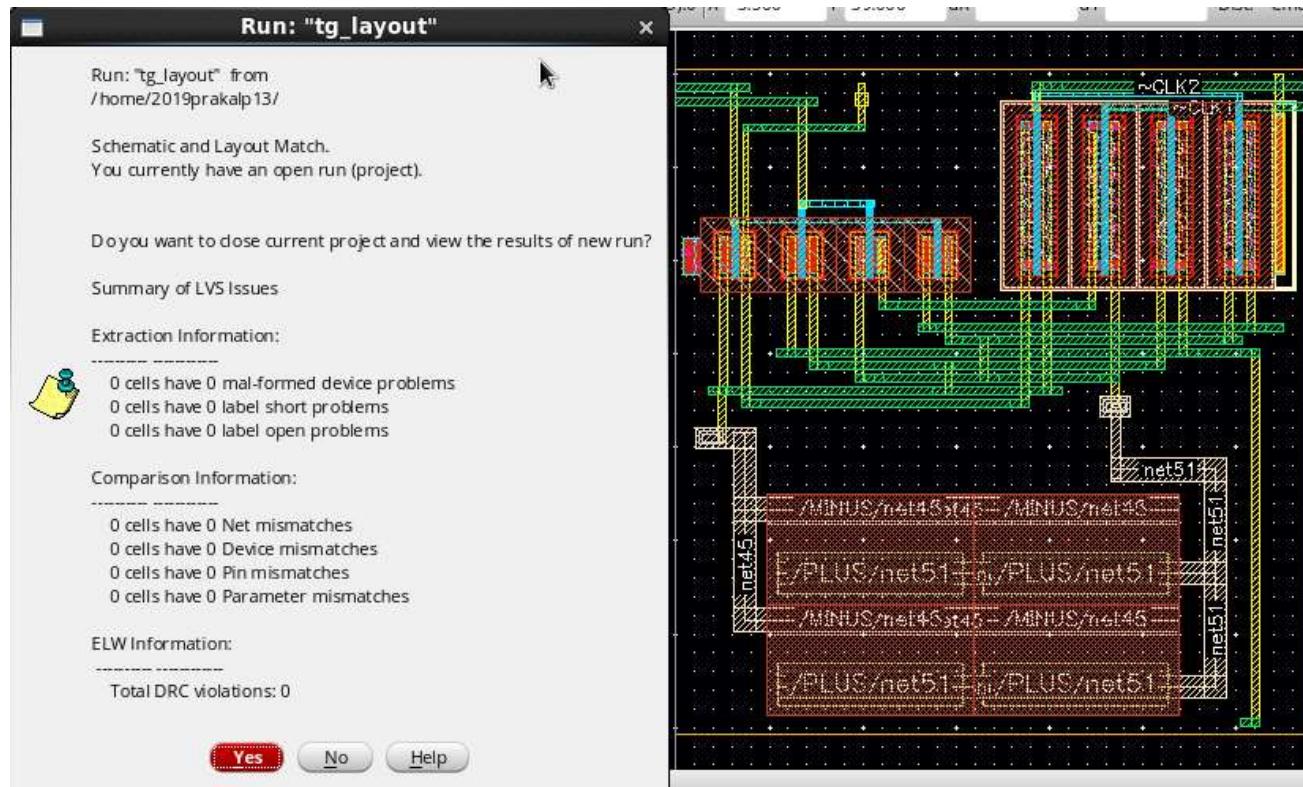
Transmission Gates Layout



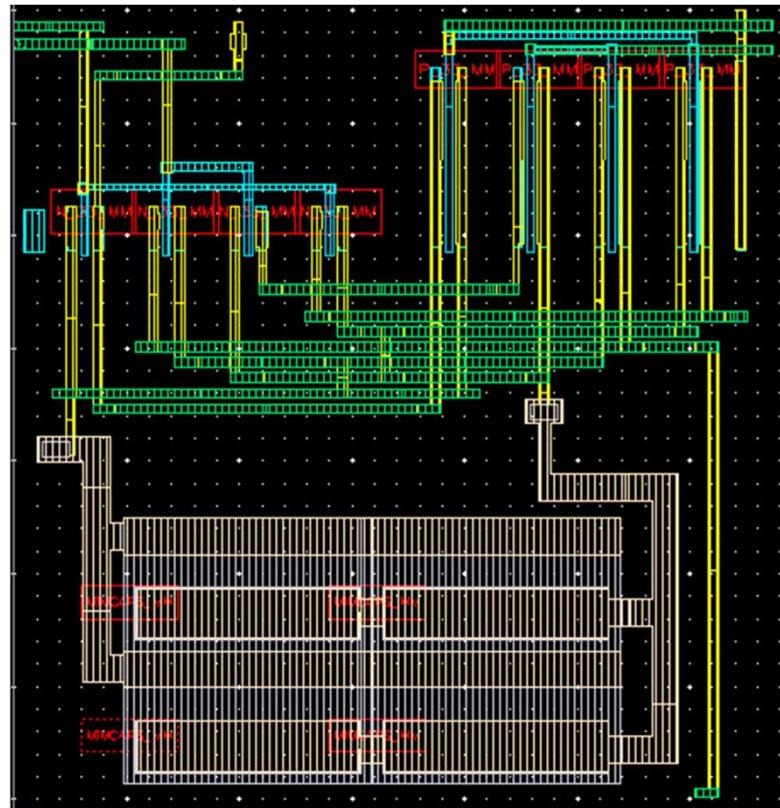
Transmission Gates Layout-DRC Results



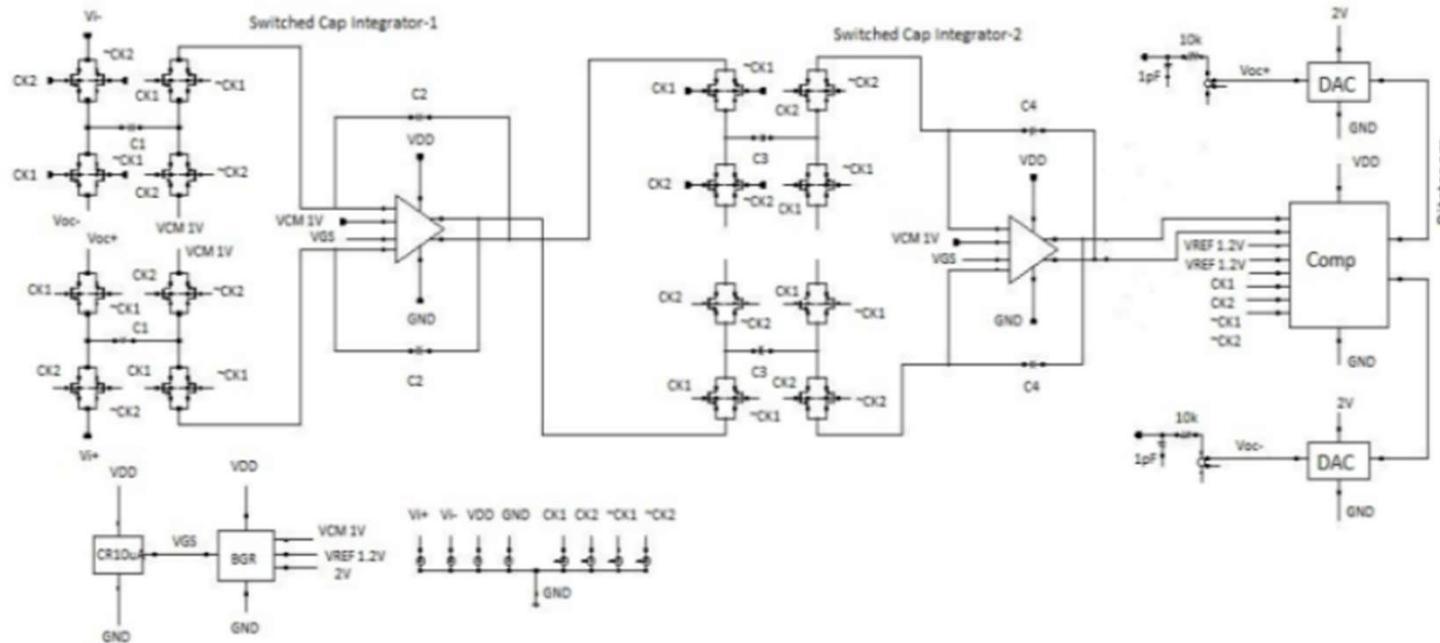
Transmission Gates Layout-LVS Results



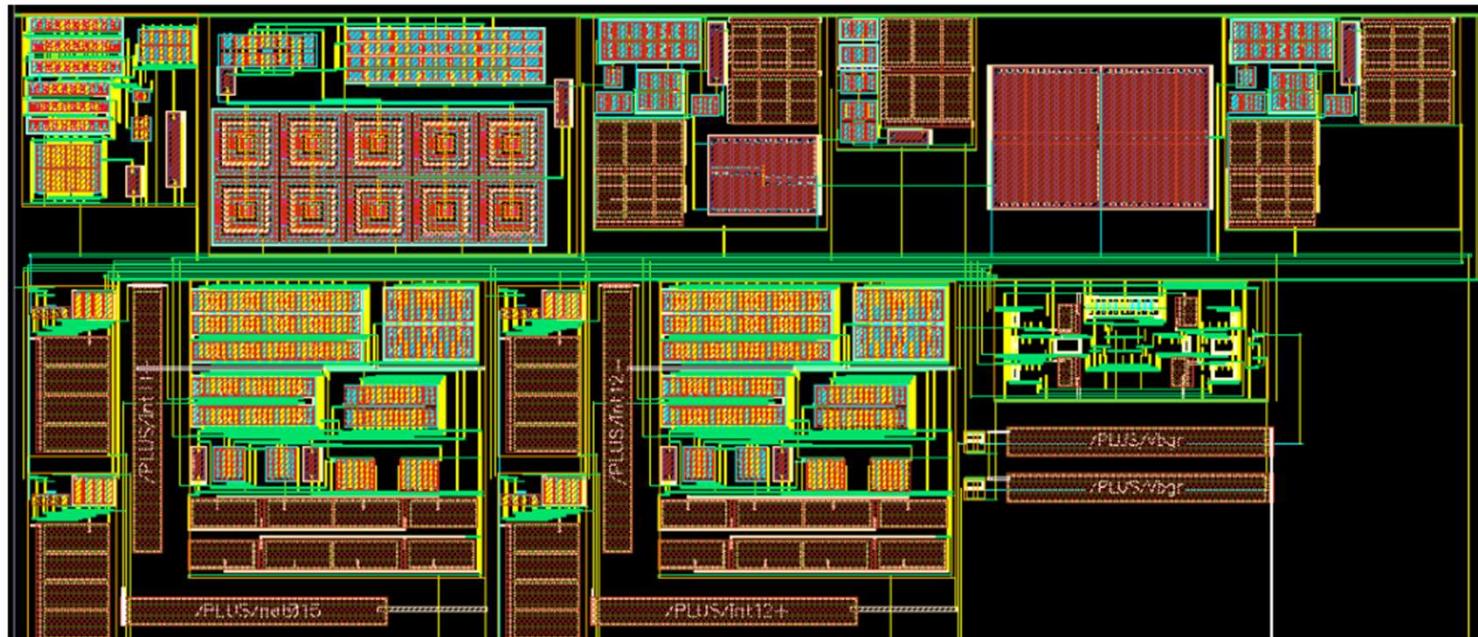
Transmission Gates Layout–RC Extraction Results



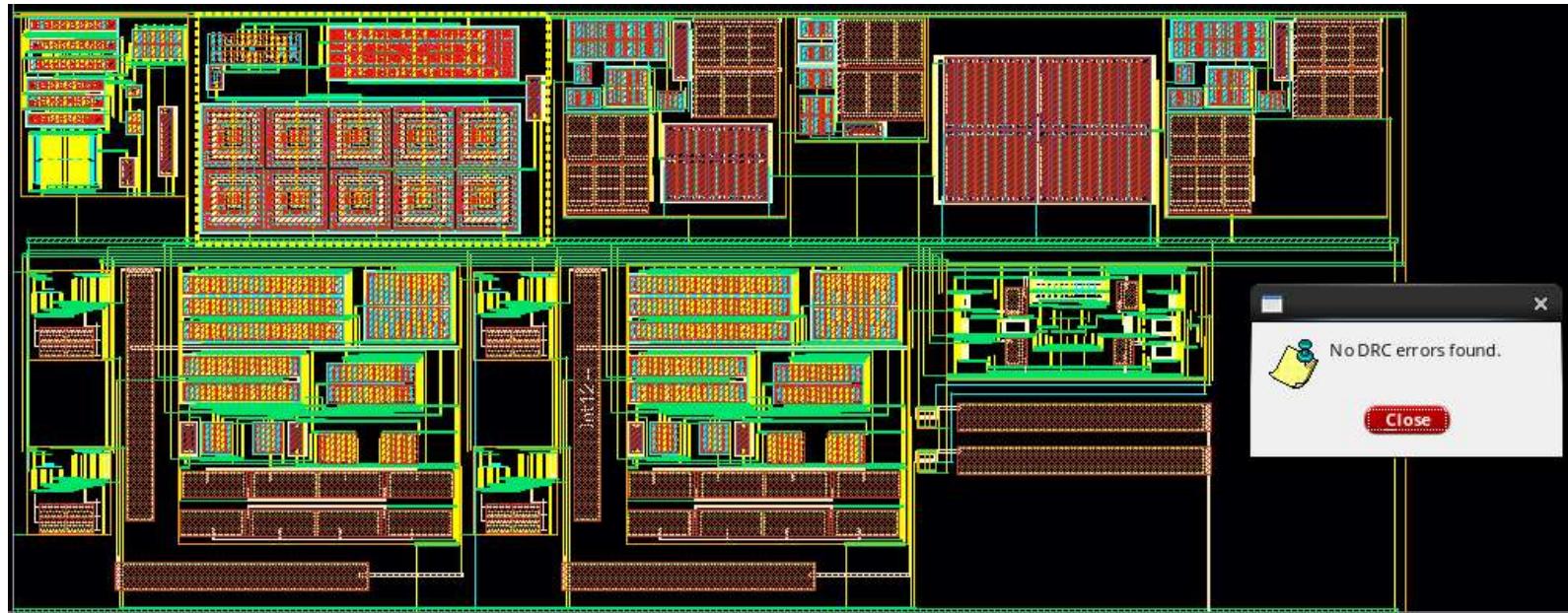
2nd Order Modulator Schematic



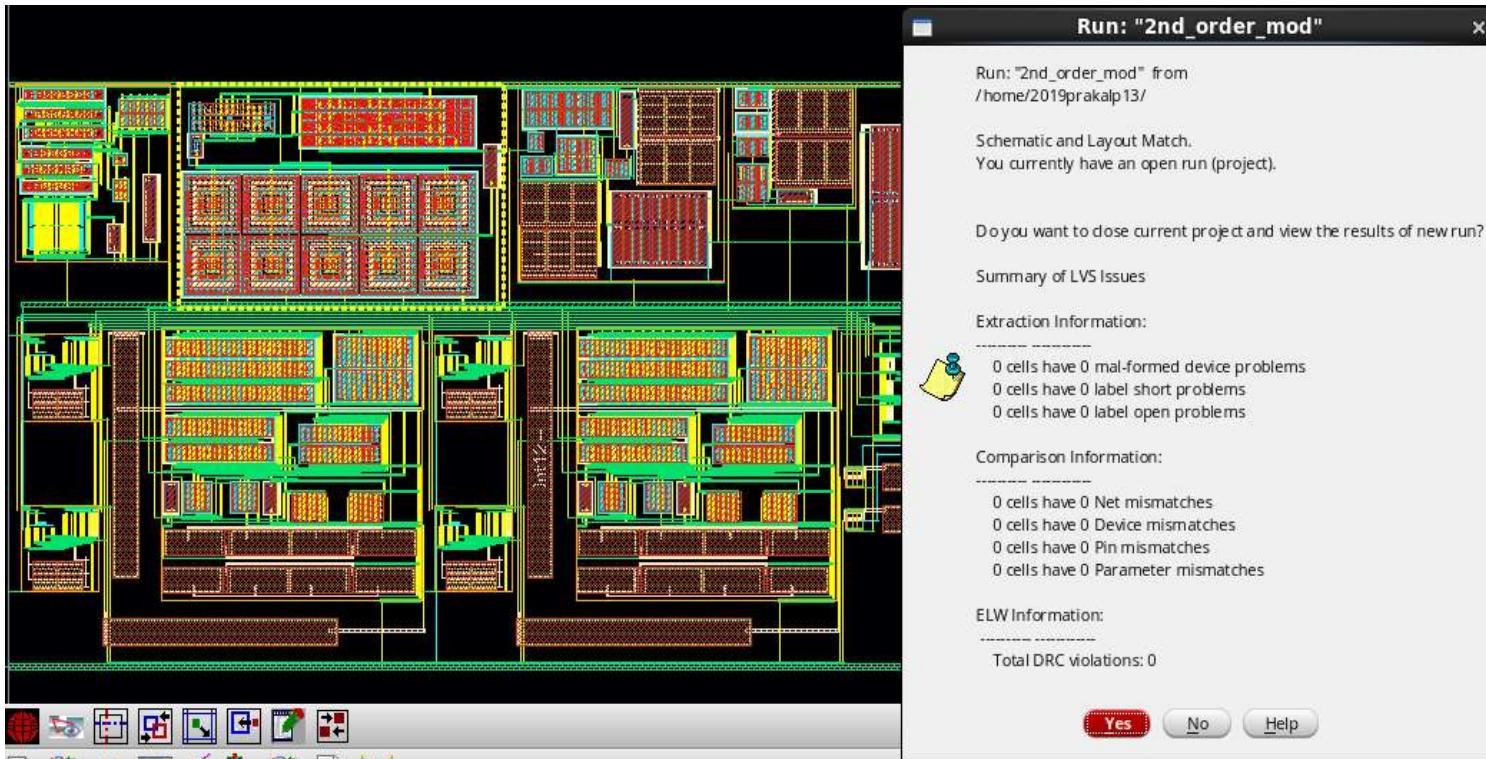
2nd Order Modulator Layout



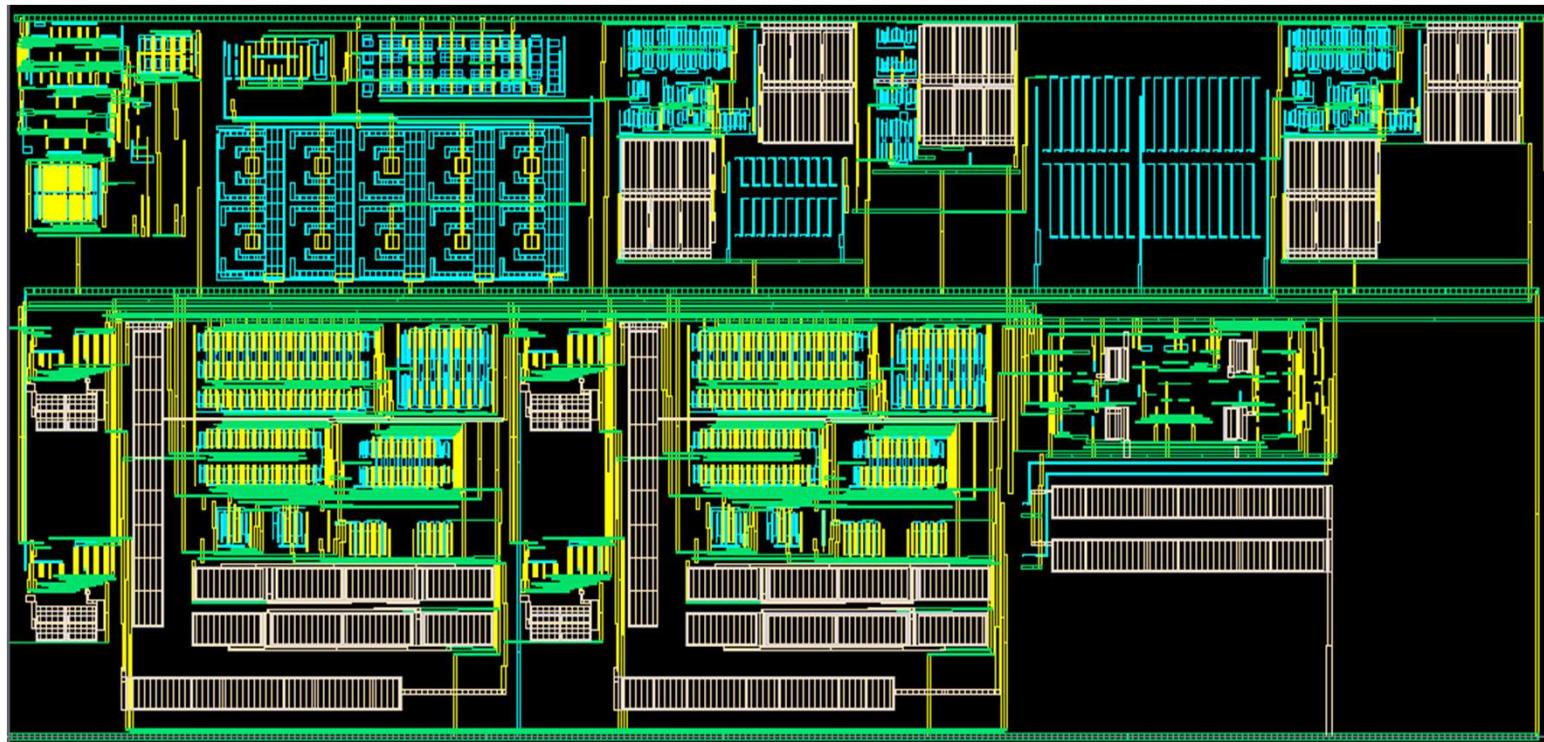
2nd Order Modulator Layout–DRC Results



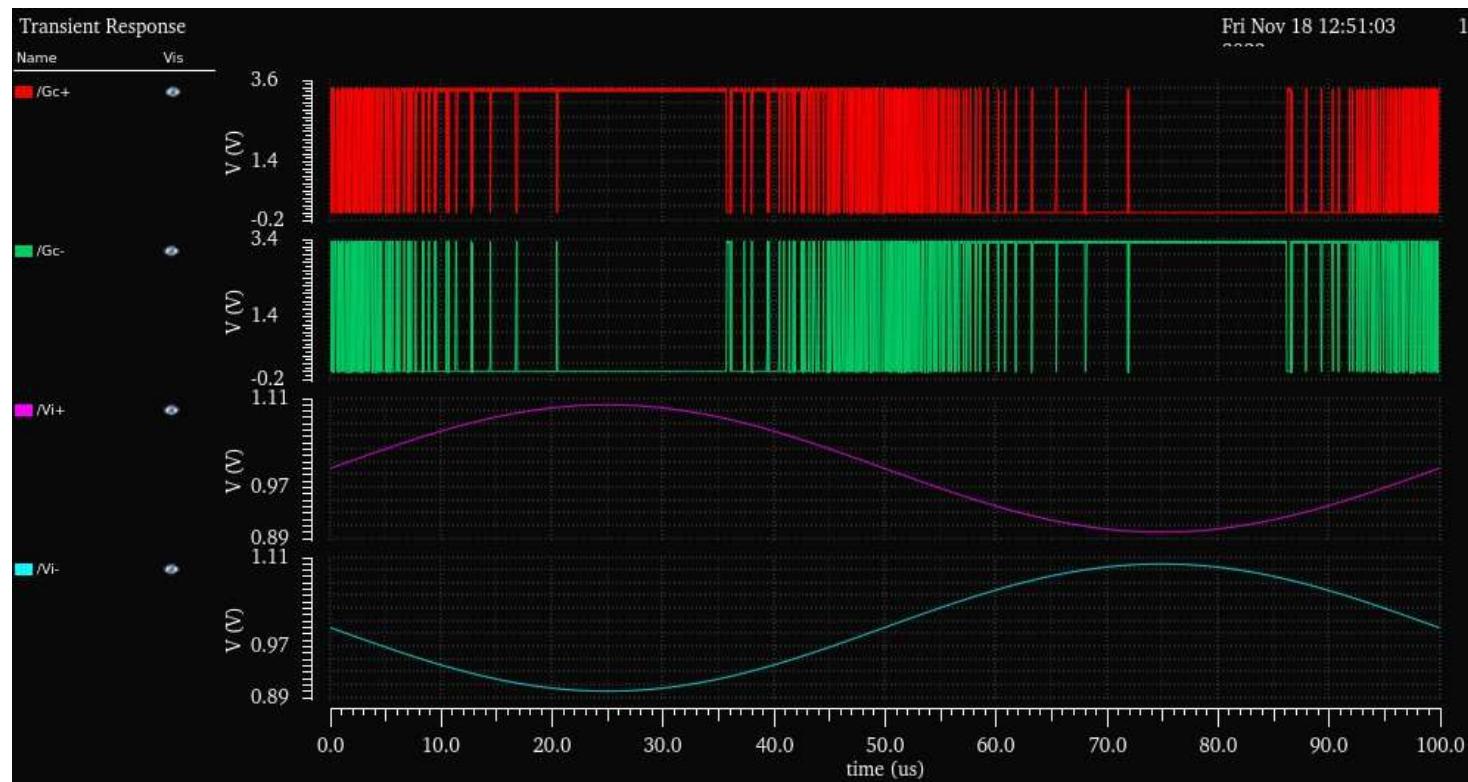
2nd Order Modulator Layout-LVS Results



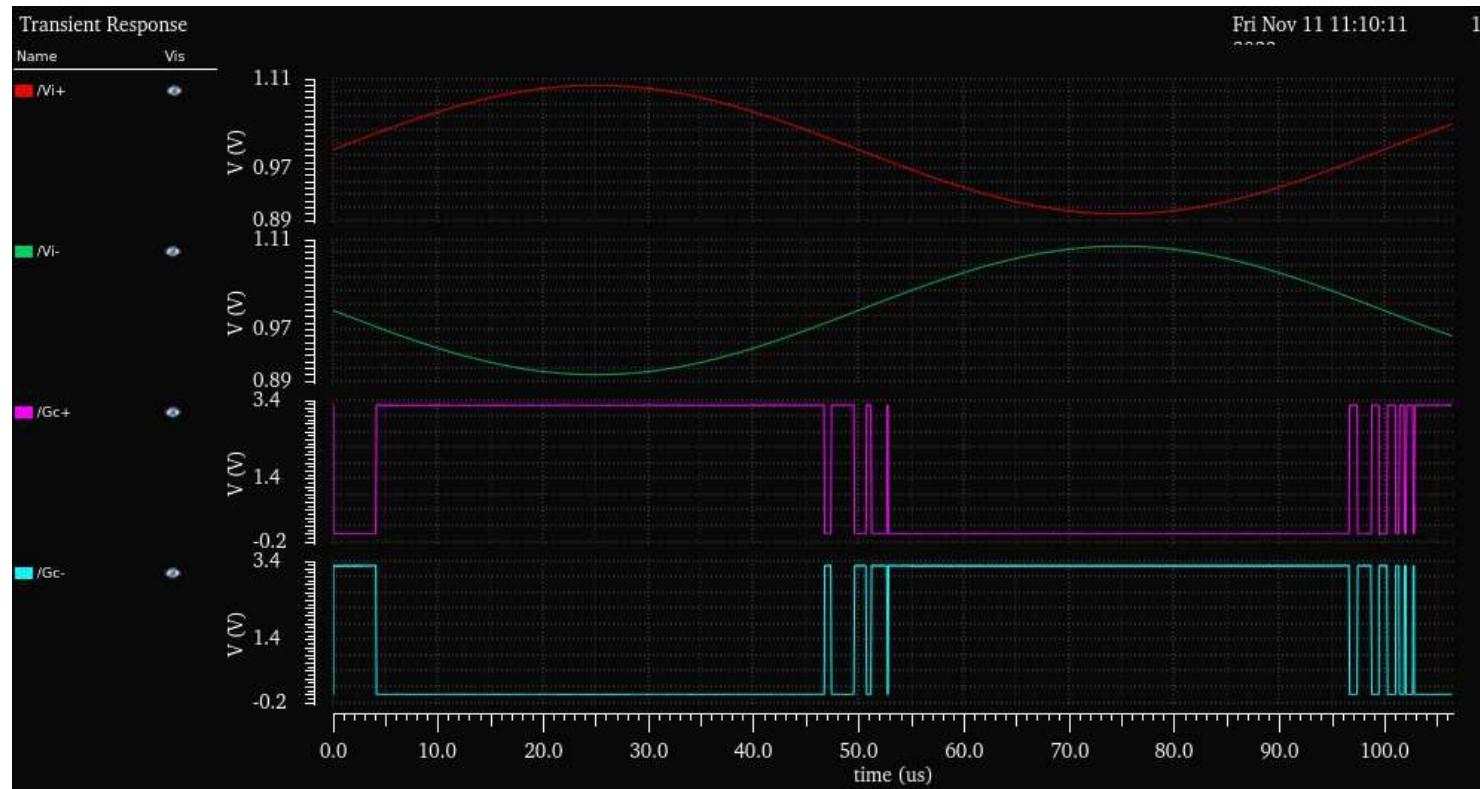
2nd Order Modulator Layout–RC Extraction Results



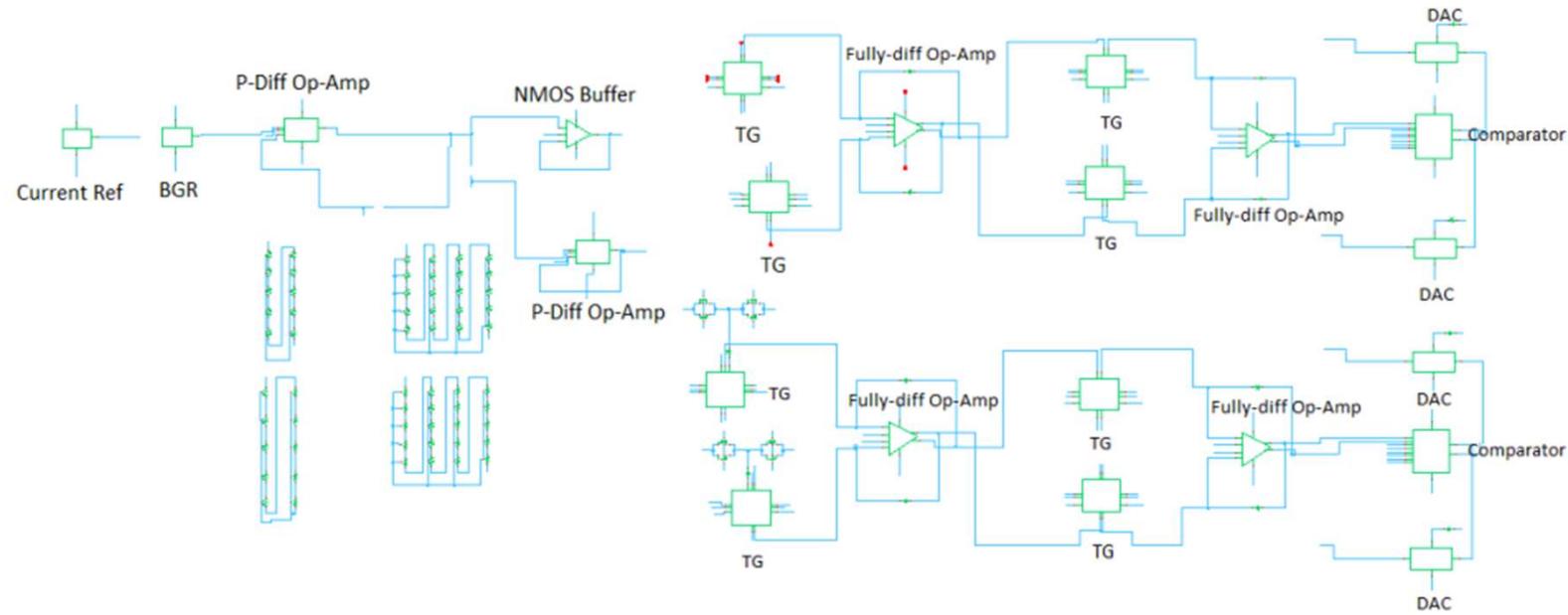
2nd Order Modulator Schematic Results



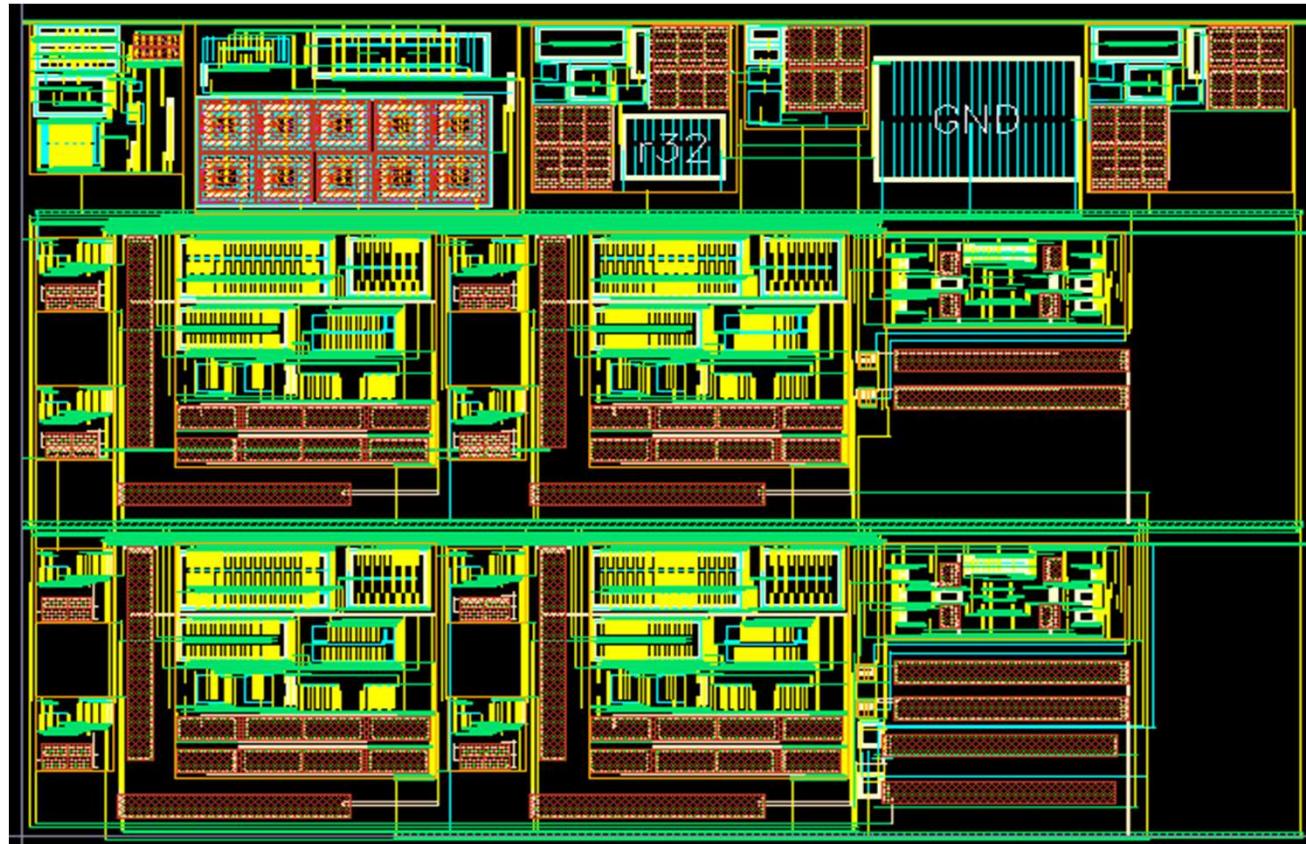
2nd Order Modulator Post–Layout Simulation Results



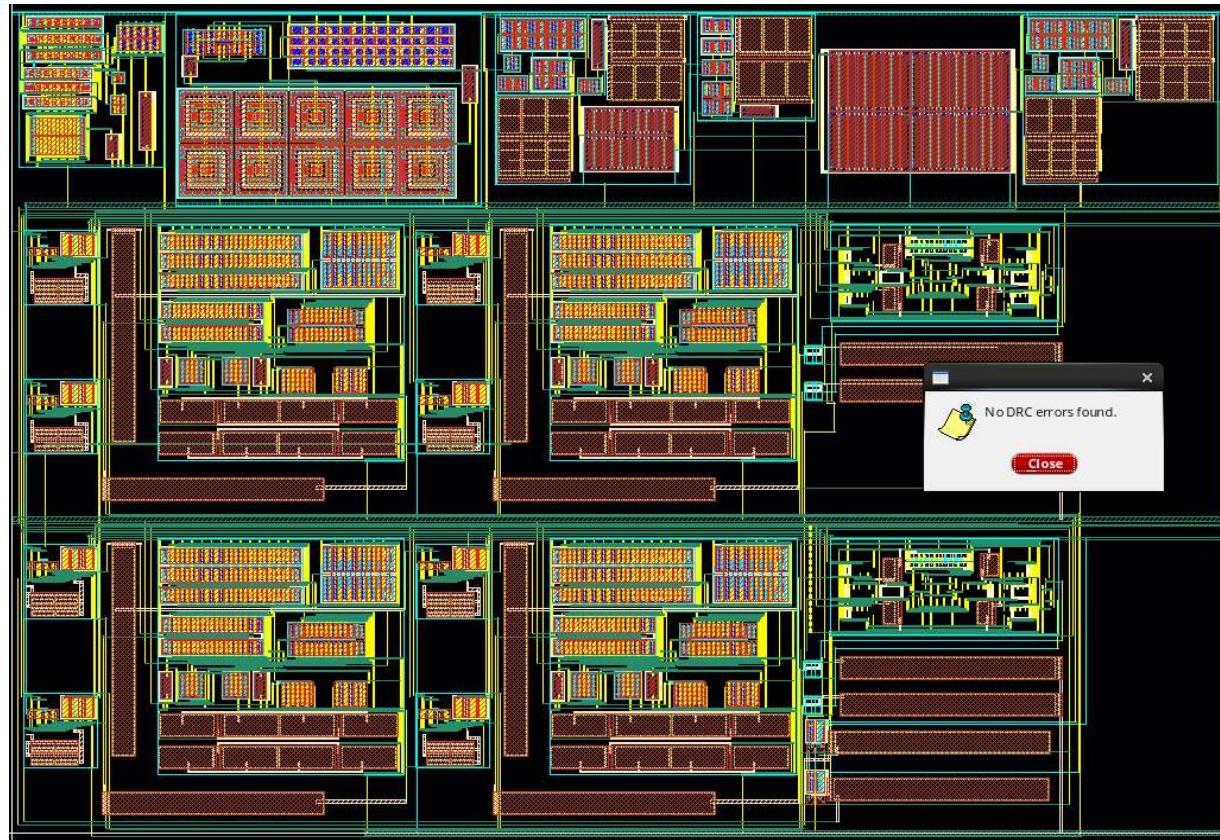
4th Order Modulator Schematic



4th Order Modulator Layout



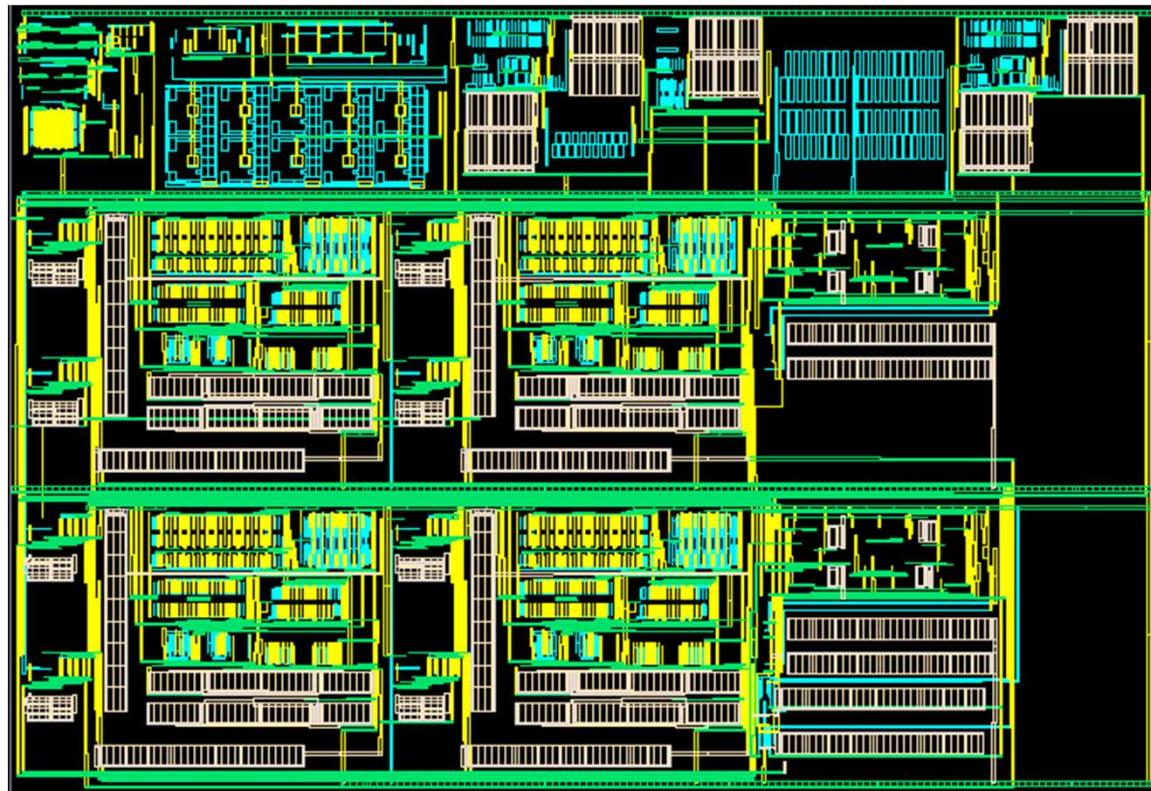
4th Order Modulator Layout-DRC Results



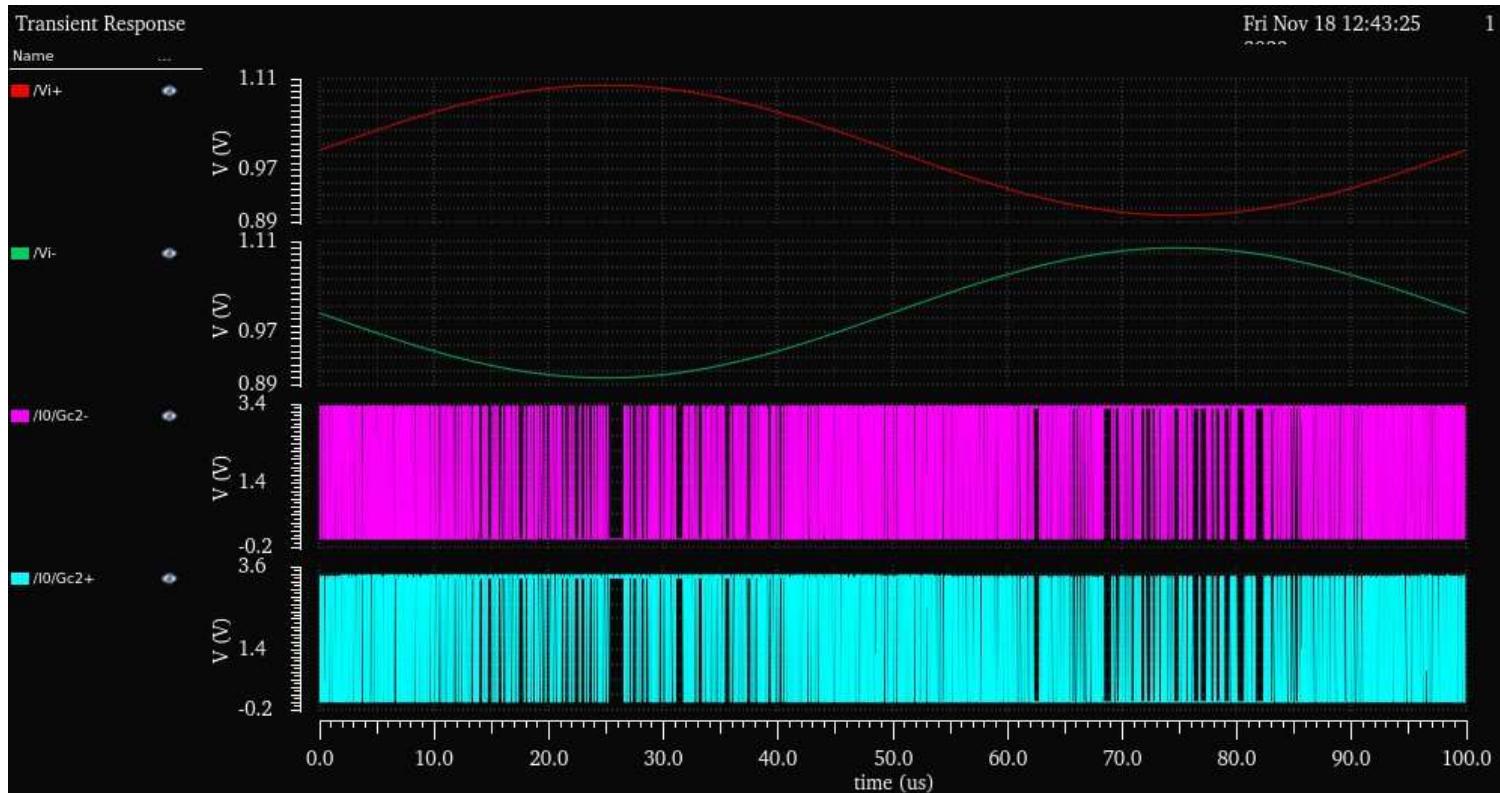
4th Order Modulator Layout-LVS Results



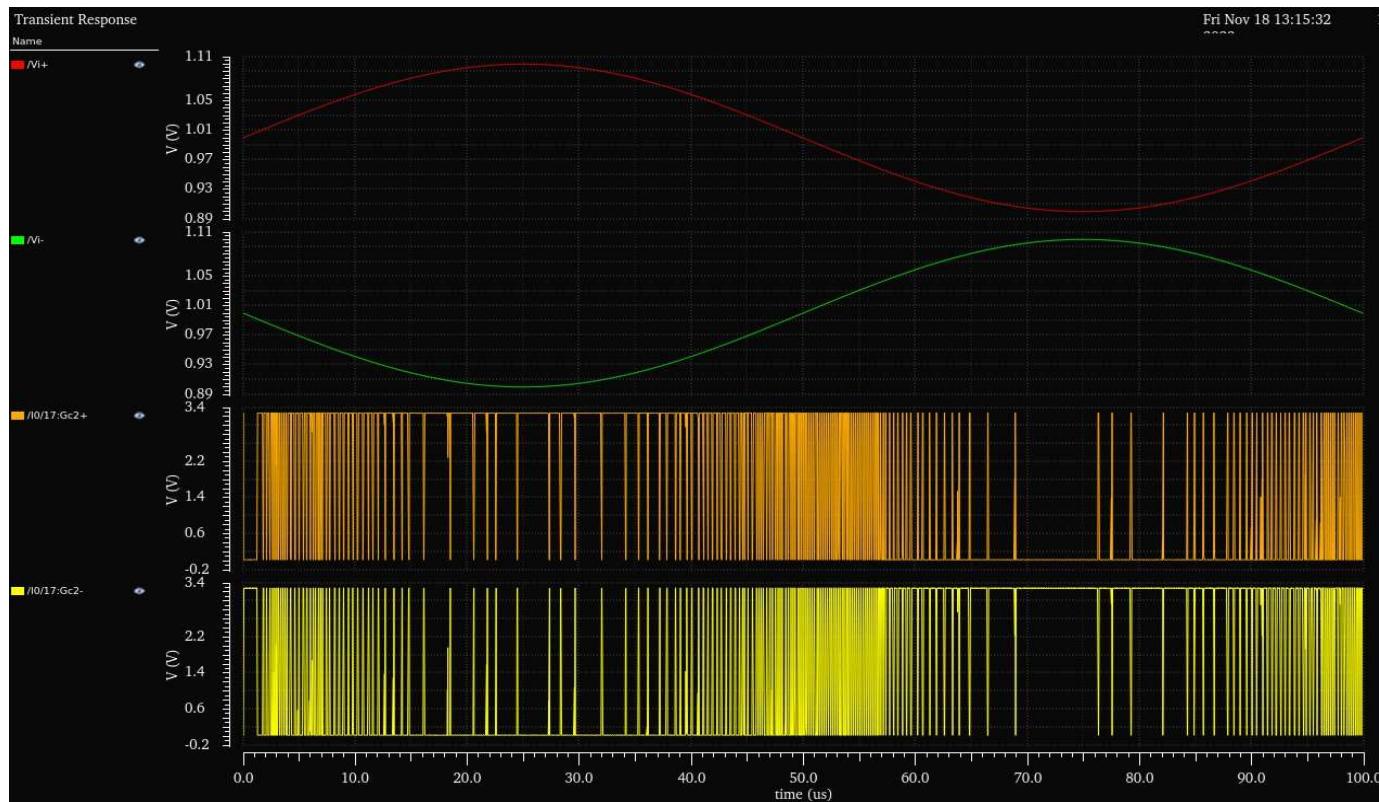
4th Order Modulator Layout–RC Extraction Results



4th Order Modulator Schematic Results



4th Order Modulator Post-Layout Simulation Results



Conclusion

- A DRC and LVS clean layouts of Fully-Differential Op-Amp, Dynamic Comparator, DAC has been designed.
- These Blocks are further integrated to obtain a DRC and LVS cleaned Second Order and Fourth Order Modulator.
- The Schematic and Post-Layout Simulation Results are comparatively same except for some delay caused due to the added parasitics in the layout.

References in IEEE format

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- [2] R. Jacob Baker. Cmos circuit design, layout and simulation. IEEE Press.
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THANK YOU