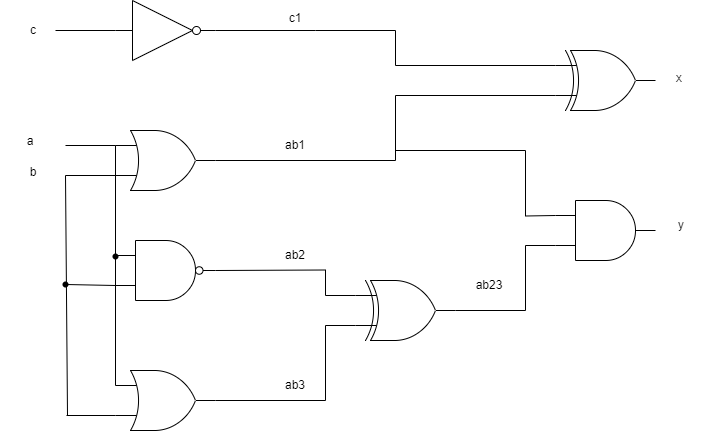
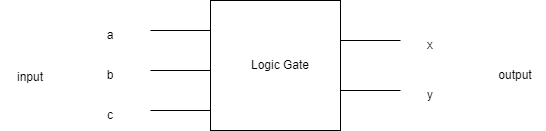
Truth Table:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **a** | **b** | **c** | **c1** | **ab1** | **ab2** | **ab3** | **ab23** | **x** | **y** |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |

Circuit Diagram:



Logic gate:



Errors in code:

Listing 4:

* There is no need of comma after carry in line 6.
* We can use “always\_comb” and “begin” instead of begin and we also use “end ” to end the program.
* In line 10 we can use “&” after “c”.

Listing 5:

* We have to add “logiccarry1” after line no 5.
* We have to add “DUT” name in line no 7.
* In line no 18 we have to write a1,b1,c1 .
* In line no 20 we have to write c1.
* In line no 24 we have to write b1.
* In line no 30 we have to write a1.
* To increase the time limit we have to increase the time value.
* At the end before “endmodule” we have to write “end” so that we can end the execution.