# Experiment No 5:

# Combinational Circuits:

# Structural Modeling Simulation

## Submitted To:

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Section D

# Digital System

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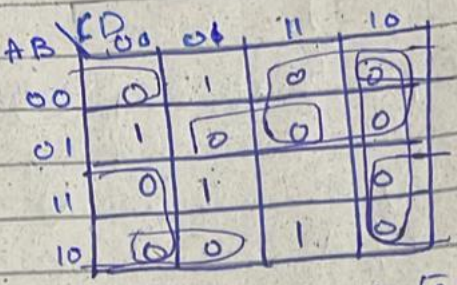
## Truth table

| characters | A1 | A0 | B1 | B0 | seg a | seg b | seg c | seg d | seg e | seg f | seg g |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 2 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 3 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 4 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 5 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 6 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 7 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 8 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 9 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| A | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| B | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| C | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| D | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| E | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| F | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |

| charachters | A2 | A1 | A0 | an. 0 | an. 1 | an. 2 | an.3 | an.4 | an.5 | an.6 | an.7 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 2 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 3 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 4 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 5 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 6 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 7 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |

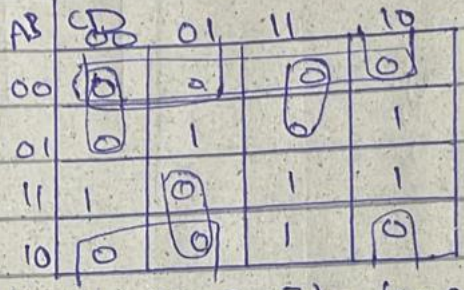
## K-maps

Seg A:



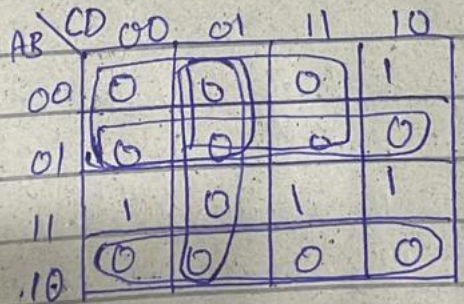

$(\bar{A}+D)\cdot(A+\bar{C})\cdot(\bar{B}+\bar{C})\cdot(\bar{B}+D)\cdot(\bar{A}+B+C)\cdot(A+\bar{B}+\bar{D})$

Seg B:



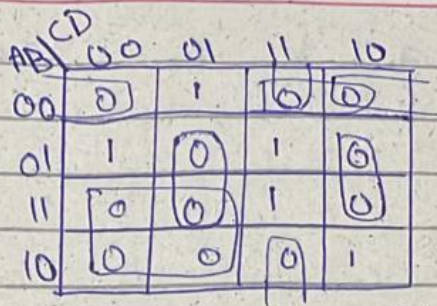

$(B+C)\cdot(B+D)\cdot(A+\bar{C}+\bar{D})\cdot(A+C+D)\cdot(\bar{A}+C+\bar{D})$

Seg C:



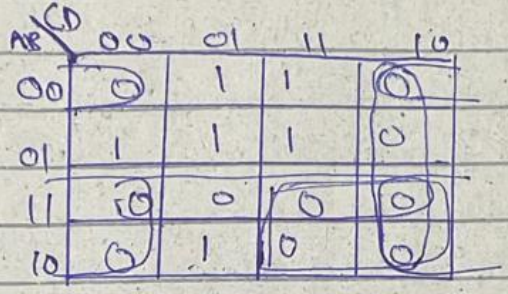

$(A+C)\cdot(A+\bar{D})\cdot(A+\bar{B})\cdot(C+\bar{D})\cdot(\bar{A}+B)$

Seg D



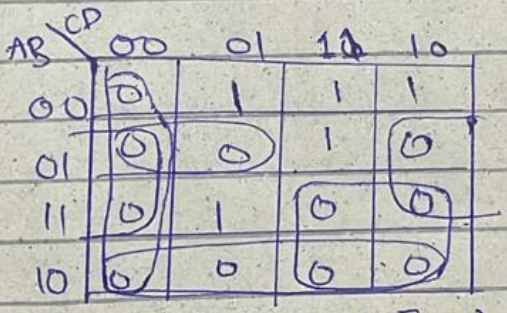

$(\bar{A}+C)\cdot(\bar{B}+C+D)\cdot(A+B+D)\cdot(B+\bar{C}+\bar{D})\cdot(\bar{B}+\bar{C}+D)$

Seg E



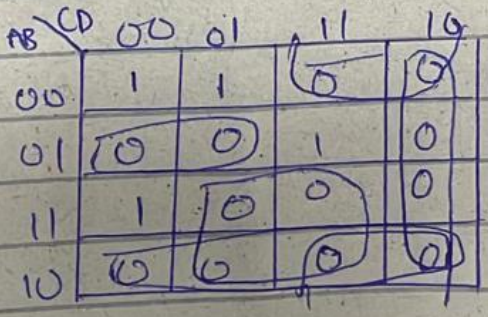

$(B+D)\cdot(\bar{A}+\bar{C})\cdot(\bar{A}+\bar{B})\cdot(\bar{C}+D)$

Seg F



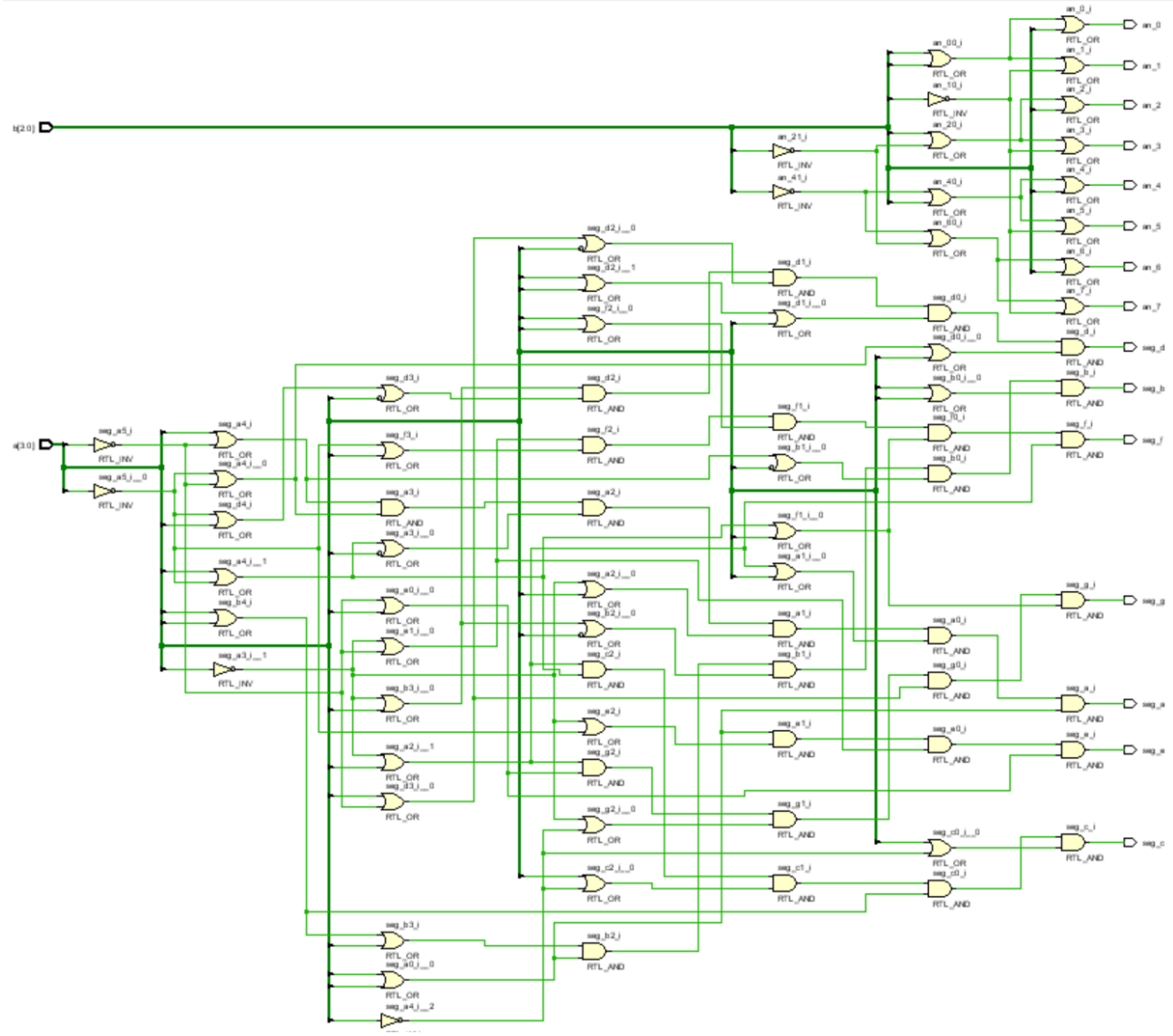

$(\bar{A}+\bar{C})\cdot(\bar{B}+D)\cdot(C+D)\,(A+\bar{B}+C)\cdot(\bar{A}+B)$

Seg G




$(\bar{A}+B)\cdot(\bar{C}+D)\cdot(\bar{A}+D)\cdot(B+\bar{C})\cdot(A+\bar{B}+C)$

## Circuit diagram using vivado:



## Maximum combinational delay in Synthesis:

| Name | Slack ^1 | Levels | Routes | High Fanout | From | To | Total Delay | Logic Delay | Net Delay | Requirement | Source Clock | Destination Clock | Exception |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Path 1 | ∞ | 3 | 2 | 8 | b[0] | an_2 | 6.836 | 5.230 | 1.606 | ∞ | input port clock | | |
| Path 2 | ∞ | 3 | 2 | 8 | b[2] | an_3 | 6.805 | 5.199 | 1.606 | ∞ | input port clock | | |
| Path 3 | ∞ | 3 | 2 | 8 | b[2] | an_7 | 6.804 | 5.199 | 1.606 | ∞ | input port clock | | |
| Path 4 | ∞ | 3 | 2 | 7 | a[1] | seg_f | 6.798 | 5.192 | 1.606 | ∞ | input port clock | | |
| Path 5 | ∞ | 3 | 2 | 7 | a[1] | seg_b | 6.792 | 5.187 | 1.606 | ∞ | input port clock | | |
| Path 6 | ∞ | 3 | 2 | 7 | a[1] | seg_a | 6.792 | 5.186 | 1.606 | ∞ | input port clock | | |
| Path 7 | ∞ | 3 | 2 | 8 | b[0] | an_5 | 6.789 | 5.184 | 1.606 | ∞ | input port clock | | |
| Path 8 | ∞ | 3 | 2 | 8 | b[0] | an_4 | 6.788 | 5.182 | 1.606 | ∞ | input port clock | | |
| Path 9 | ∞ | 3 | 2 | 7 | a[3] | seg_d | 6.784 | 5.178 | 1.606 | ∞ | input port clock | | |
| Path 10 | ∞ | 3 | 2 | 8 | b[0] | an_6 | 6.779 | 5.173 | 1.606 | ∞ | input port clock | | |

## Maximum combinational delay in Implementation:

| Name | Slack | Levels | Routes | High Fanout | From | To | Total Delay | Logic Delay | Net Delay | Requirement | Source Clock | Destination Clock | Exception |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Path 1 | ∞ | 3 | 2 | 8 | b[1] | an_6 | 11.080 | 5.339 | 5.741 | ∞ | input port clock | | |
| Path 2 | ∞ | 3 | 2 | 7 | a[2] | seg_a | 10.407 | 5.414 | 4.993 | ∞ | input port clock | | |
| Path 3 | ∞ | 3 | 2 | 7 | a[2] | seg_b | 10.150 | 5.159 | 4.991 | ∞ | input port clock | | |
| Path 4 | ∞ | 3 | 2 | 8 | b[1] | an_7 | 10.114 | 5.400 | 4.714 | ∞ | input port clock | | |
| Path 5 | ∞ | 3 | 2 | 8 | b[1] | an_2 | 10.110 | 5.192 | 4.917 | ∞ | input port clock | | |
| Path 6 | ∞ | 3 | 2 | 8 | b[1] | an_3 | 9.927 | 5.406 | 4.521 | ∞ | input port clock | | |
| Path 7 | ∞ | 3 | 2 | 7 | a[2] | seg_f | 9.832 | 5.397 | 4.434 | ∞ | input port clock | | |
| Path 8 | ∞ | 3 | 2 | 8 | b[1] | an_0 | 9.649 | 5.382 | 4.268 | ∞ | input port clock | | |
| Path 9 | ∞ | 3 | 2 | 7 | a[3] | seg_d | 9.623 | 5.382 | 4.241 | ∞ | input port clock | | |
| Path 10 | ∞ | 3 | 2 | 7 | a[2] | seg_e | 9.298 | 5.137 | 4.161 | ∞ | input port clock | | |

## Resource Utilization Summary:

1. Slice Logic

| Site Type | Used | Fixed | Available | Util% |
|---|---|---|---|---|
| Slice LUTs* | 8 | 0 | 63400 | 0.01 |
| LUT as Logic | 8 | 0 | 63400 | 0.01 |
| LUT as Memory | 0 | 0 | 19000 | 0.00 |
| Slice Registers | 0 | 0 | 126800 | 0.00 |
| Register as Flip Flop | 0 | 0 | 126800 | 0.00 |
| Register as Latch | 0 | 0 | 126800 | 0.00 |
| F7 Muxes | 0 | 0 | 31700 | 0.00 |
| F8 Muxes | 0 | 0 | 15850 | 0.00 |

## 4. IO and GT Specific

| Site Type | Used | Fixed | Available | Util% |
|---|---|---|---|---|
| Bonded IOB | 22 | 0 | 210 | 10.48 |
| Bonded IPADs | 0 | 0 | 2 | 0.00 |
| PHY_CONTROL | 0 | 0 | 6 | 0.00 |
| PHASER_REF | 0 | 0 | 6 | 0.00 |
| OUT_FIFO | 0 | 0 | 24 | 0.00 |
| IN_FIFO | 0 | 0 | 24 | 0.00 |
| IDELAYCTRL | 0 | 0 | 6 | 0.00 |
| IBUFDS | 0 | 0 | 202 | 0.00 |
| PHASER_OUT/PHASER_OUT_PHY | 0 | 0 | 24 | 0.00 |
| PHASER_IN/PHASER_IN_PHY | 0 | 0 | 24 | 0.00 |
| IDELAYE2/IDELAYE2_FINEDELAY | 0 | 0 | 300 | 0.00 |
| ILOGIC | 0 | 0 | 210 | 0.00 |
| OLOGIC | 0 | 0 | 210 | 0.00 |

## 7. Primitives

| Ref Name | Used | Functional Category |
|---|---|---|
| OBUF | 15 | IO |
| LUT3 | 8 | LUT |
| LUT4 | 7 | LUT |
| IBUF | 7 | IO |