Experiment No 6:

Digital System

Submitted To:

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2022-EE-172

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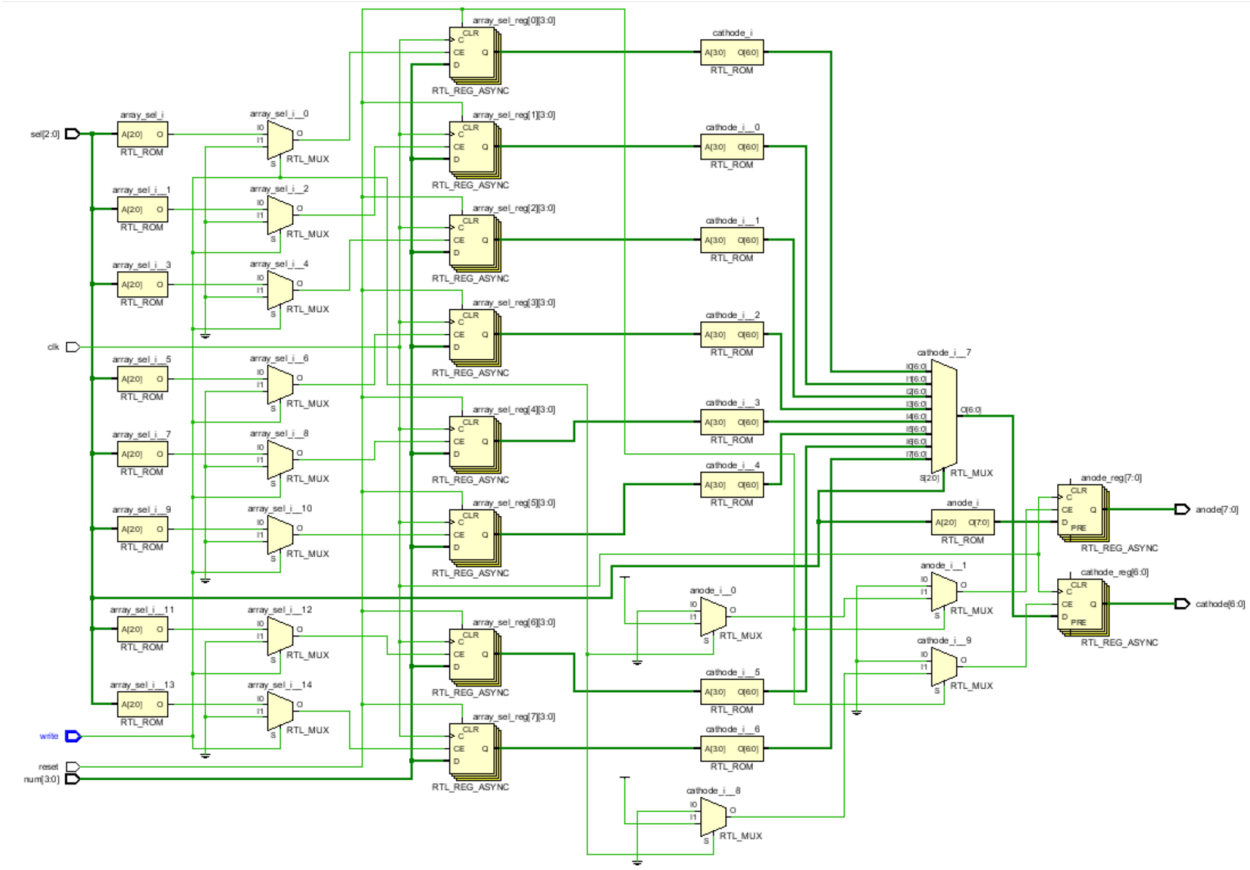
Circuit diagram:



Maximum combinational delay in implementation:

Unconstrained Paths - NONE - NONE - Setup

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destination Clock	Exception
Path 1	∞	2	1	1	anode_reg[6]/C	anode[6]	8.758	3.974	4.785	∞			
Path 2	∞	2	1	1	anode_reg[3]/C	anode[3]	6.878	4.146	2.732	∞			
Path 3	∞	2	1	1	cathode_reg[6]/C	cathode[6]	6.739	4.033	2.706	∞			
Path 4	∞	2	1	1	cathode_reg[5]/C	cathode[5]	6.710	4.011	2.699	∞			
Path 5	∞	2	1	1	cathode_reg[3]/C	cathode[3]	6.638	4.006	2.632	∞			
Path 6	∞	2	1	1	anode_reg[2]/C	anode[2]	6.608	4.030	2.578	∞			
Path 7	∞	2	1	1	anode_reg[7]/C	anode[7]	6.531	4.009	2.522	∞			
Path 8	∞	2	1	1	anode_reg[0]/C	anode[0]	6.469	3.992	2.478	∞			
Path 9	∞	2	1	1	cathode_reg[1]/C	cathode[1]	6.367	4.079	2.288	∞			
Path 10	∞	2	1	1	cathode_reg[4]/C	cathode[4]	6.332	4.011	2.321	∞			

Unconstrained Paths - NONE - NONE - Hold

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destination Clock	Exception
Path 11	∞	4	2	7	array_sel_reg[6][2]/C	cathode_reg[0]/D	0.641	0.356	0.285	-∞			
Path 12	∞	4	2	7	array_sel_reg[6][1]/C	cathode_reg[2]/D	0.642	0.367	0.275	-∞			
Path 13	∞	4	2	7	array_sel_reg[0][2]/C	cathode_reg[6]/D	0.660	0.379	0.281	-∞			
Path 14	∞	4	2	7	array_sel_reg[5][1]/C	cathode_reg[3]/D	0.661	0.368	0.293	-∞			
Path 15	∞	1	1	8	num[1]	array_sel_reg[1][1]/D	0.698	0.253	0.445	-∞	input port clock		
Path 16	∞	4	2	7	array_sel_reg[2][3]/C	cathode_reg[1]/D	0.722	0.356	0.366	-∞			
Path 17	∞	1	1	8	num[1]	array_sel_reg[4][1]/D	0.741	0.253	0.488	-∞	input port clock		
Path 18	∞	1	1	8	num[1]	array_sel_reg[6][1]/D	0.741	0.253	0.488	-∞	input port clock		
Path 19	∞	1	1	8	num[1]	array_sel_reg[0][1]/D	0.751	0.253	0.498	-∞	input port clock		
Path 20	∞	4	2	7	array_sel_reg[2][3]/C	cathode_reg[5]/D	0.752	0.365	0.387	-∞			

Maximum combinational delay in synthesis:

Unconstrained Paths - NONE - NONE - Setup

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock
Path 1	∞	2	1	1	cathode_reg[6]/C	cathode[6]	5.033	4.230	0.803	∞	
Path 2	∞	2	1	1	anode_reg[2]/C	anode[2]	5.030	4.227	0.803	∞	
Path 3	∞	2	1	1	cathode_reg[1]/C	cathode[1]	5.017	4.214	0.803	∞	
Path 4	∞	2	1	1	cathode_reg[5]/C	cathode[5]	5.011	4.208	0.803	∞	
Path 5	∞	2	1	1	anode_reg[7]/C	anode[7]	5.009	4.206	0.803	∞	
Path 6	∞	2	1	1	anode_reg[3]/C	anode[3]	5.008	4.205	0.803	∞	
Path 7	∞	2	1	1	anode_reg[5]/C	anode[5]	5.008	4.205	0.803	∞	
Path 8	∞	2	1	1	cathode_reg[3]/C	cathode[3]	5.006	4.203	0.803	∞	
Path 9	∞	2	1	1	anode_reg[4]/C	anode[4]	5.006	4.203	0.803	∞	
Path 10	∞	2	1	1	cathode_reg[0]/C	cathode[0]	4.993	4.190	0.803	∞	

Unconstrained Paths - NONE - NONE - Hold

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock
Path 11	∞	1	1	8	num[0]	array_sel_reg[0][0]/D	0.583	0.245	0.338	-∞	input port clock
Path 12	∞	1	1	8	num[0]	array_sel_reg[1][0]/D	0.583	0.245	0.338	-∞	input port clock
Path 13	∞	1	1	8	num[0]	array_sel_reg[2][0]/D	0.583	0.245	0.338	-∞	input port clock
Path 14	∞	1	1	8	num[0]	array_sel_reg[3][0]/D	0.583	0.245	0.338	-∞	input port clock
Path 15	∞	1	1	8	num[0]	array_sel_reg[4][0]/D	0.583	0.245	0.338	-∞	input port clock
Path 16	∞	1	1	8	num[0]	array_sel_reg[5][0]/D	0.583	0.245	0.338	-∞	input port clock
Path 17	∞	1	1	8	num[0]	array_sel_reg[6][0]/D	0.583	0.245	0.338	-∞	input port clock
Path 18	∞	1	1	8	num[0]	array_sel_reg[7][0]/D	0.583	0.245	0.338	-∞	input port clock
Path 19	∞	1	1	8	num[3]	array_sel_reg[0][3]/D	0.584	0.245	0.338	-∞	input port clock
Path 20	∞	1	1	8	num[3]	array_sel_reg[1][3]/D	0.584	0.245	0.338	-∞	input port clock

Resource Utilization Summary :

1. Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	80	0	63400	0.13
LUT as Logic	80	0	63400	0.13
LUT as Memory	0	0	19000	0.00
Slice Registers	47	0	126800	0.04
Register as Flip Flop	47	0	126800	0.04
Register as Latch	0	0	126800	0.00
F7 Muxes	28	0	31700	0.09
F8 Muxes	0	0	15850	0.00

4. IO and GT Specific

Site Type	Used	Fixed	Available	Util%
Bonded IOB	25	0	210	11.90
Bonded IPADs	0	0	2	0.00
PHY_CONTROL	0	0	6	0.00
PHASER_REF	0	0	6	0.00
OUT_FIFO	0	0	24	0.00
IN_FIFO	0	0	24	0.00
IDELAYCTRL	0	0	6	0.00
IBUFDS	0	0	202	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	24	0.00
PHASER_IN/PHASER_IN_PHY	0	0	24	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	300	0.00
ILOGIC	0	0	210	0.00
OLOGIC	0	0	210	0.00

5. Clocking

Site Type	Used	Fixed	Available	Util%
BUFGCTRL	1	0	32	3.13
BUFIO	0	0	24	0.00
MMCME2_ADV	0	0	6	0.00
PLLE2_ADV	0	0	6	0.00
BUFMRCE	0	0	12	0.00
BUFHCE	0	0	96	0.00
BUFR	0	0	24	0.00

7. Primitives

Ref Name	Used	Functional Category
LUT4	64	LUT
FDCE	32	Flop & Latch
MUXF7	28	MuxFx
OBUF	15	IO
IBUF	10	IO
LUT2	8	LUT
FDSE	8	Flop & Latch
LUT6	7	LUT
FDRE	7	Flop & Latch
LUT3	4	LUT
BUFG	1	Clock