卷积模块HLS综合结果

Synthesis Summary Report of 'Conv'

General Information

Date: Tue Jul 18 15:48:21 2023
Version: 2022.2 (Build 3670227 on Oct 13 2022)
Project: conv

Solution: solution1 (Vivado IP Flow Target)
Product family: zynq
Target device: xc7z020-clg484-1

Timing Estimate

Target	Estimated	Uncertainty
10.00 ns	7.300 ns	2.70 ns

Performance & Resource Estimates

Modules Loops

Modules & Loops	Issue Type	Violation Type	Distance	Slack	Latency(cycles)	Latency(ns)	Iteration Latency	Interval	Trip Count	Pipelined	BRAM	DSP	FF	LUT	URAM
Conv				-	-	-	-	-	-	no	0	26	5387	6050	0
VITIS_LOOP_45_1_VITIS_LOOP_46_2_VITIS_LOOP_47_3	II Violation			-	-	-	-	-	4261413375	no	-	-	-	-	-

Performance Pragma

Modules & Loops	Target TI(cycles)	TI(cycles)	TI met
Conv	-	-	-
VITIS_LOOP_45_1_VITIS_LOOP_46_2_VITIS_LOOP_47_3	-	-	-

HW Interfaces

M_AXI

Interface	Data Width (SW->HW)	Address Width	Latency	Offset	Register	Max Widen Bitwidth	Max Read Burst Length	Max Write Burst Length	Num Read Outstanding	Num Write Outstanding
m_axi_gmem	32 -> 32	64	0	slave	0	0	16	16	16	16

池化模块HLS综合结果

Synthesis Summary Report of 'Pool'

General Information

Date: Tue Jul 18 16:02:11 2023
Version: 2022.2 (Build 3670227 on Oct 13 2022)
Project: pool
Solution: solution1 (Vivado IP Flow Target)
Product family: zynq
Target device: xc7z020-clg484-1

Timing Estimate

Target	Estimated	Uncertainty
10.00 ns	7.300 ns	2.70 ns

Performance & Resource Estimates

% Modules Loops

Modules & Loops	Issue Type	Violation Type	Distance	Slack	Latency(cycles)	Latency(ns)	Iteration Latency	Interval	Trip Count	Pipelined	BRAM	DSP	FF	LUT	URAM
Pool				-	-	-	-	0	-	no	0	19	4026	4668	0
VITIS_LOOP_24_1_VITIS_LOOP_25_2_VITIS_LOOP_26_3	II Violation			-	?	?	325177	-	281462092005375	no	-	-	-	-	-

Performance Pragma

Modules & Loops	Target TI(cycles)	TI(cycles)	TI met
Pool	-	-	-
VITIS_LOOP_24_1_VITIS_LOOP_25_2_VITIS_LOOP_26_3	-	-	-

HW Interfaces

M_AXI

Interface	Data Width (SW->HW)	Address Width	Latency	Offset	Register	Max Widen Bitwidth	Max Read Burst Length	Max Write Burst Length	Num Read Outstanding	Num Write Outstanding
m_axi_gmem	32 -> 32	64	0	slave	0	0	16	16	16	16

Vivado Block Design