

# LI-IMX274-MIPI-CS Data Sheet

### **Key Features**

- Sony Diagonal 7.20 mm (Type 1/2.5) CMOS Image Sensor IMX274
- Active pixels: 3864H x 2196V
- Pixel size: 1.62 um x 1.62 um
- Color sensor
- Interface: MIPI output
- Support CS lens
- Module Size: 38mmx38mm
- Weight: 54 g
- Part#: LI-IMX274-MIPI-CS

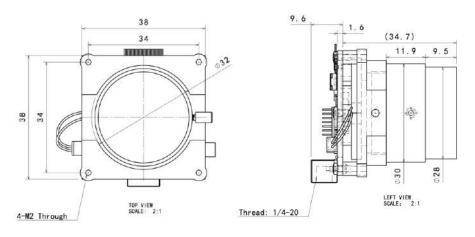


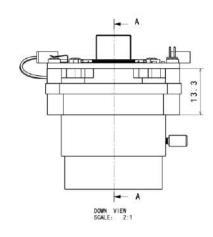


## **Lens Spec**

- Model: ES0522F.IR
- Focal length: 5.0 mm
- Aperture, F/#: 2.2
- Built in 650nm IR cut filter
- FOV (D/H/V): 87 °/76 °/43 °
- TV Distortion: < -8%
- Mount Type: CS

#### **Dimensions**

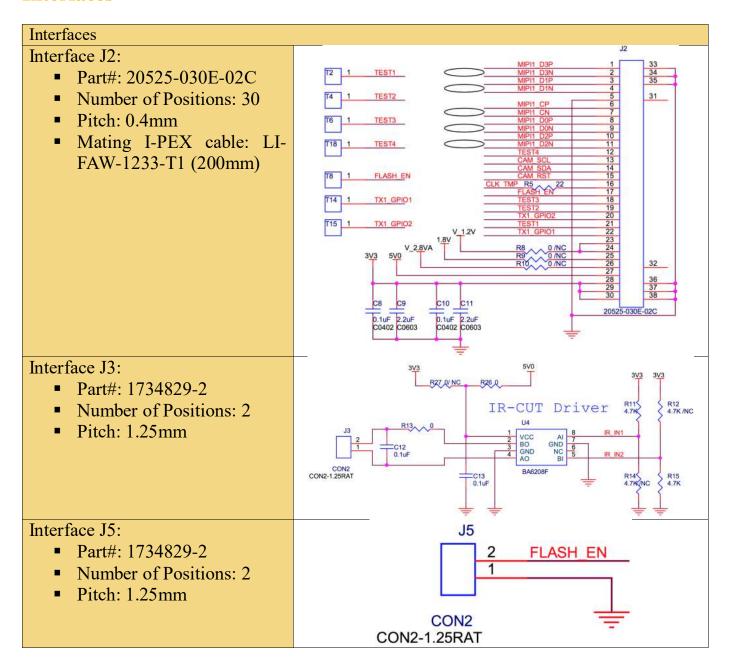






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#### **Interfaces**



# **IMX274 Sensor Spec**

## **Absolute Maximum Ratings**

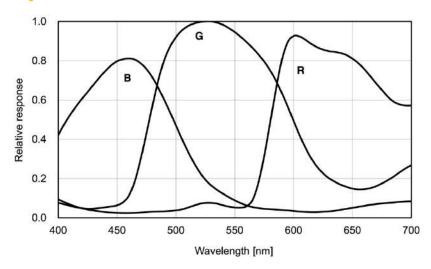
Item	Symbol	Ratings	Unit
Supply voltage (Analog)	V <sub>ADD</sub> *1	-0.3 to +3.3	٧
Supply voltage (Digital 1)	V <sub>DDD1</sub> *2	-0.5 to +2.0	٧
Supply voltage (Digital 2)	V <sub>DDD2</sub> *3	-0.5 to +3.3	٧
Input voltage (Digital)	Vı	-0.3 to V <sub>DDD2</sub> + 0.3	V
Output voltage (Digital)	Vo	-0.3 to V <sub>DDD2</sub> + 0.3	V
Guaranteed operating temperature	T <sub>OPR</sub>	-30 to +75	°C
Storage guarantee temperature	T <sub>STG</sub>	-30 to +80	°C
Performance guarantee temperature	T <sub>SPEC</sub>	-10 to +60	°C

## **Recommended Operating Conditions**

Item	Symbol	Rating	Unit
Supply voltage (Analog)	V <sub>ADD</sub> *1	2.8 ± 0.1	٧
Supply voltage (Digital 1)	V <sub>DDD1</sub> *2	1.2 ± 0.1	V
Supply voltage (Digital 2)	V <sub>DDD2</sub> *3	1.8 ± 0.1	V
Input voltage (Digital)	Vı	-0.1 to V <sub>DDD2</sub> + 0.1	V

<sup>&</sup>lt;sup>1</sup> V<sub>ADD</sub>: V<sub>DD</sub>SUB, V<sub>DD</sub>HCM, V<sub>DD</sub>HPX, V<sub>DD</sub>HDA, V<sub>DD</sub>HCP (2.8 V power supply)

# **Spectral Sensitivity Characteristics**





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VDDD1: VDDLCN, VDDLSC1 to 2, VDDLPA, VDDLPL1, VDDLPL2 to 3, VDDLIF (1.2 V power supply)

<sup>&</sup>lt;sup>\*3</sup> V<sub>DDD2</sub>: V<sub>DD</sub>MIO, V<sub>DD</sub>MIF (1.8 V power supply)

#### **DC** Characteristics

#### **Current Consumption and Gain Vatriable Range**

(V<sub>ADD</sub> = 2.9 V, V<sub>DDD1</sub> = 1.3 V, V<sub>DDD2</sub> = 1.9 V, Tj = 60  $^{\circ}$ C, Reference Gain (0 dB) All pixel scan mode (MODE0), 29.97 frame/s)

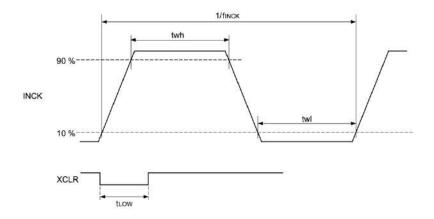
Item	Symbol	Min.	Тур.	Max	Unit	Remarks
Current consumption (Analog)	I <sub>ADD</sub>	88 <u>——</u> 9	_	62	mA	
Current consumption (Digital 1)	I <sub>DDD1</sub>	_	_	190	mA	
Current consumption (Digital 2)	I <sub>DDD2</sub>		-	1	mA	
Standby current (Analog)	I <sub>ADDSTB</sub>	_	_	35	μA	In the dark
Standby current (Digital 1)	I <sub>DDD1STB</sub>	-	· —	13	mA	In the dark
Standby current (Digital 2)	I <sub>DDD2STB</sub>	10	11 <u>—</u> 1	20	μA	In the dark
PGA gain variable range	PGAG	0	10 <del>-0</del> 0	27	dB	

#### **Supply Voltage and I/O Voltage**

It	em	Pins	Symbol	Min.	Тур.	Max.	Unit
	Analog	V <sub>DD</sub> SUB, V <sub>DD</sub> HCM, V <sub>DD</sub> HPX, V <sub>DD</sub> HDA, V <sub>DD</sub> HCP	V <sub>ADD</sub>	2.70	2.80	2.90	٧
Supply voltage	Digital 1	V <sub>DD</sub> LCN, V <sub>DD</sub> LSC1 to 2, V <sub>DD</sub> LPL1, V <sub>DD</sub> LPA, V <sub>DD</sub> LPL2 to 3, V <sub>DD</sub> LIF	V <sub>DDD1</sub>	1.10	1.20	1.30	V
	Digital 2	V <sub>DD</sub> MIO, V <sub>DD</sub> MIF	V <sub>DDD2</sub>	1.70	1.80	1.90	V
		SDA,	V <sub>IH1</sub>	$0.7 \times V_{DDD2}$	_	1.9	V
Digital in	put	SCL	V <sub>IL1</sub>	-0.3	_	0.3 × V <sub>DDD2</sub>	V
voltage		XCLR,	V <sub>IH2</sub>	0.65 × V <sub>DDD2</sub>	· —	V <sub>DDD2</sub> + 0.3	V
		INCK	V <sub>IL2</sub>	-0.3	_	0.35 × V <sub>DDD2</sub>	V
Digital ou voltage	itput	XHS, XVS	V <sub>HVOUT</sub>	_	V <sub>DDD2</sub>	_	٧

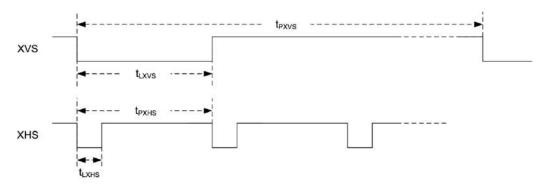
## **AC Characteristics**

#### **INCK, XCLR**



Item	Symbol	Min.	Тур.	Max.	Unit
INCK clock frequency	finck	6	_	27	MHz
INCK Low level pulse width	twl	5	(3)	_	ns
INCK High level pulse width	twh	5	7	(s <u>—</u> s	ns
Clock duty		40	50	60	%
XCLR Low level pulse width	t <sub>LOW</sub>	100	5°	-	ns

#### XHS, XVS (Output)



Item	Symbol	Min.	Тур.	Max.	Unit	Remarks
XHS Low level pulse width	t <sub>LXHS</sub>		222		ns	16 clk@72MHz
XHS pulse period	t <sub>PXHS</sub>		HMAX*1		clk@72MHz	
XVS Low level pulse width	t <sub>LXVS</sub>		t <sub>PXHS</sub>		clk@72MHz	
XVS pulse period	t <sub>PXVS</sub>		HMAX*1 × VMAX*2		clk@72MHz	

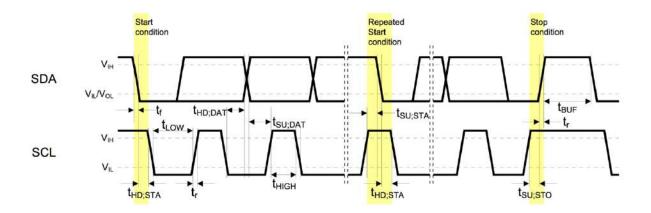
The value set as HMAX (address 30F6h, bit [7:0] and address 30F7h, bit [7:0])



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The value set as VMAX (address 30F8h, bit [7:0], address 30F9h, bit [7:0] and address 30FAh, bit [3:0]).

## I<sup>2</sup>C Communication



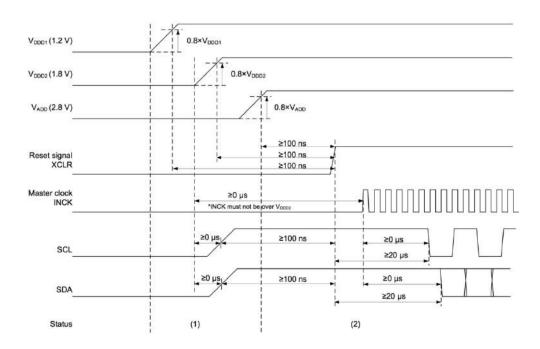
#### I<sup>2</sup>C Specification

Item	Symbol	Min.	Тур.	Max.	Unit	Remarks
Low level input voltage	V <sub>IL</sub>	-0.3	·—	0.3 × V <sub>DDD2</sub>	V	
High level input voltage	VIH	0.7 × V <sub>DDD2</sub>	5 <del></del> 1	1.9	V	
Low level output voltage	VoL	0	-	$0.2 \times V_{DDD2}$	٧	V <sub>DDD2</sub> < 2 V, Sink 3 mA
Output fall time	tof	_	3 <del></del> 3	250	ns	Load 10 pF to 400 pF, 0.7 × V <sub>DDD2</sub> to 0.3 × V <sub>DDD2</sub>
Input current (SCL, SDA, XCLR, INCK)	li I	-10		10	μA	0.1 × V <sub>DDD2</sub> to 0.9 × V <sub>DDD2</sub>
Input capacitance of SCL / SDA	Ci	_	2 <del></del> 1	10	pF	

## I<sup>2</sup>C AC Characteristics

Item	Symbol	Min.	Тур.	Max.	Unit
SCL clock frequency	f <sub>SCL</sub>	0	-	400	kHz
Hold time (Start Condition)	t <sub>HD;STA</sub>	0.6	_	# <u>—</u> #	μs
Low period of the SCL clock	t <sub>LOW</sub>	1.3		—.	μs
High period of the SCL clock	t <sub>HIGH</sub>	0.6	-	_	μs
Set-up time (Repeated Start Condition)	t <sub>SU;STA</sub>	0.6	15-18	(a <del></del> 2).	μs
Data hold time	t <sub>HD;DAT</sub>	0	_	0.9	μs
Data set-up time	t <sub>SU;DAT</sub>	100	_		ns
Rise time of both SDA and SCL signals	t <sub>r</sub>	1		300	ns
Fall time of both SDA and SCL signals	t <sub>f</sub>	_	_	300	ns
Set-up time (Stop Condition)	t <sub>su;sto</sub>	0.6	1	-	μs
Bus free time between a STOP and START Condition	t <sub>BUF</sub>	1.3	8-8	7_0	μs

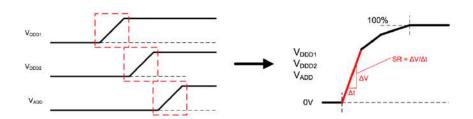
## **Power-on Sequence**



Period name	Remarks
(1) Power stabilization	All input signals are set to Low level.
period	There are no constraints of the power-on sequence with V <sub>ADD</sub> , V <sub>DDD1</sub> , and V <sub>DDD2</sub> .
(2) Register communication period for standby cancel	Wait 100 ns after the last power supply in $V_{ADD}$ , $V_{DDD1}$ and $V_{DDD2}$ . Then set XCLR to "H" and start the standby cancel sequence.

## **Slew Rate Limitation of Power-on Sequence**

Conform to the slew rate limitation shown below when power supply change  $0\ V$  to each voltage  $(0\ \%\ to\ 100\ \%)$  in power-on sequence.



Item	Symbol	Power supply	Min.	Max.	Unit	Remarks
		V <sub>DDD1</sub> (1.2 V)	( <b>—</b> )	25	mV/us	
Slew rate	SR	V <sub>DDD2</sub> (1.8 V)	14-0	25	mV/us	1
		V <sub>ADD</sub> (2.8 V)	A <del>rea -</del> O	25	mV/us	

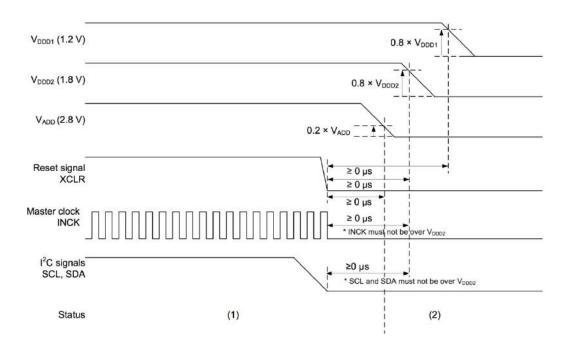


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# **Power-off Sequence**



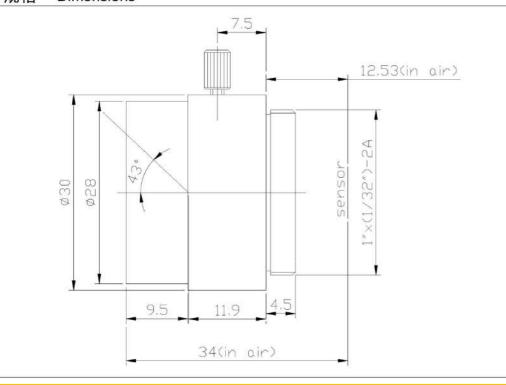
Period name	Remarks
(1) Pixel output period	Pixel signal output period
(2) Power-off period	Turn the power supplies off after all input signals are set to "Low" level except SCL and SDA. Set SCL and SDA to "Low" level at the same time with turning off the power supply of $V_{DDD2}$ . There are no constraints of the power-off sequence with $V_{ADD}$ , $V_{DDD1}$ , and $V_{DDD2}$ .

# 10 Megapixel IR Series



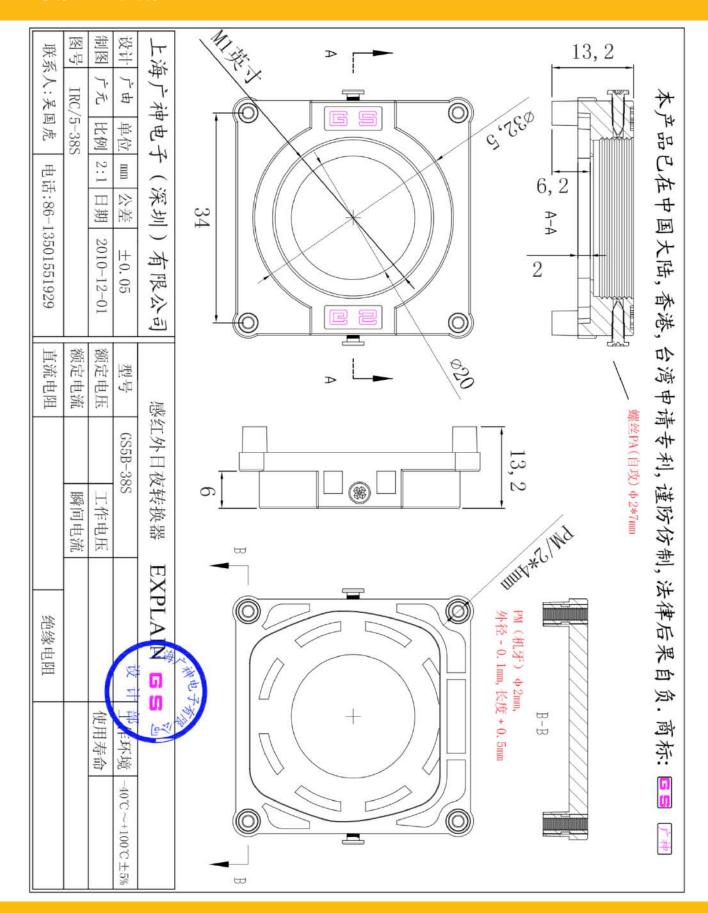


有效焦距	E.F.L.	5 mm	
相对孔径	F No.		F2.2
接口类型	Mount Type		CS
水平视角	H.FOV	1/1.8"	72°
像面尺寸	Image Format (Max)		1/1.8"
光圈类型	Iris Type		Fixed
近摄距	M.O.D		0.3m
畸 变	TV Distortion	1/1.8"	-8%
+E +& <del></del>	Ocataal Taraa	变倍 Zoom	1
操控方式	Control Type	聚焦 Focus	Manual
工作温度	Operating Temperature		-30°C ~ 70°C
镜头重量	Weight		39g
尺寸规格	Dimensions	35	





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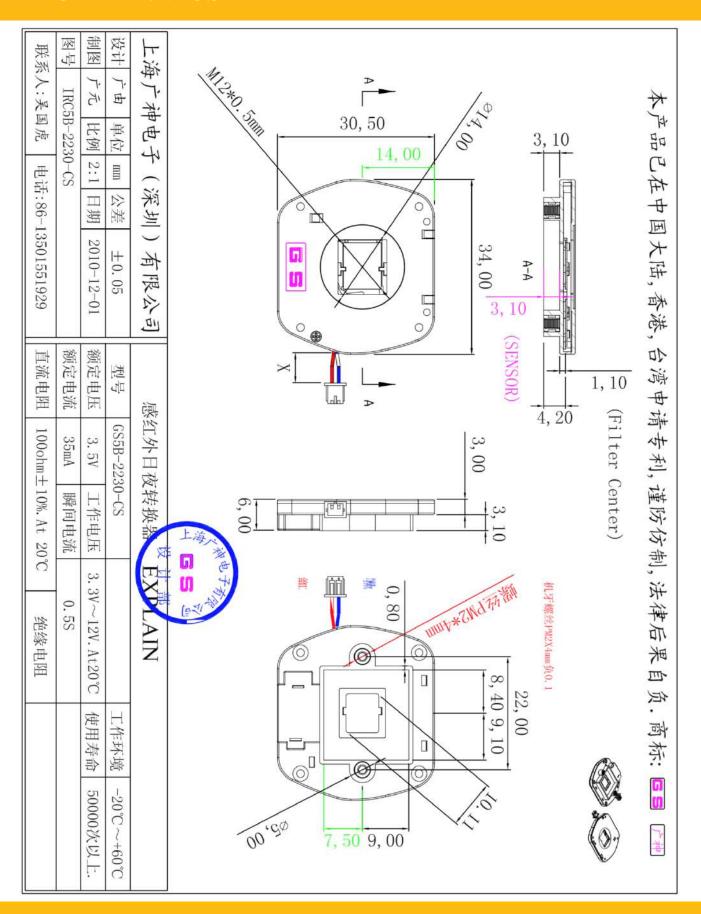




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