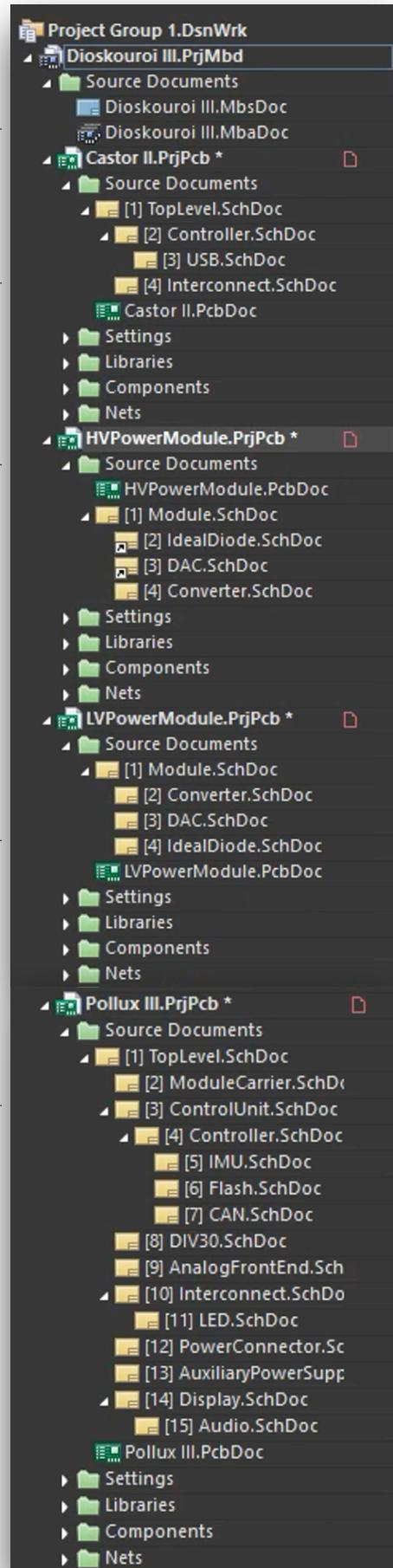


Power Supply V4

Review document

Power Supply V4



Dioskouroi III

Assembly document of all modules. Nothing to review here.

Castor II

PCB and schematics of Castor II, the power supply's 2.4GHz WiFi module. Same design as last year.

HV Power Module

PCB and schematics of the high-voltage power module.

Two 24V buck-boosts were implemented instead of one boost and one buck-boost this year. The converter schematics remains the same. Additionally, an ideal diode was added to the output and a DAC changes the feedback loop's reference to reprogram the output voltage if necessary.

Please review the PCB, IdealDiode and DAC.

LV Power Module

PCB and schematics of the low-voltage power module.

A dual buck controller that nominally provides 5V/15V is used. The converter's design is the same as last year. The PCB however has completely been redesigned.

Pollux III

PCB and schematics of the power supply's motherboard.

A STM32H7 monitors the power supplies through power monitors and temperature sensors.

As space allowed, an IMU, a touch-screen and an audio amplifier were also added to the board.

If you can, please review the PCB, Controller, IMU, AuxiliaryPowerSupply, Display and Audio. Some footprints still need to be updated though.

Castor II

WiFi Module

A

A

B

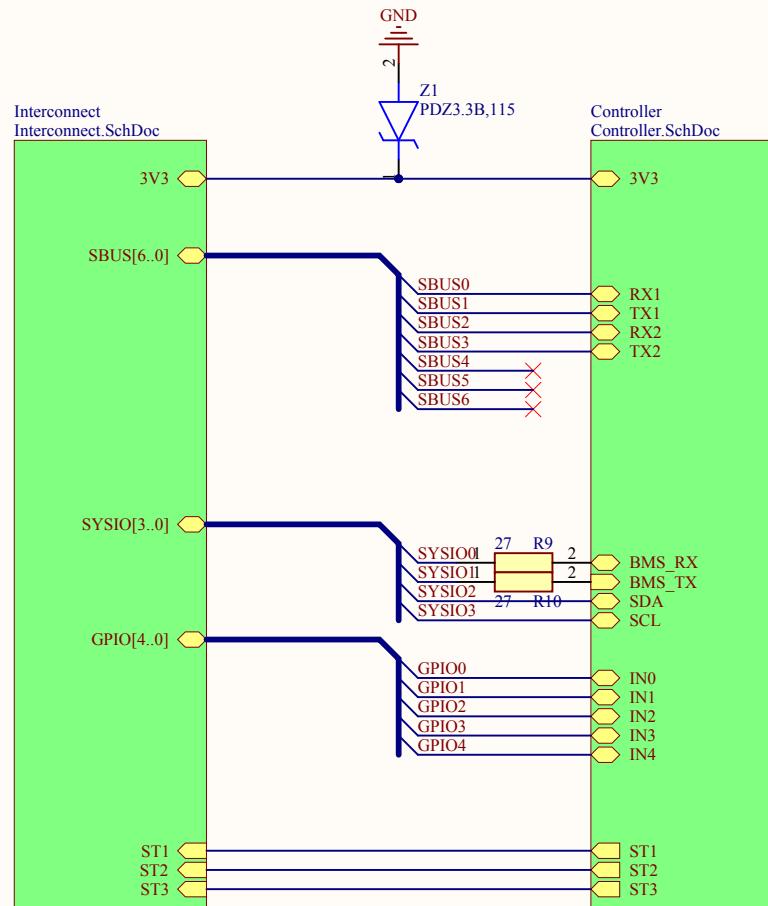
B

C

C

D

D



Title
Control Module Top Level

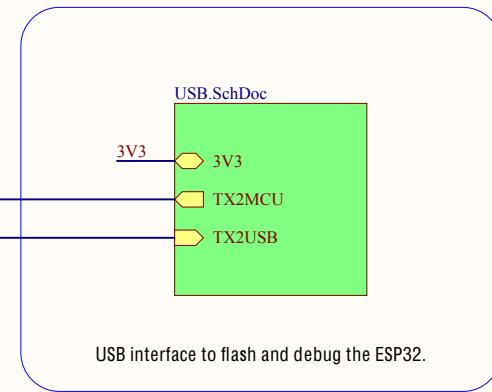
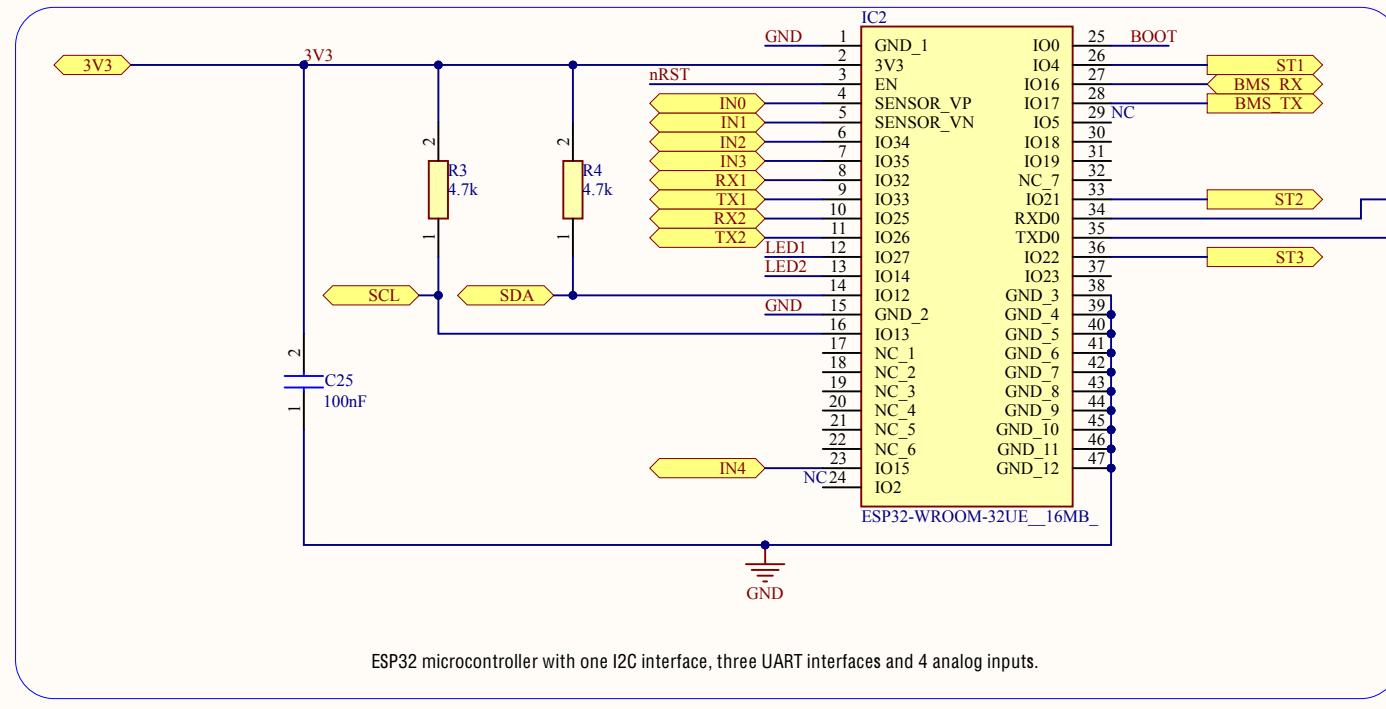
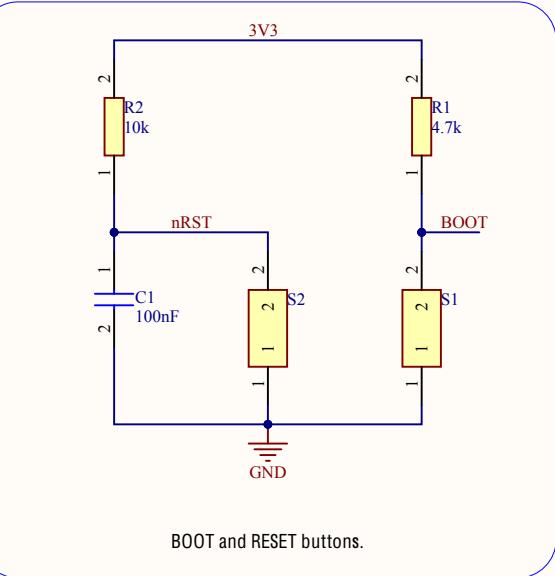
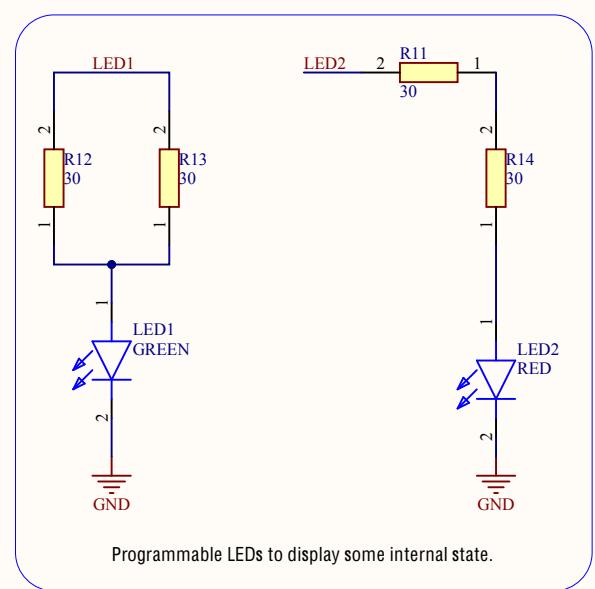
Size	Number	Revision
A4	1	1
Date:	4.04.2023	Sheet of EPFL Xplore
File:	\..\TopLevel.SchDoc	Drawn By: Arion Zimmermann

1

2

3

4



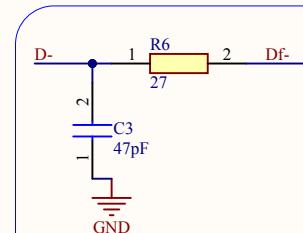
Title Power Supply Controller		
Size A4	Number 1	Revision 7
Date: 4.04.2023	Sheet of DC/DC converters	
File: \Controller.SchDoc	Drawn By: Arion Zimmermann	

1

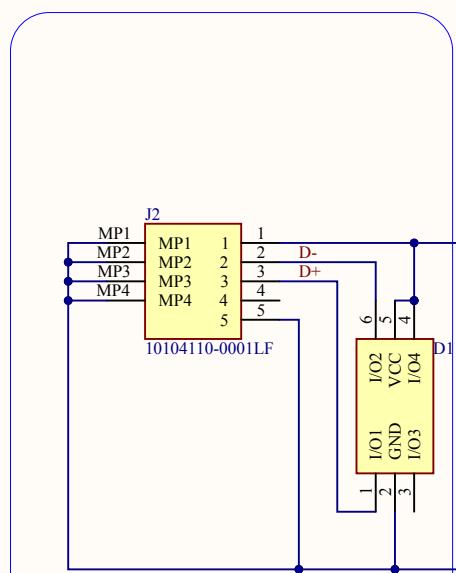
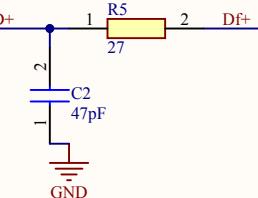
2

3

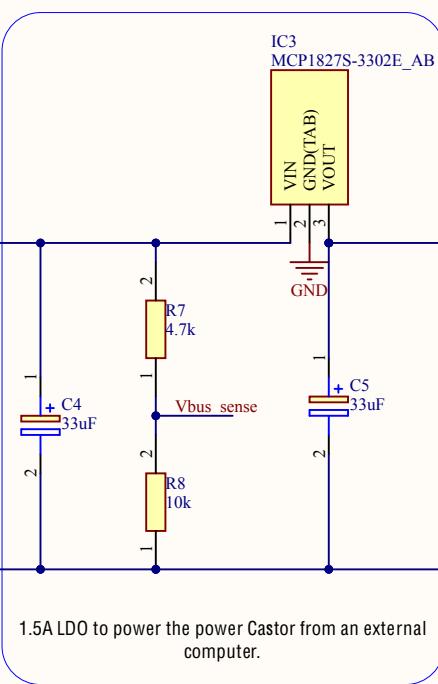
4



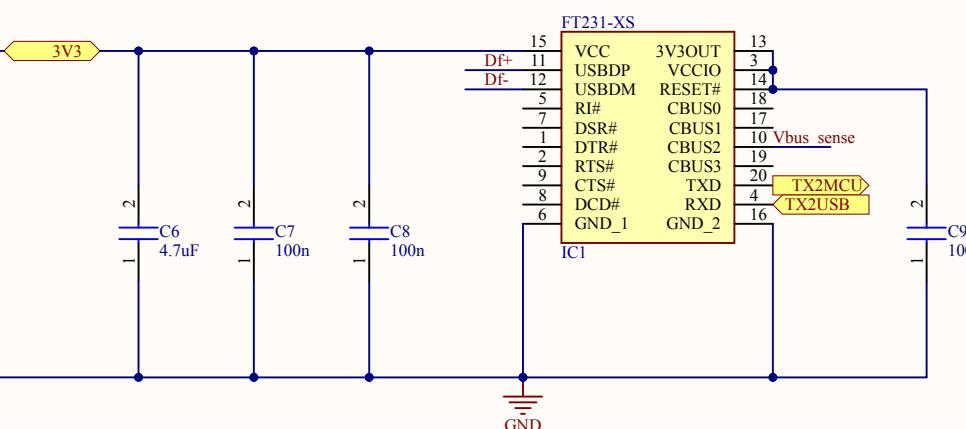
USB data RC 125MHz low-pass filter.



USB connector and anti-ESD.



1.5A LDO to power the power Castor from an external computer.



FTDI USB to UART controller.

Title		
Control Module USB Controller		
Size	Number	Revision
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Date:	4.04.2023	Sheet of EPFL Xplore
File:	\..\USB.SchDoc	Drawn By: Arion Zimmermann

A

A

B

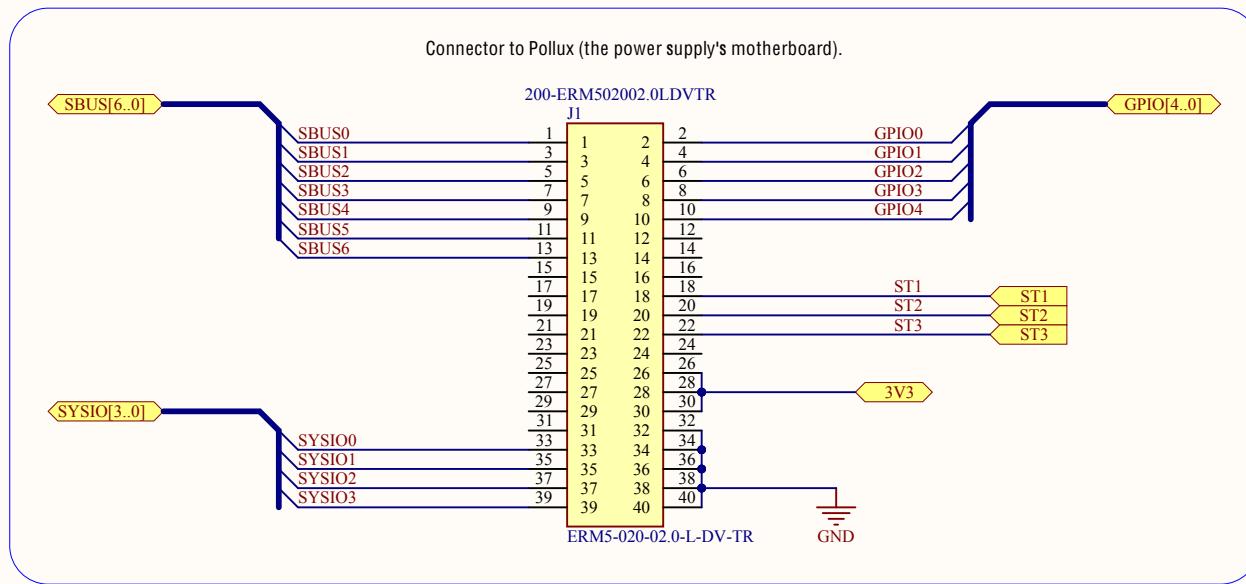
B

C

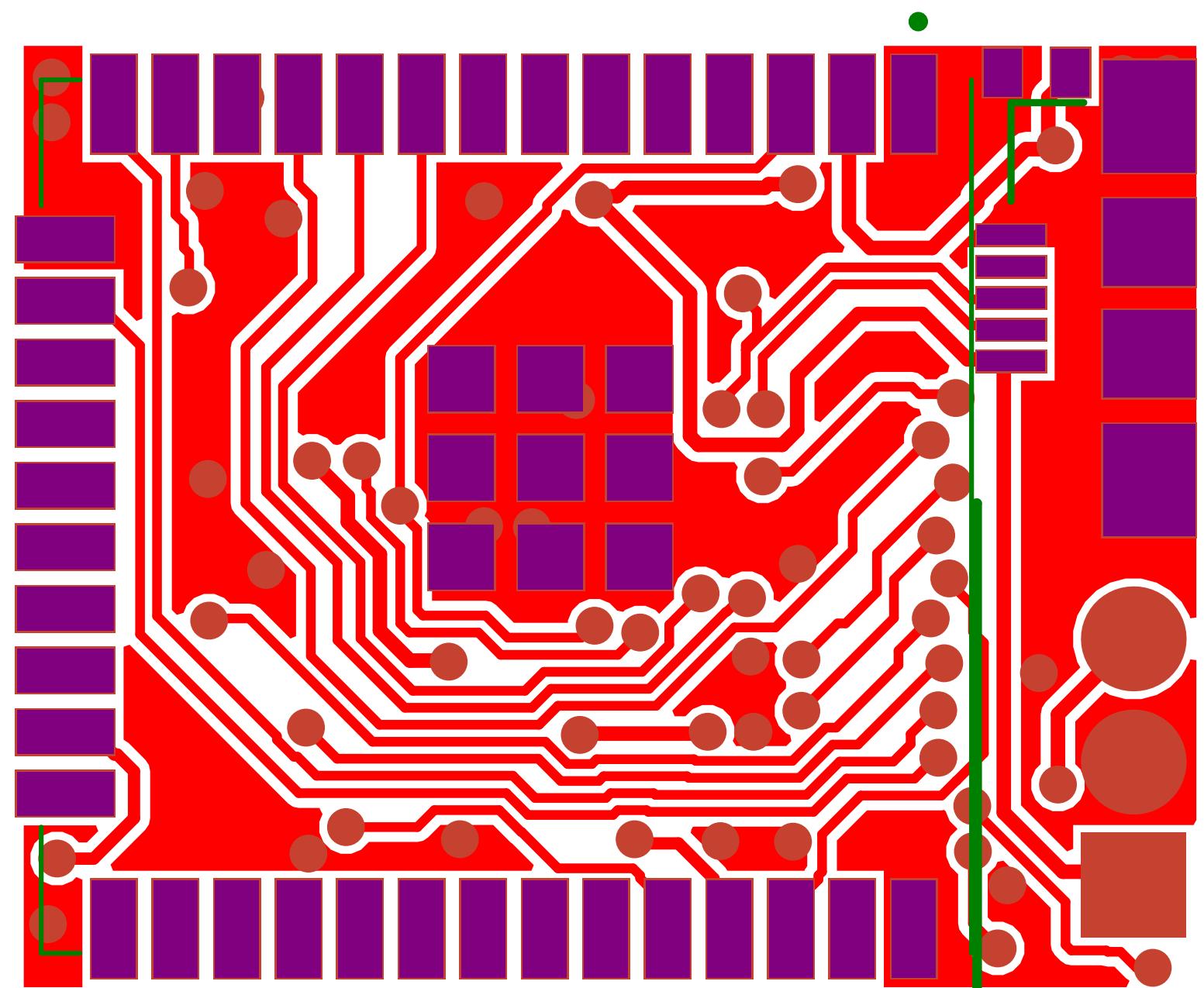
C

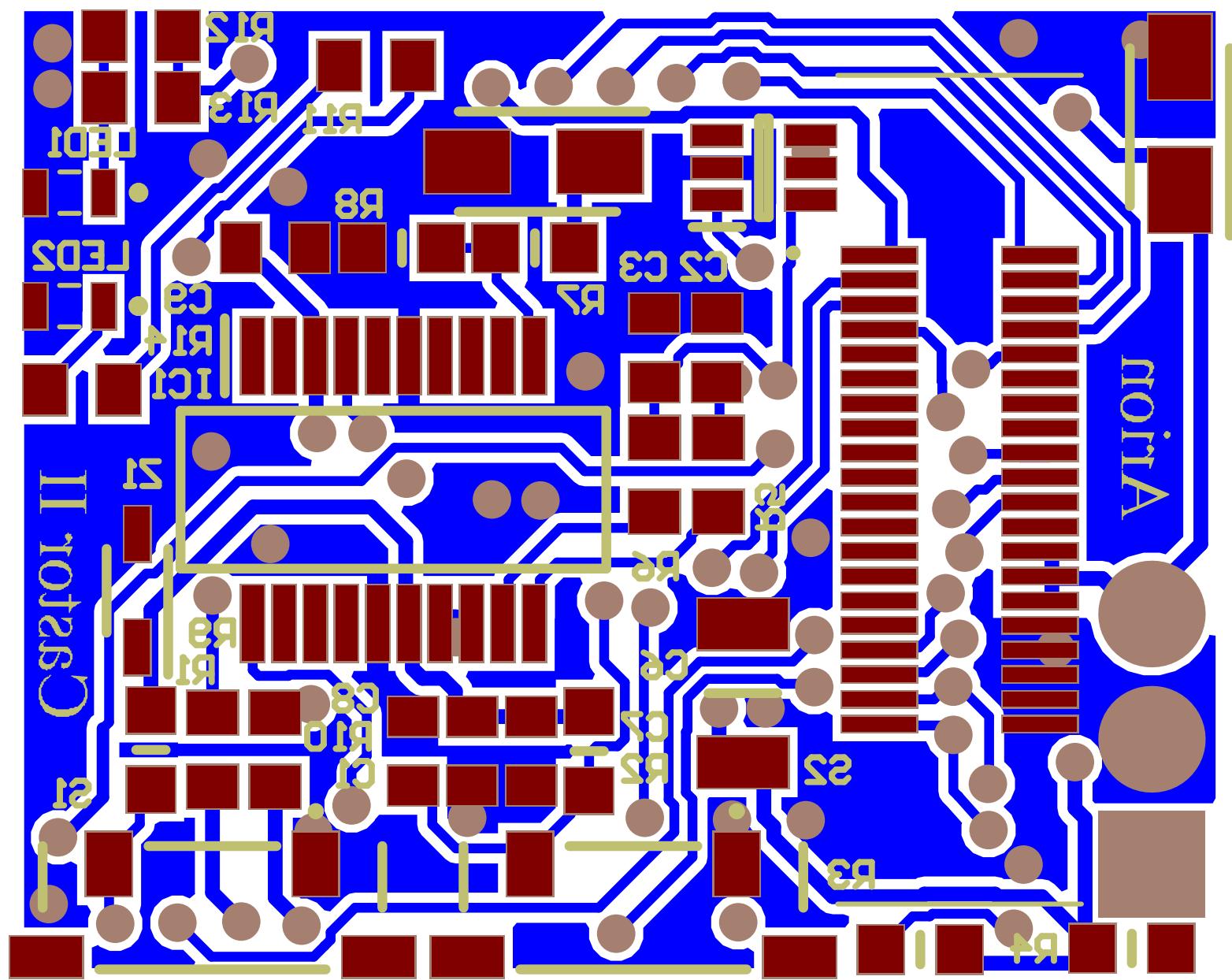
D

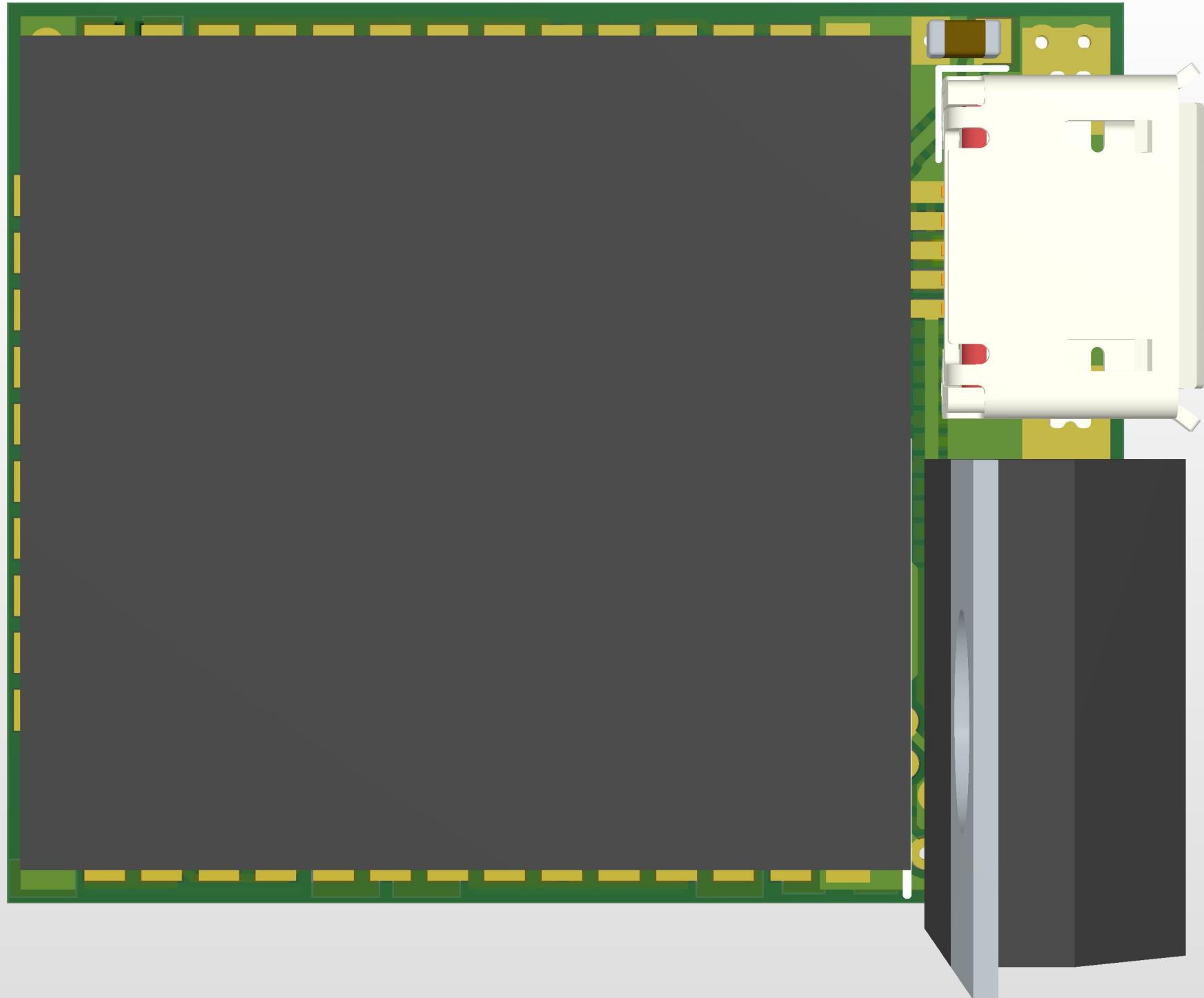
D

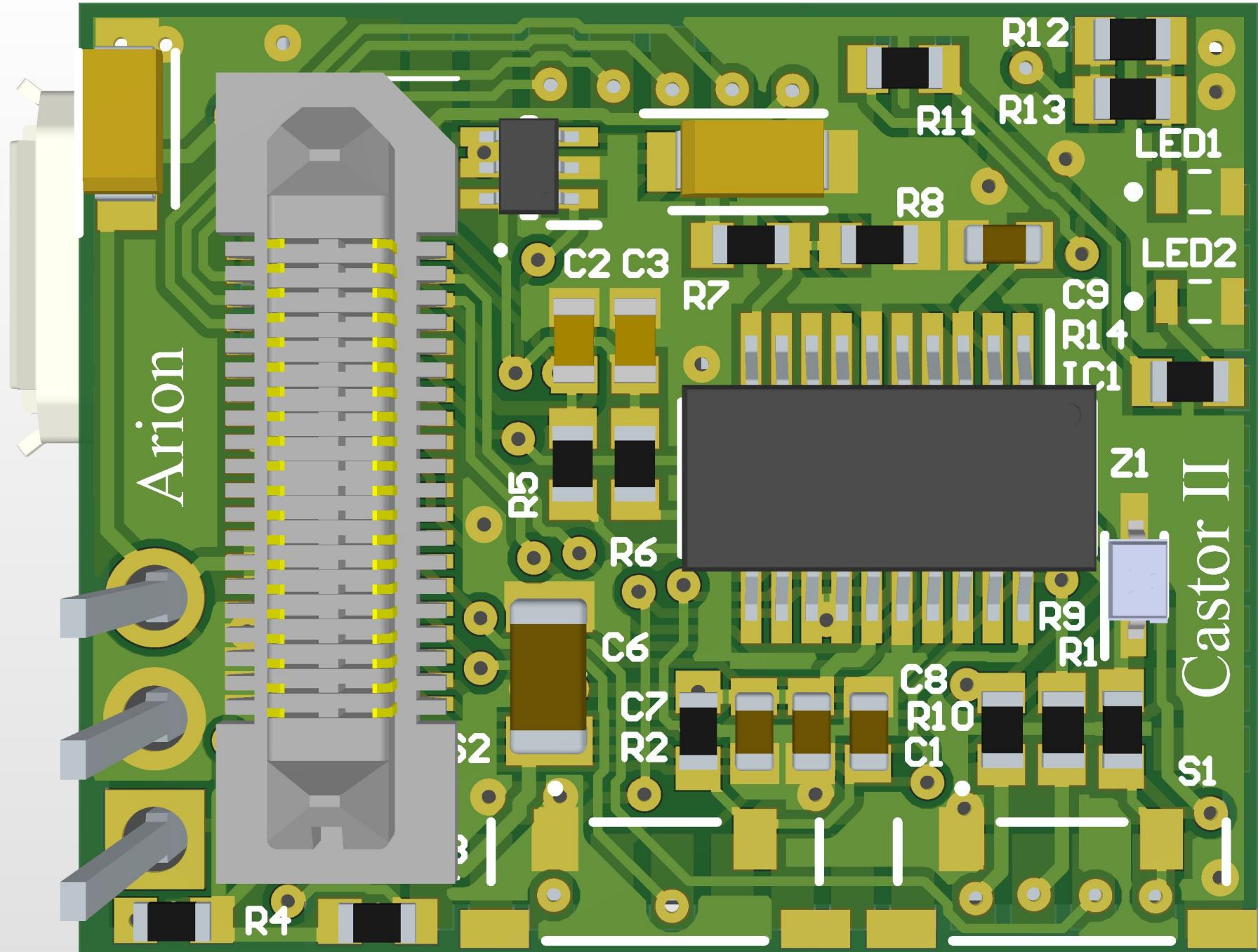


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Size A4	Number 1	Revision 1
Date: 4.04.2023	Sheet of EPFL Xplore	
File: \Interconnect.SchDoc	Drawn By: Arion Zimmermann	



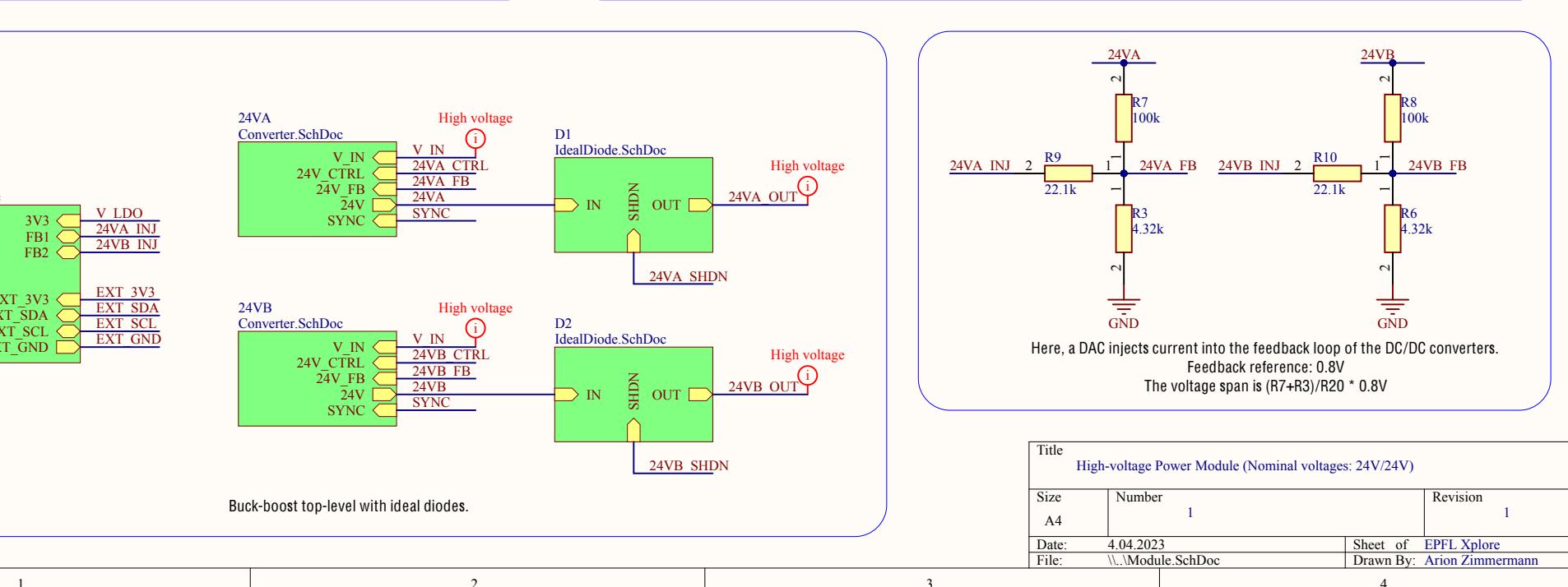
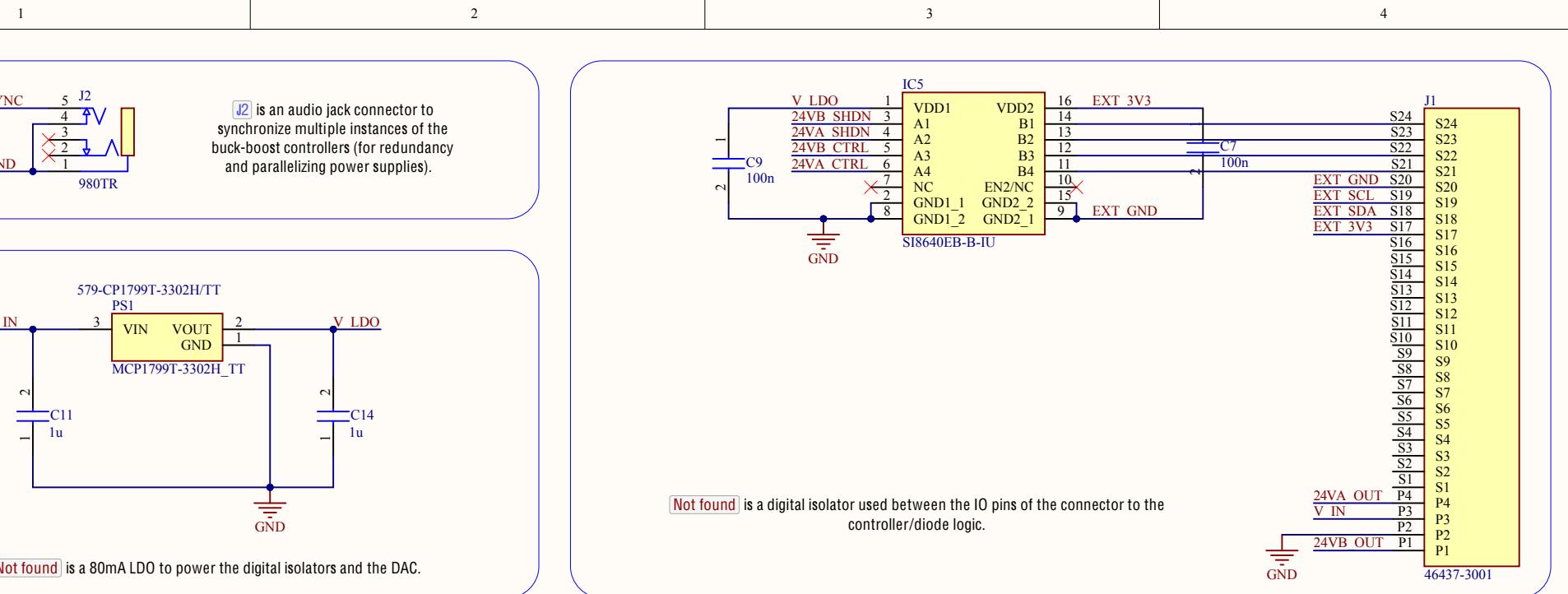




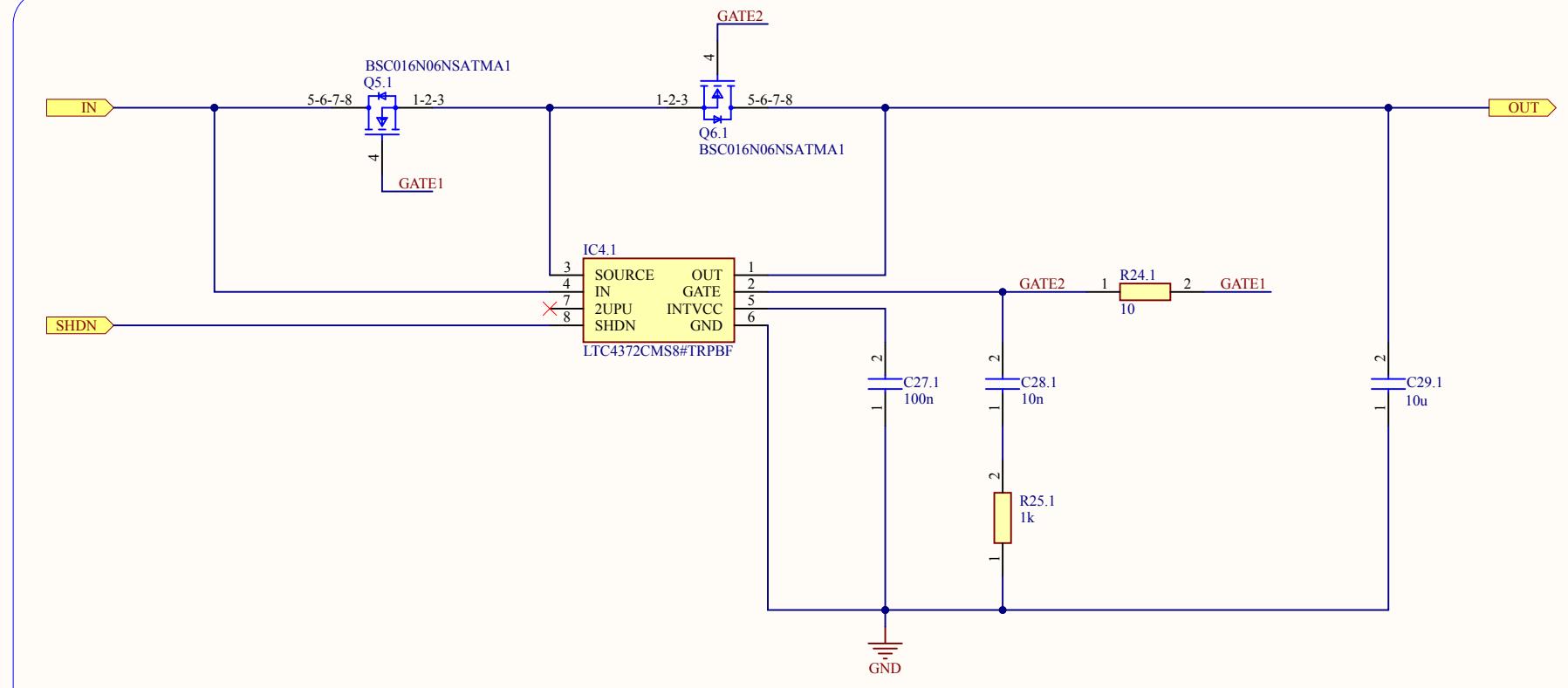


HV Power Module

Buck-boost regulators



A



Title Ideal Diode		
Size A4	Number 1	Revision 1
Date: 4.04.2023	Sheet of EPFL Xplore	
File: \IdealDiode.SchDoc	Drawn By: Arion Zimmermann	

A

A

B

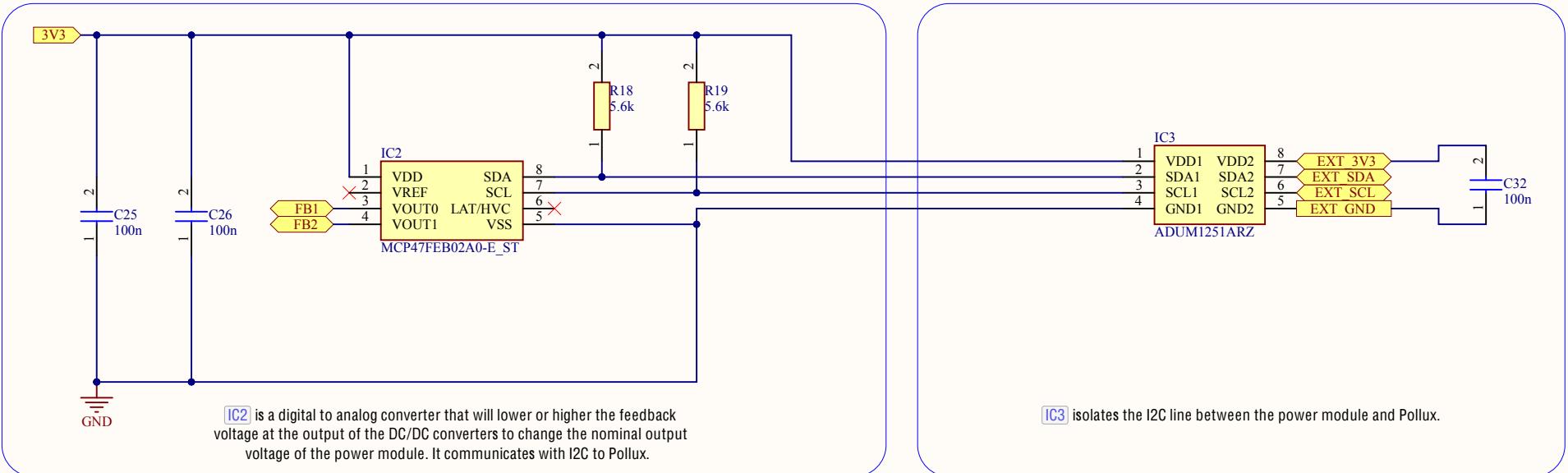
B

C

C

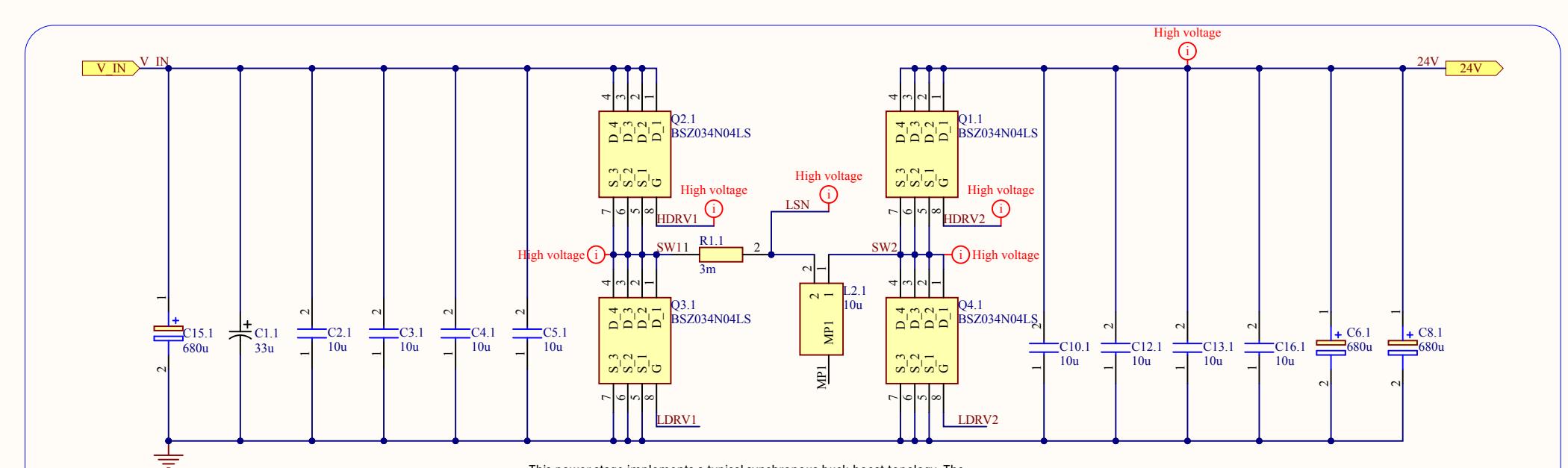
D

D



Title Isolated Digital-to-Analog Converter		
Size A4	Number 1	Revision 1
Date: 4.04.2023	Sheet of EPFL Xplore	
File: \..\DAC.SchDoc	Drawn By: Arion Zimmermann	

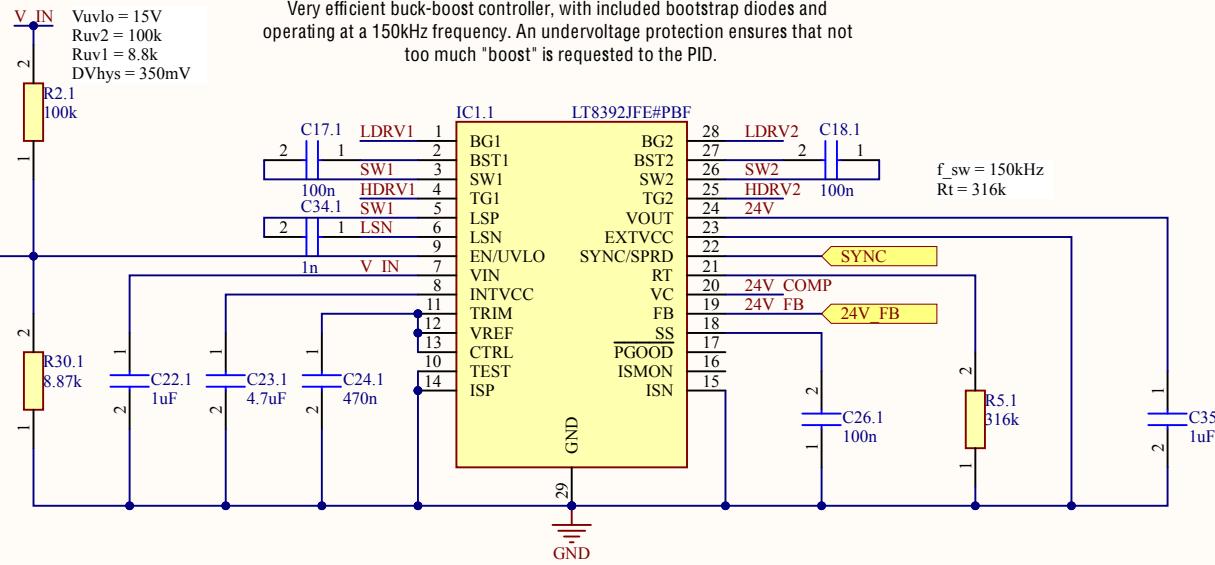
1 2 3 4



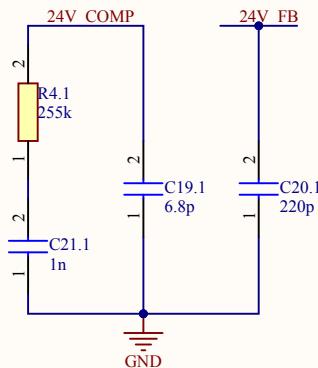
This power stage implements a typical synchronous buck-boost topology. The left part bucks the input voltage, whereas the right part boosts it. Large input/output capacitances ensures that the control system PID remains stable.

V_{IN}
 $V_{UVLO} = 15V$
 $R_{UV2} = 100k$
 $R_{UV1} = 8.8k$
 $DV_{HYS} = 350mV$

Very efficient buck-boost controller, with included bootstrap diodes and operating at a 150kHz frequency. An undervoltage protection ensures that not too much "boost" is requested to the PID.



Title: Power Module Buck-Boost Converter (Nominal 20V:30V -> 24V)
 Size: A4 Number: 1 Revision: 1
 Date: 4.04.2023 Sheet of 1 of EPFL Xplore
 File: \\.\Converter.SchDoc Drawn By: Arion Zimmermann



PID coefficients tuned through LTPowerCAD.

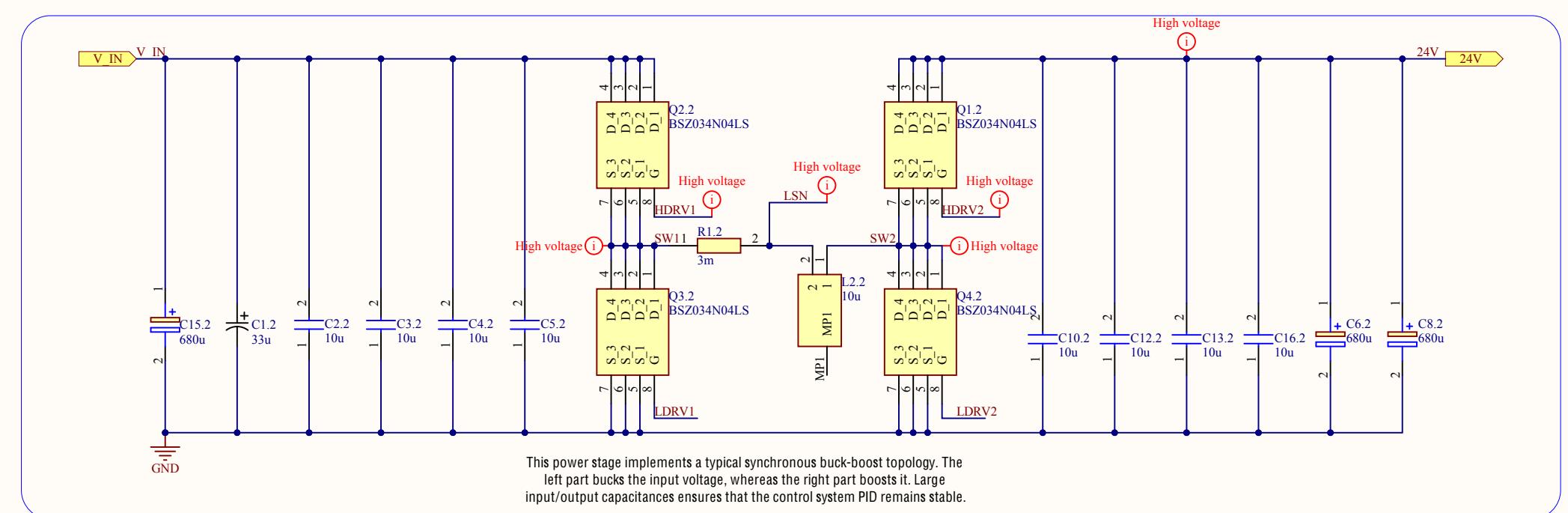
1 2 3 4

1

2

3

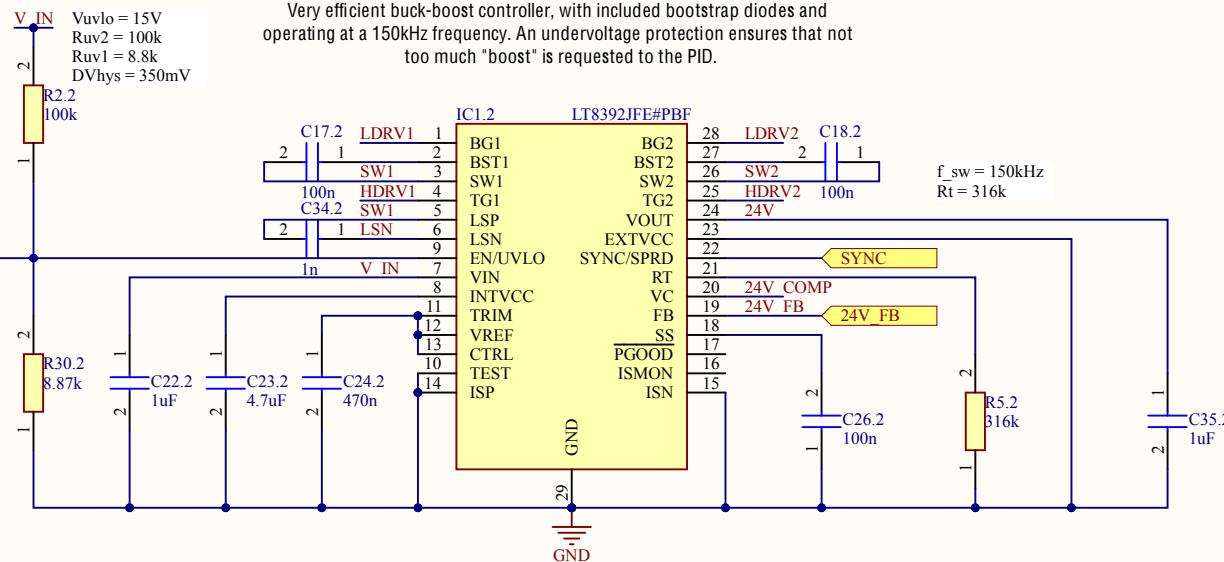
4



V_{IN}
R_{2.2} = 100k
R_{uv2} = 100k
R_{uv1} = 8.8k
DV_{hys} = 350mV

Very efficient buck-boost controller, with included bootstrap diodes and operating at a 150kHz frequency. An undervoltage protection ensures that not too much "boost" is requested to the PID.

C



PID coefficients tuned through LTpowerCAD.
Title: Power Module Buck-Boost Converter (Nominal 20V:30V > 24V)

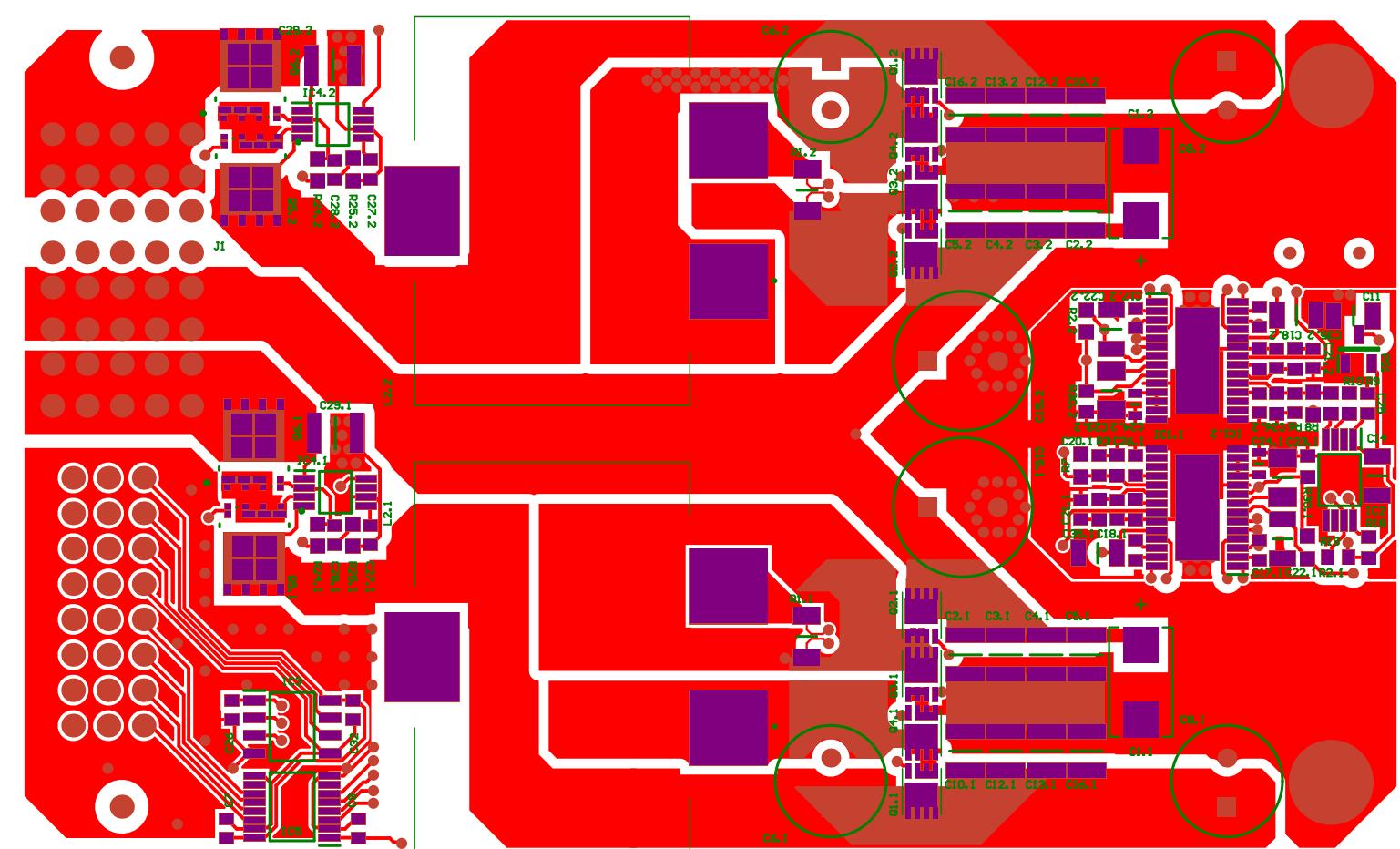
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Date:	4.04.2023	Sheet of EPFL Xplore
File:	\..\Converter.SchDoc	Drawn By: Arion Zimmermann

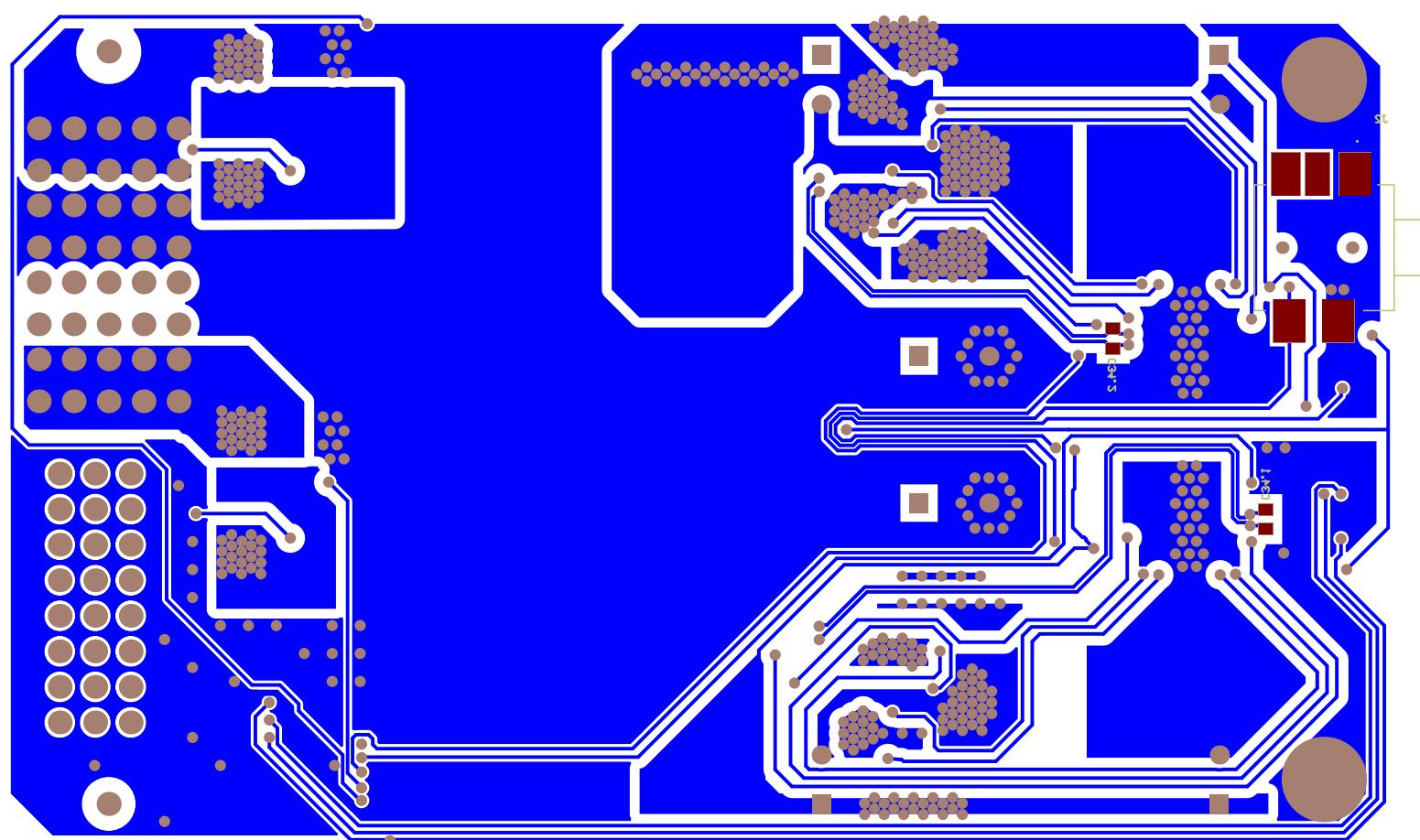
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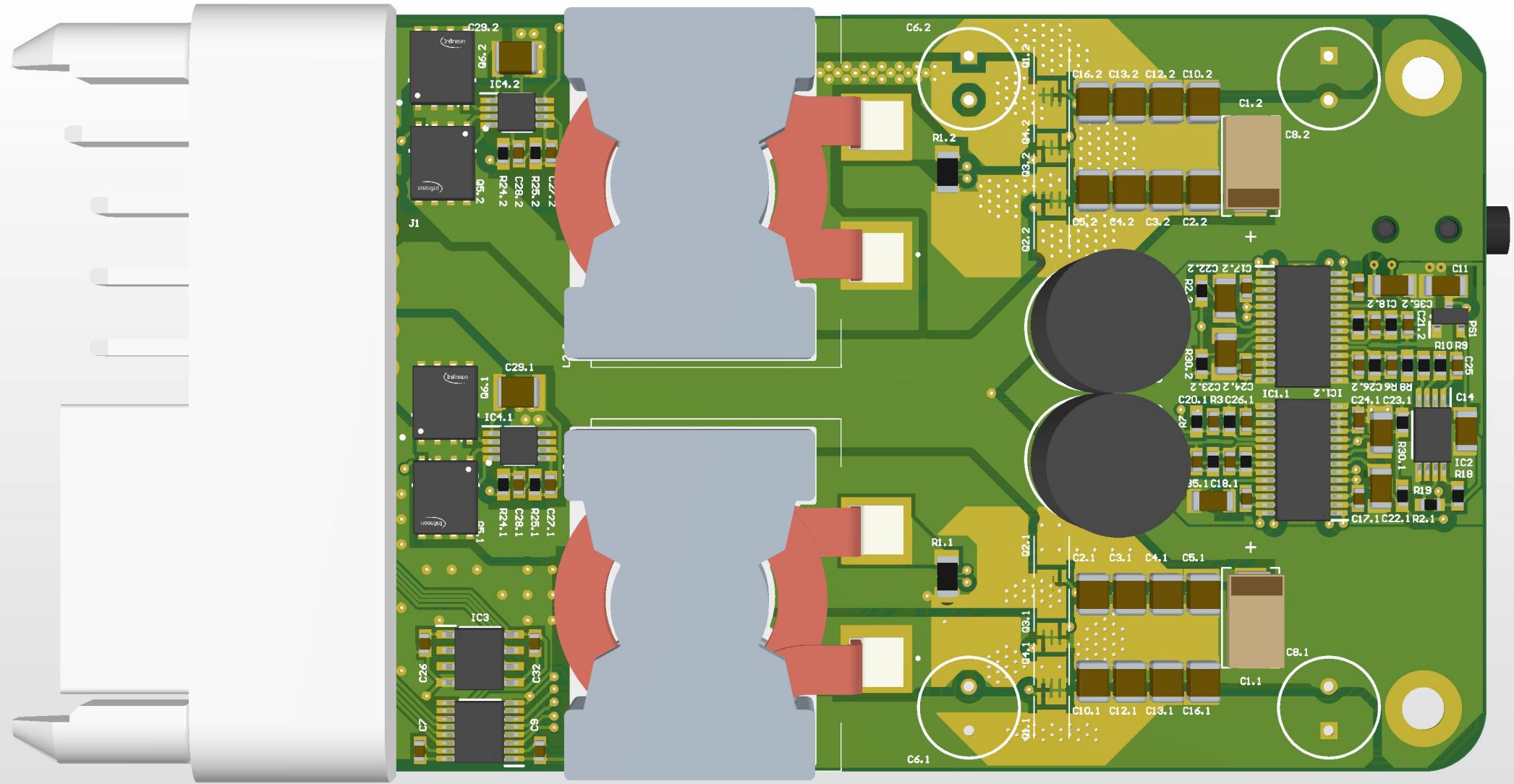
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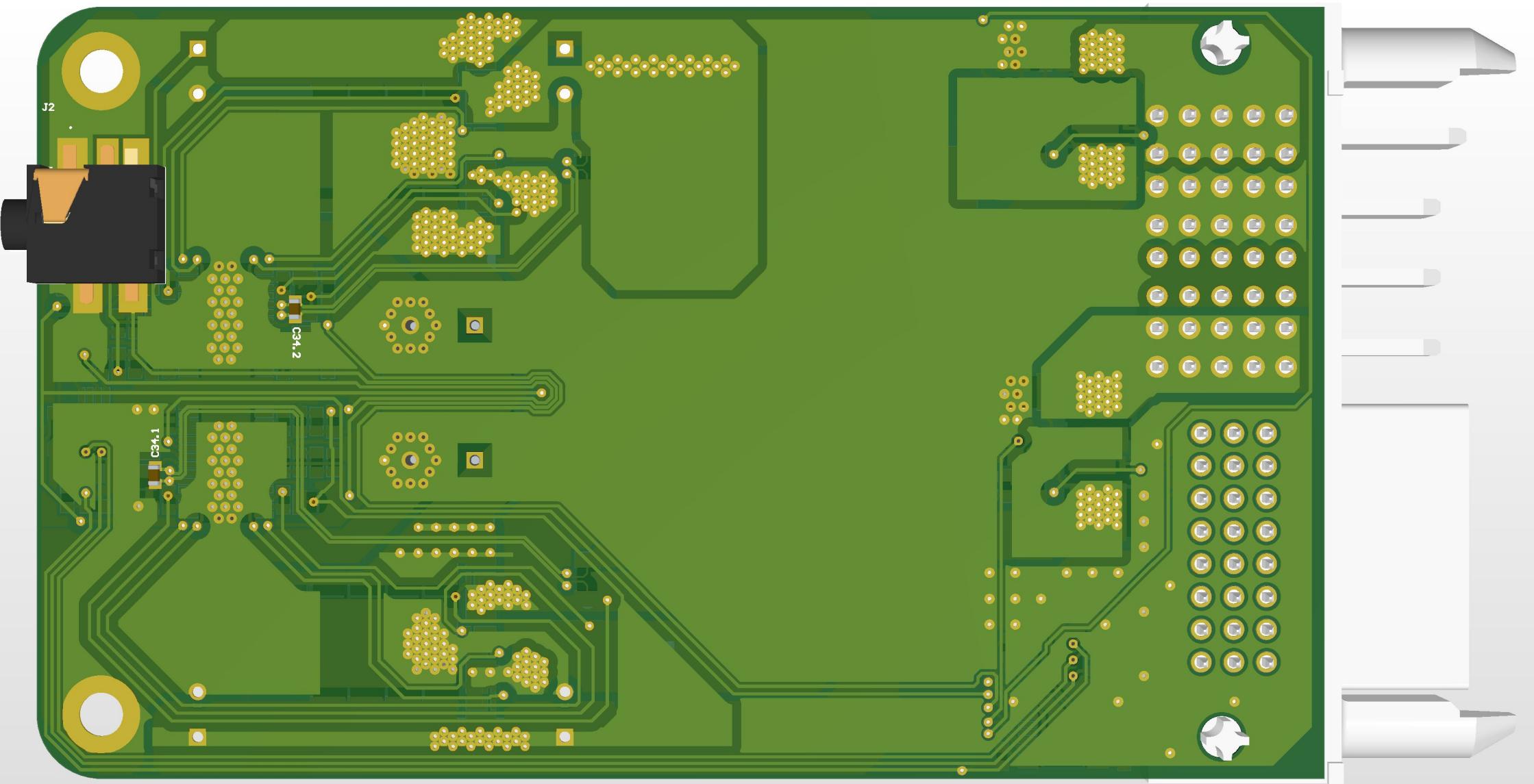
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4



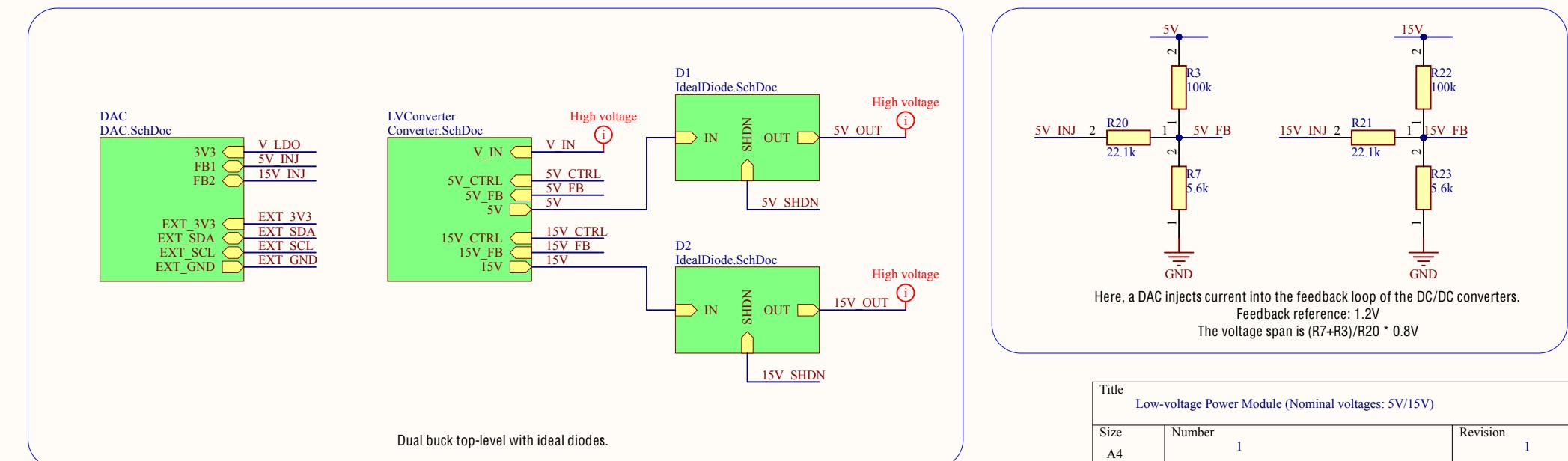
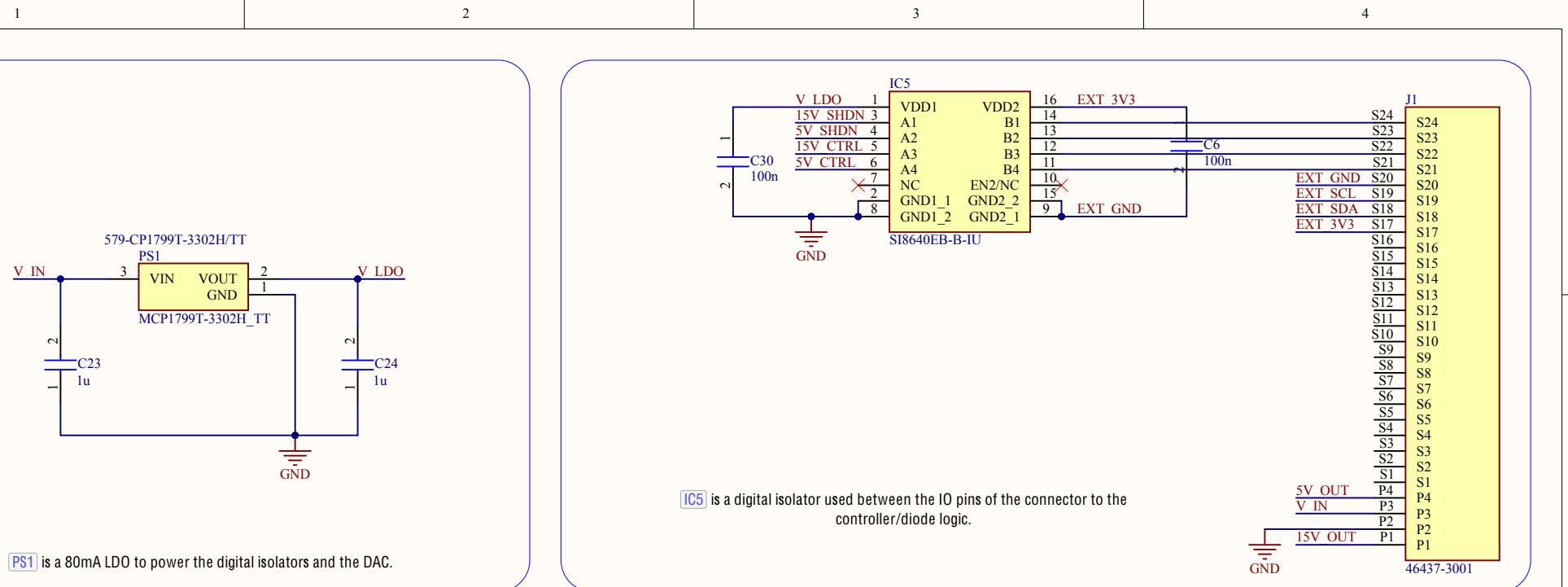


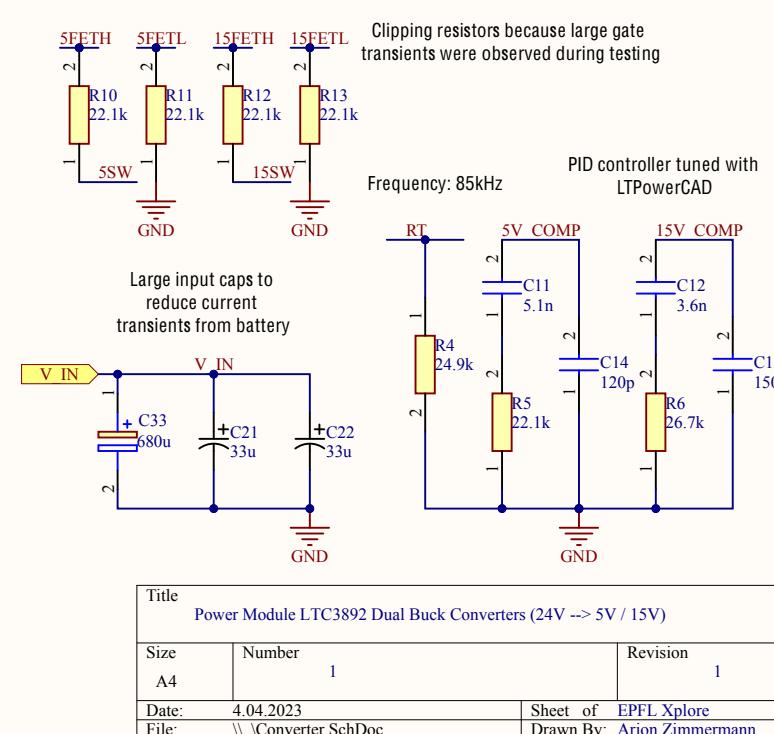
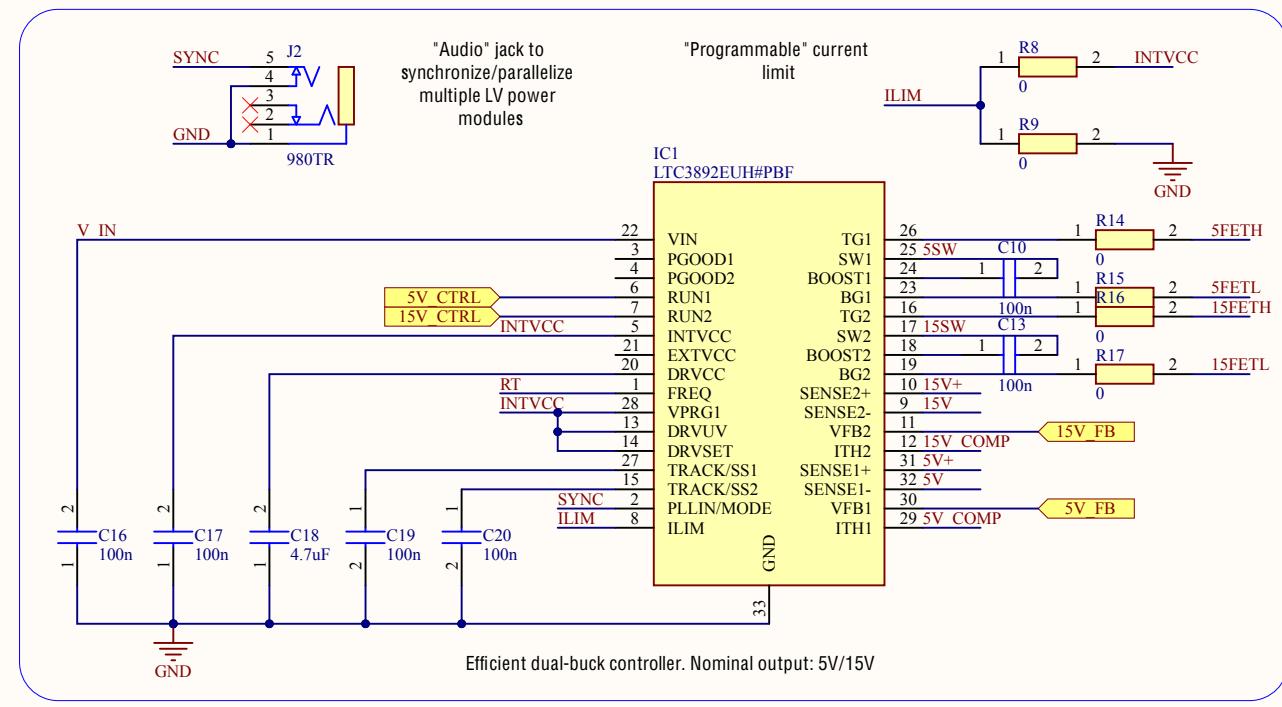
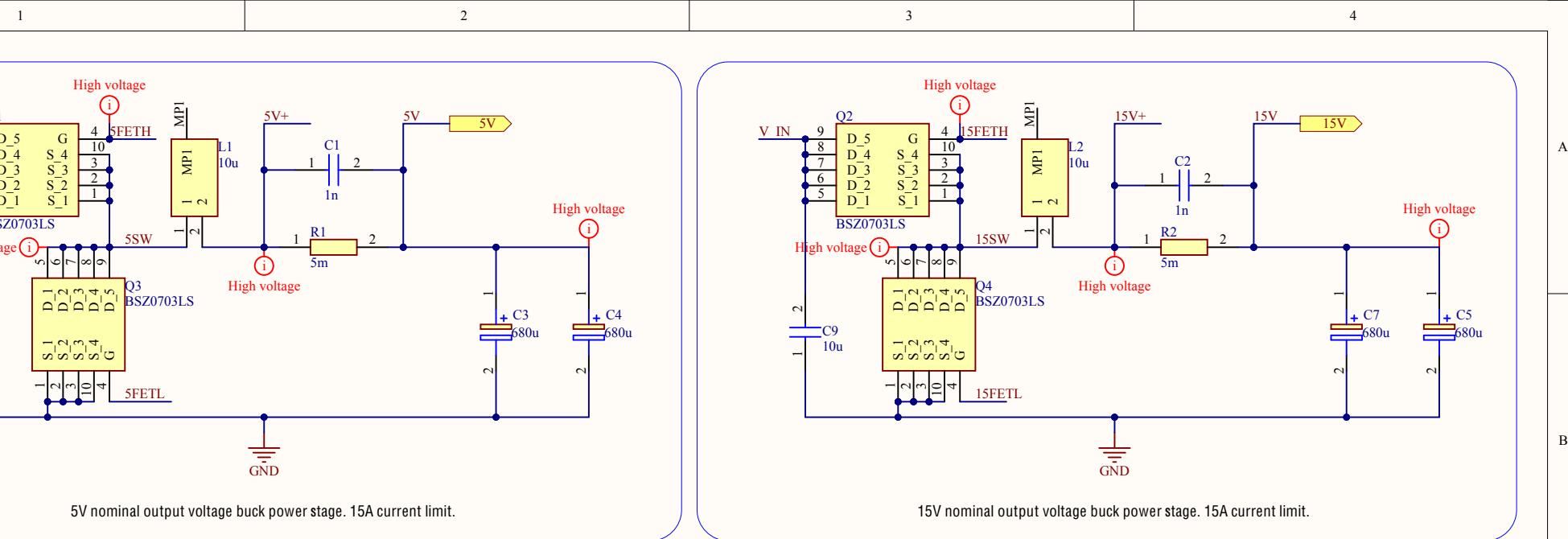




LV Power Module

Buck regulators





A

A

B

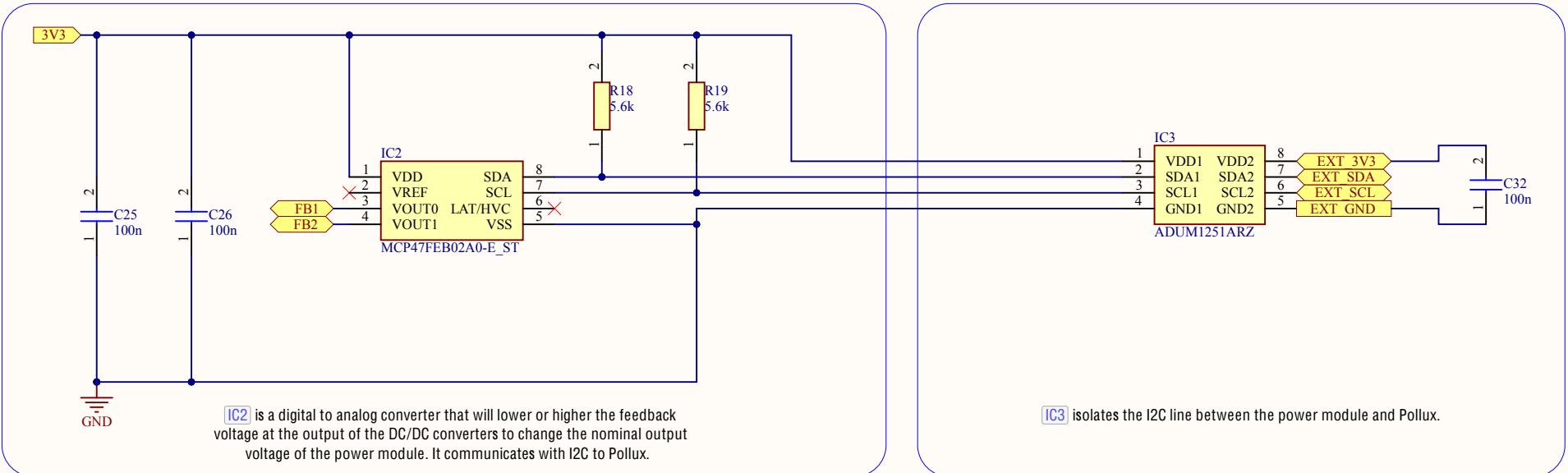
B

C

C

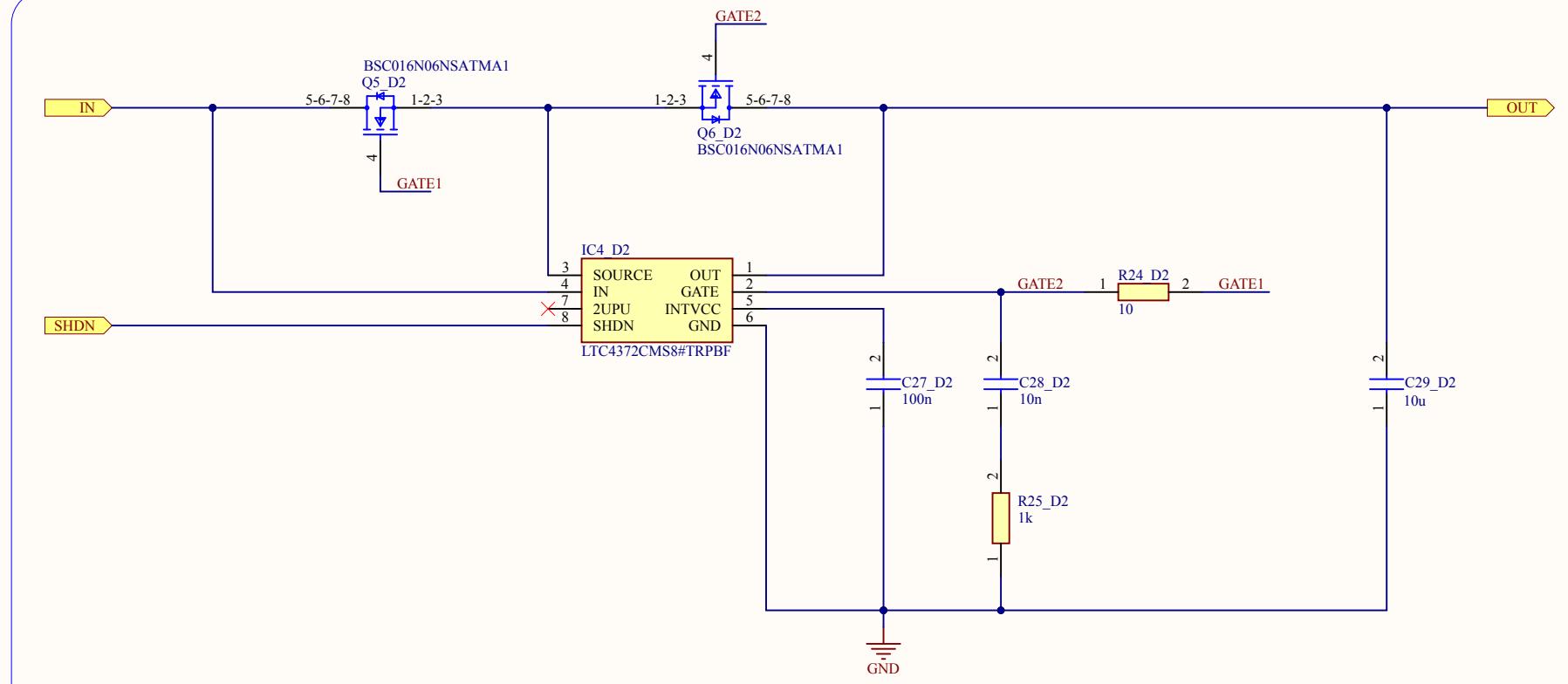
D

D



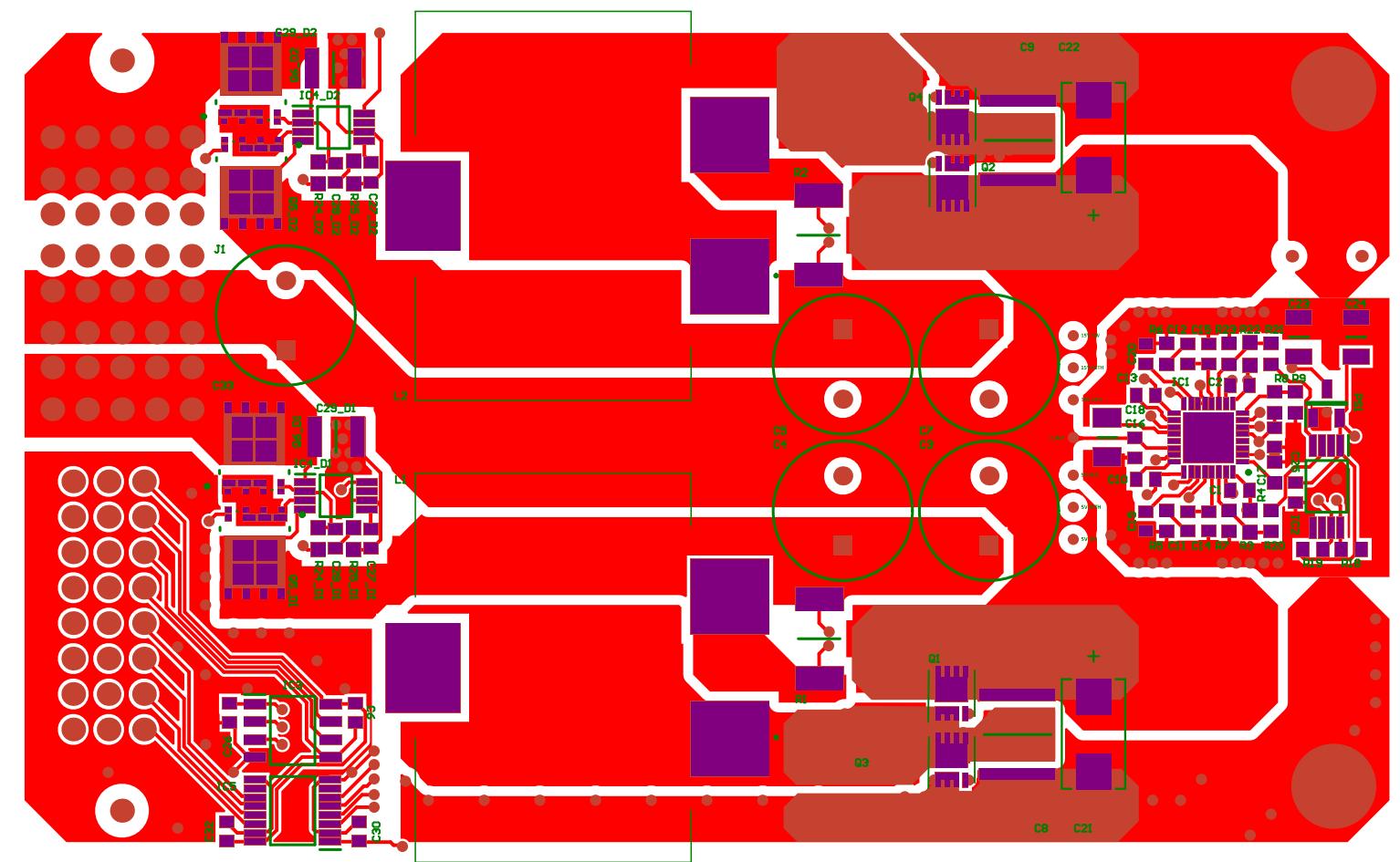
Title Isolated Digital-to-Analog Converter		
Size A4	Number 1	Revision 1
Date: 4.04.2023	Sheet of EPFL Xplore	
File: \..\DAC.SchDoc	Drawn By: Arion Zimmermann	

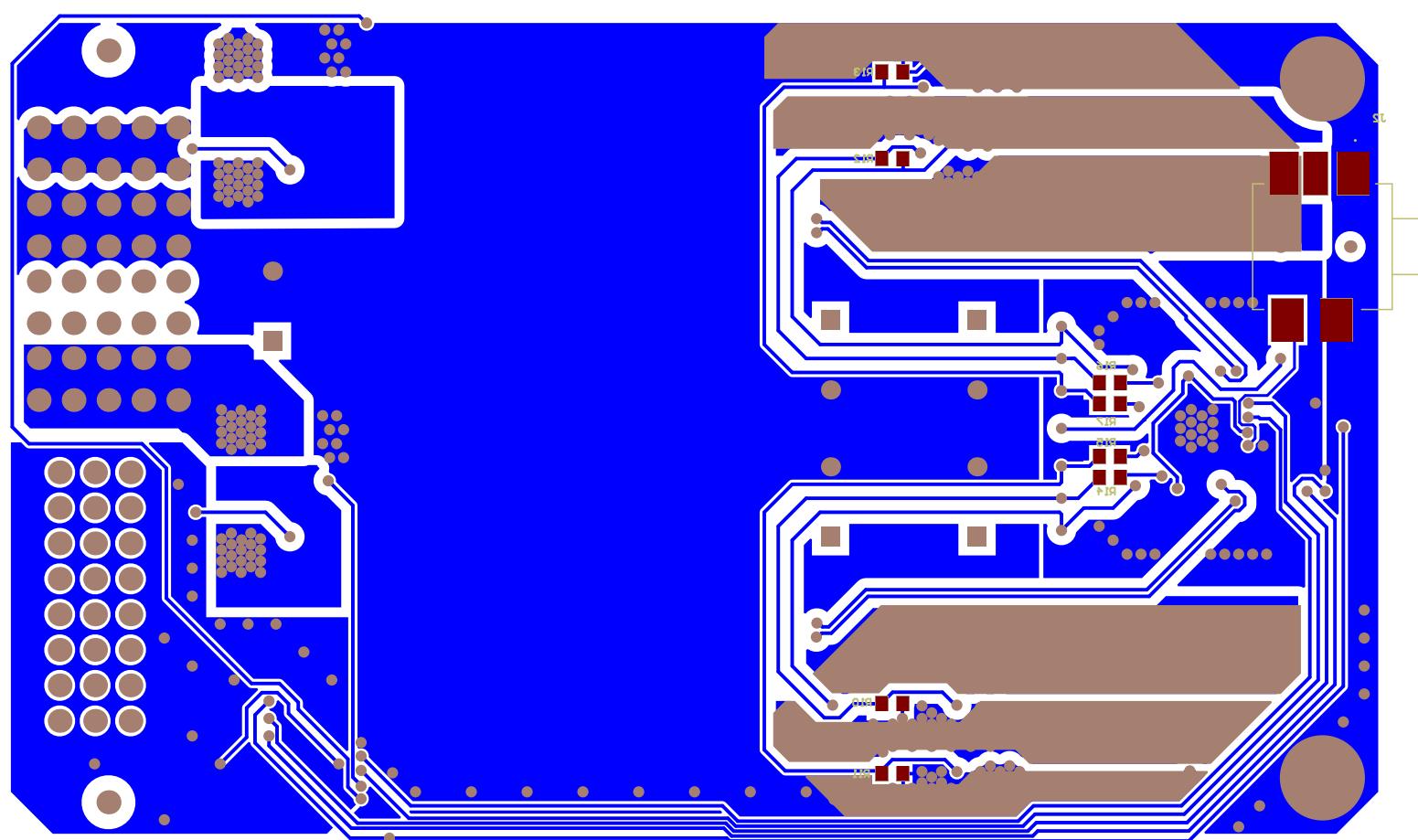
A

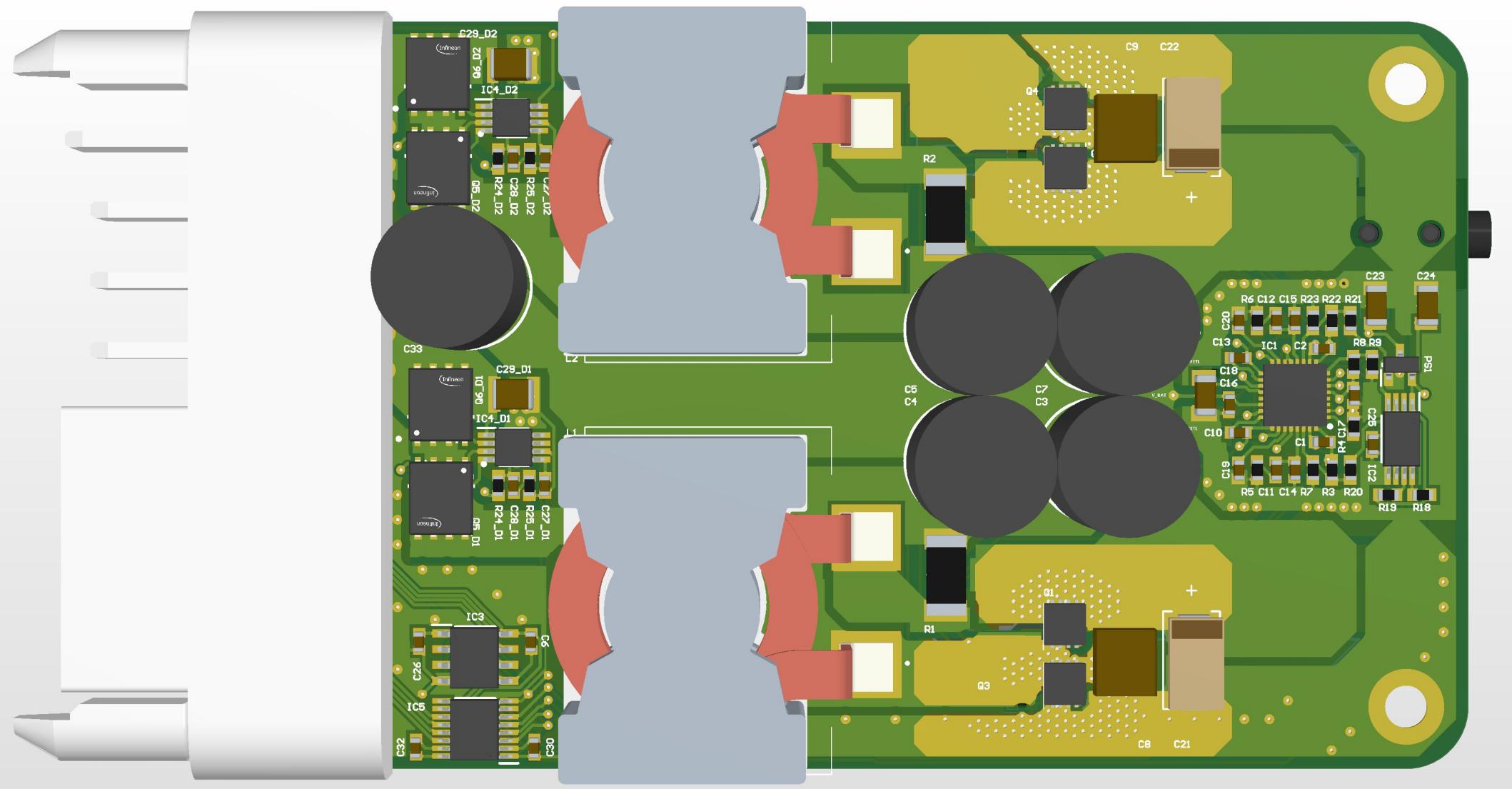


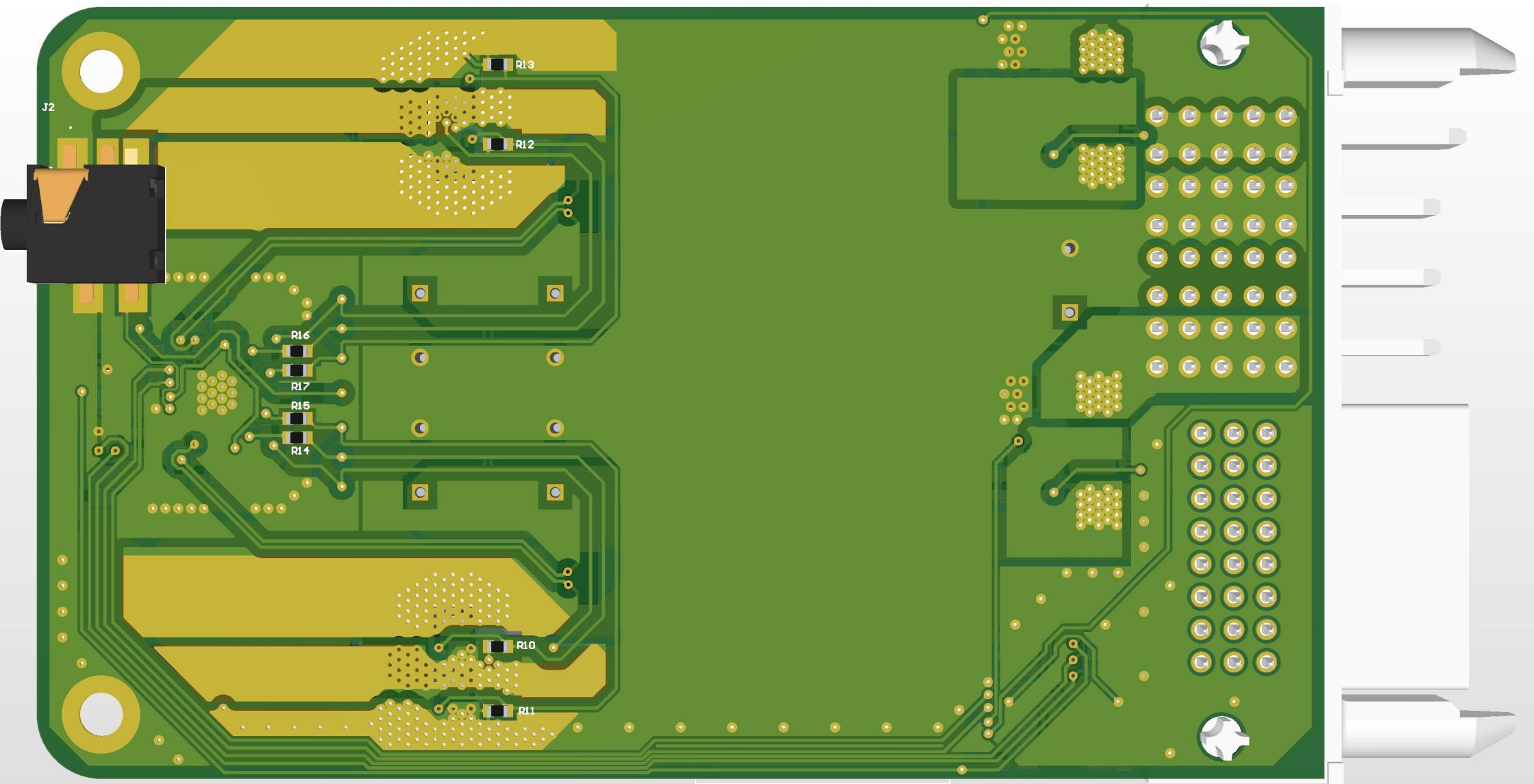
The two MOSFETs **Q5** and **Q6** control the current from the DC/DC converter and the load. Having an output voltage higher than the input voltage will trigger the **IC4** ideal diode controller to disconnect the DC/DC converter from the load line. Some care was taken to reduce transients on the gate pin.

Title Ideal Diode		
Size A4	Number 1	Revision 1
Date: 4.04.2023	Sheet of EPFL Xplore	
File: \IdealDiode.SchDoc	Drawn By: Arion Zimmermann	





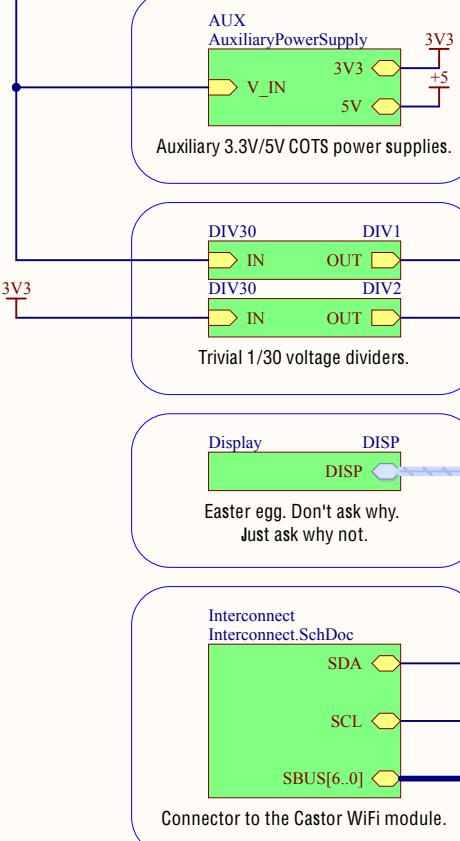
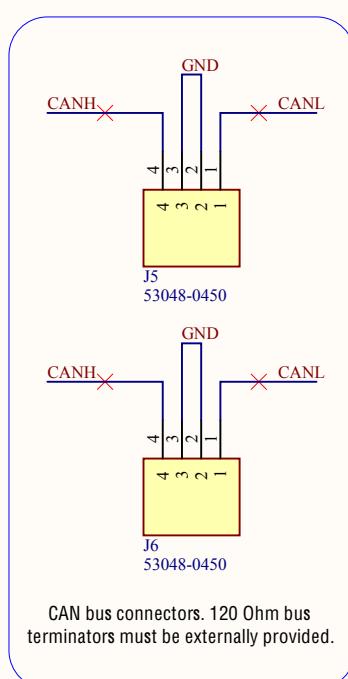
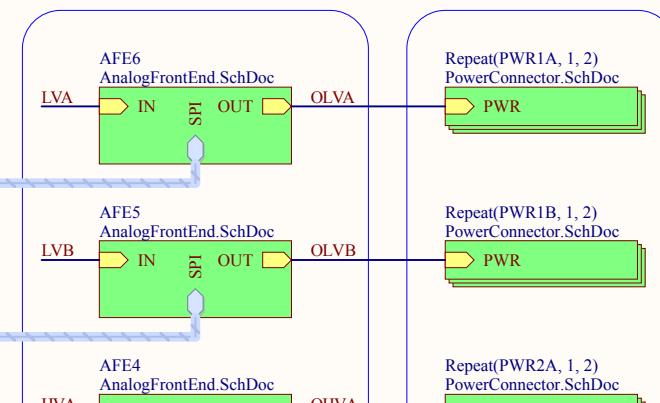
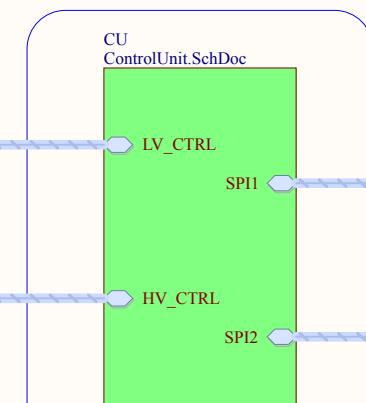
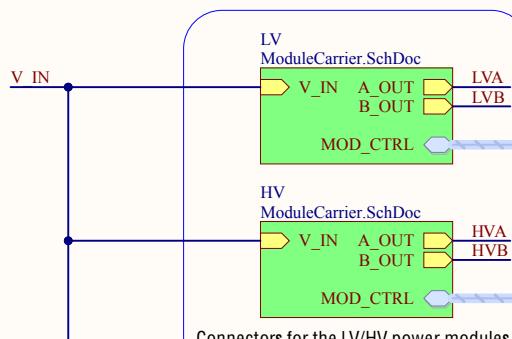
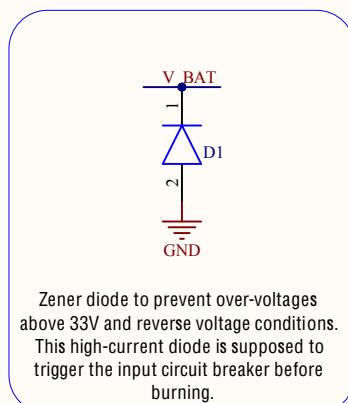




Pollux III

Motherboard

1 2 3 4



Title
Pollux III Top Level

Size	Number	Revision
A4	1	1
Date:	4.04.2023	Sheet of EPFL Xplore
File:	\..\TopLevel.SchDoc	Drawn By: Arion Zimmermann

1 2 3 4

A

A

B

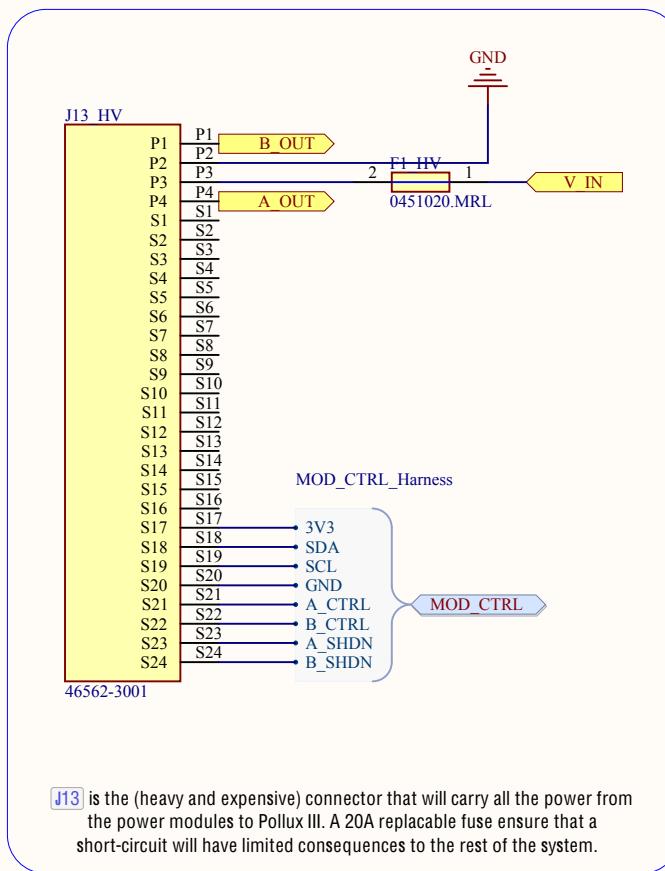
B

C

C

D

D



Title		
Interface to the Power Modules		
Size	Number	Revision
A4	1	1
Date:	4.04.2023	Sheet of EPFL Xplore
File:	\..\ModuleCarrier.SchDoc	Drawn By: Arion Zimmermann

A

A

B

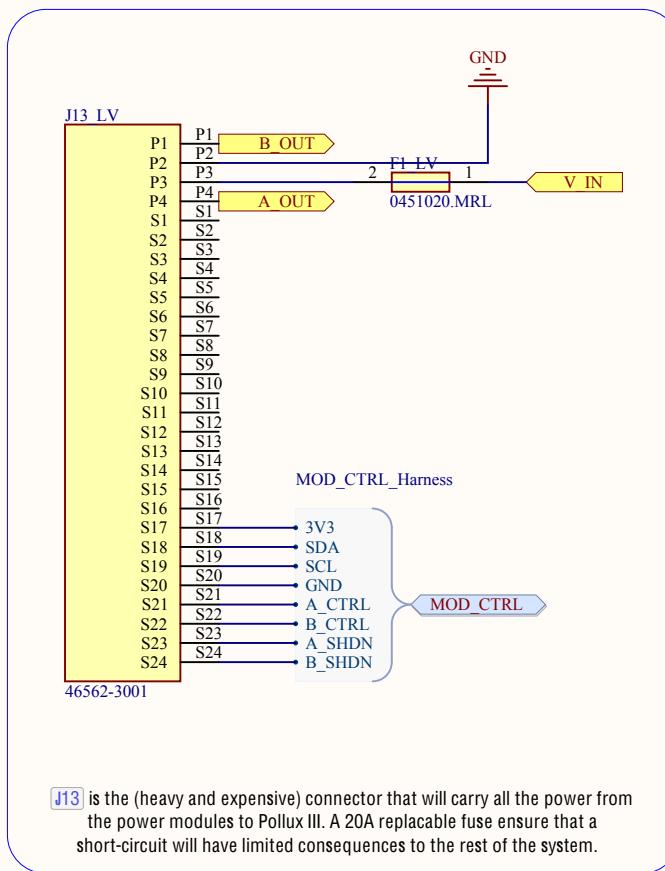
B

C

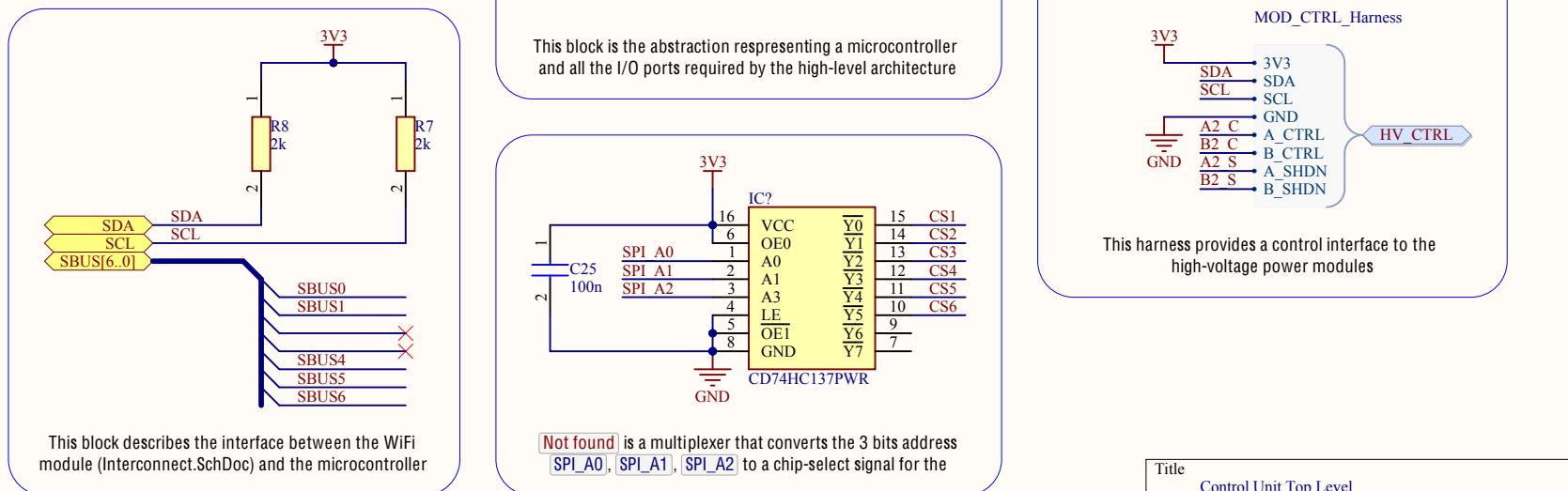
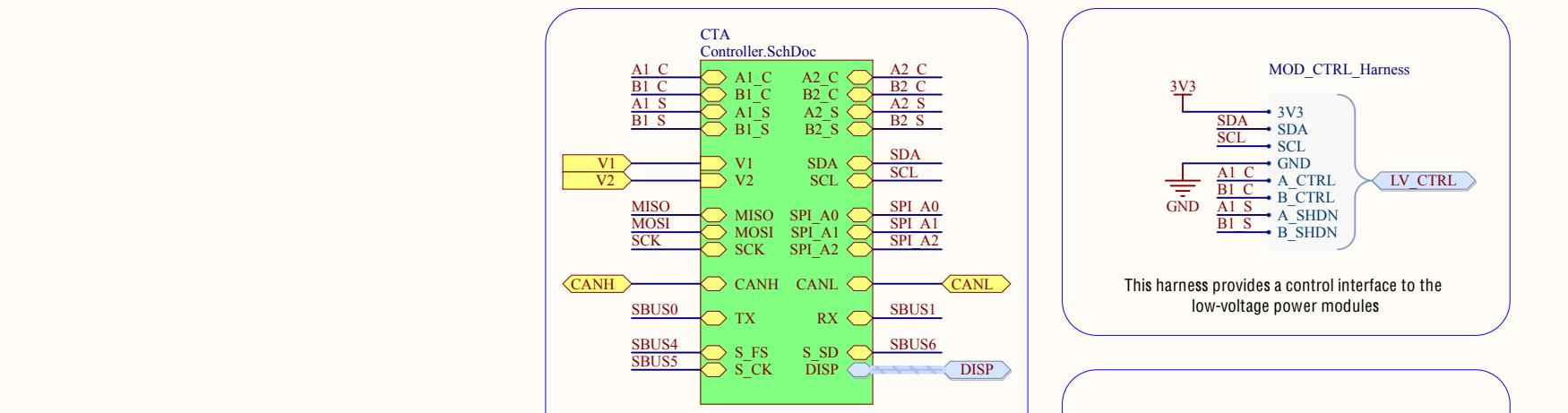
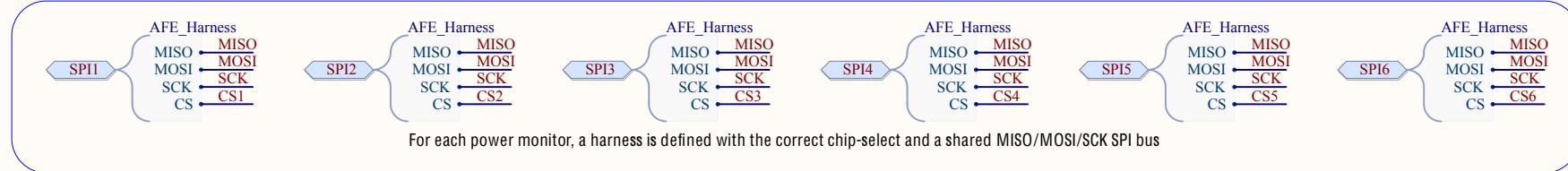
C

D

D



Title		
Interface to the Power Modules		
Size	Number	Revision
A4	1	1
Date:	4.04.2023	Sheet of EPFL Xplore
File:	\..\ModuleCarrier.SchDoc	Drawn By: Arion Zimmermann



Title: Control Unit Top Level

Size	Number	Revision
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Date:	4.04.2023	Sheet of EPFL Xplore
File:	\ControlUnit.SchDoc	Drawn By: Arion Zimmermann

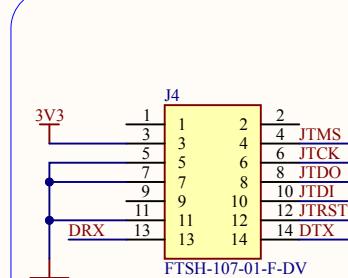
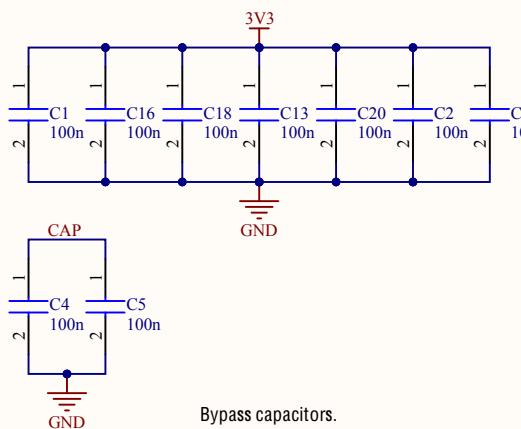
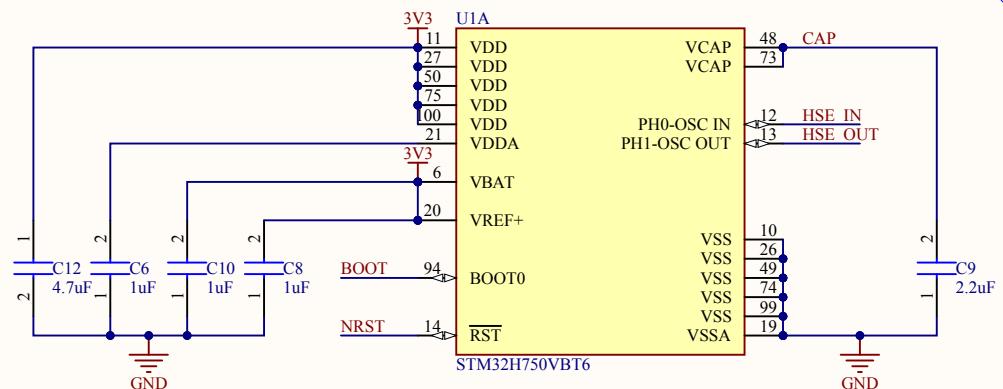
1

2

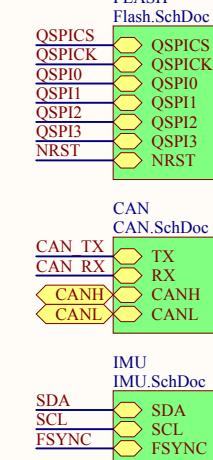
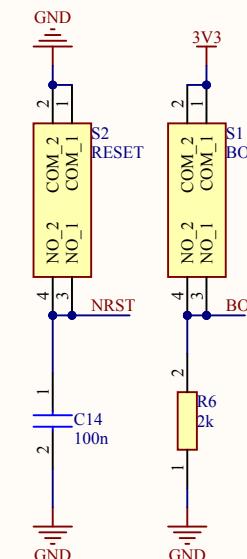
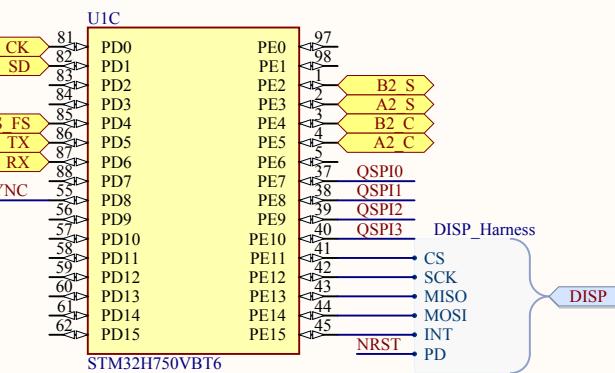
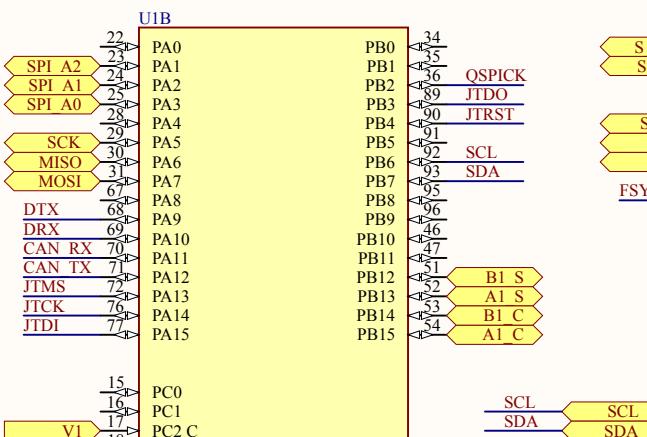
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4

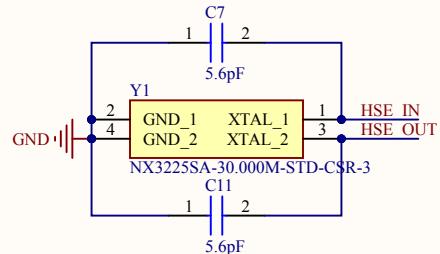
A



B



C



Title: Digital Signal Processor (STM32H750VBT6)

Size	Number	Revision
A4	1	1
Date:	4.04.2023	Sheet of EPFL Xplore
File:	\Controller.SchDoc	Drawn By: Arion Zimmermann

1

2

3

4

A

A

B

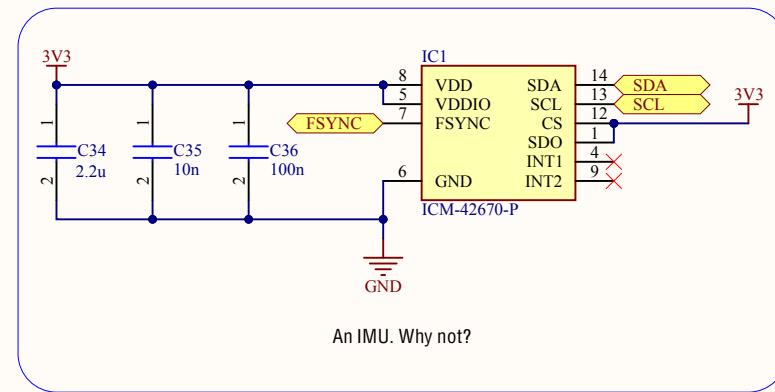
B

C

C

D

D



Title IMU		
Size A4	Number 1	Revision 1
Date: 4.04.2023	Sheet of EPFL Xplore	
File: \IMU.SchDoc	Drawn By: Arion Zimmermann	

A

A

B

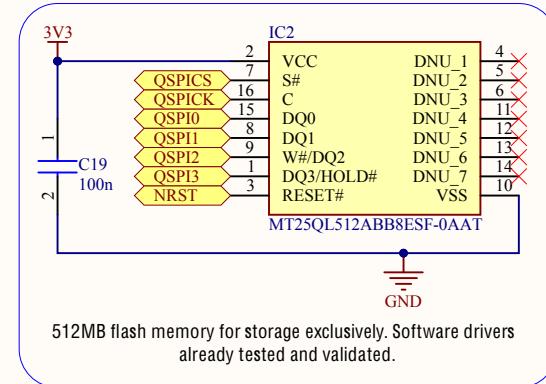
B

C

C

D

D



Title Flash Memory		
Size A4	Number 1	Revision 1
Date: 4.04.2023	Sheet of EPFL Xplore	
File: \.\Flash.SchDoc	Drawn By: Arion Zimmermann	

A

A

B

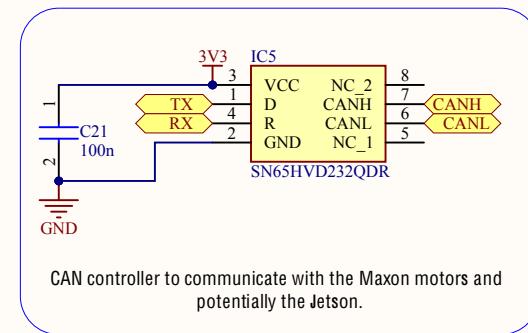
B

C

C

D

D



Title CAN Bus Controller		
Size A4	Number 1	Revision 1
Date: 4.04.2023	Sheet of EPFL Xplore	
File: \..\CAN.SchDoc	Drawn By: Arion Zimmermann	

A

A

B

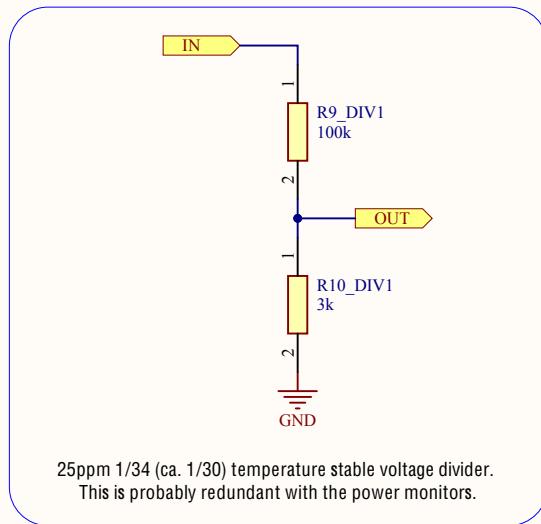
B

C

C

D

D



Title 1/30 Stable Voltage Divider		
Size A4	Number 1	Revision 1
Date: 4.04.2023	Sheet of EPFL Xplore	
File: \DIV30.SchDoc	Drawn By: Arion Zimmermann	

A

A

B

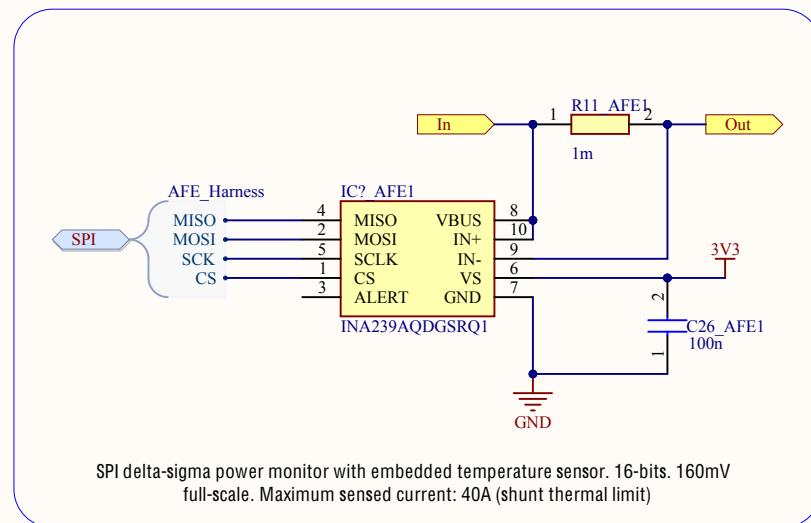
B

C

C

D

D



Title		
Power Monitor		
Size	Number	Revision
A4	1	1
Date:	4.04.2023	Sheet of EPFL Xplore
File:	\.\.\AnalogFrontEnd.SchDoc	Drawn By: Arion Zimmermann

A

A

B

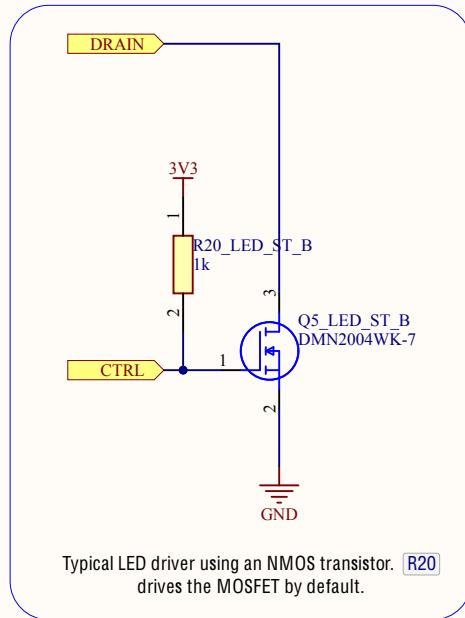
B

C

C

D

D



Title		
LED Driver		
Size	Number	Revision
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Date:	4.04.2023	Sheet of EPFL Xplore
File:	\..\LED.SchDoc	Drawn By: Arion Zimmermann

A

A

B

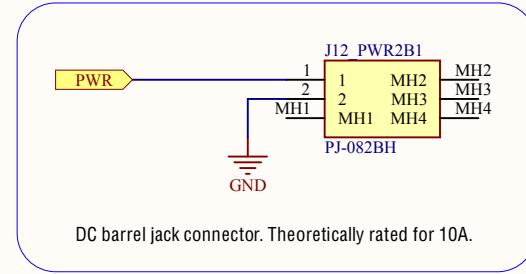
B

C

C

D

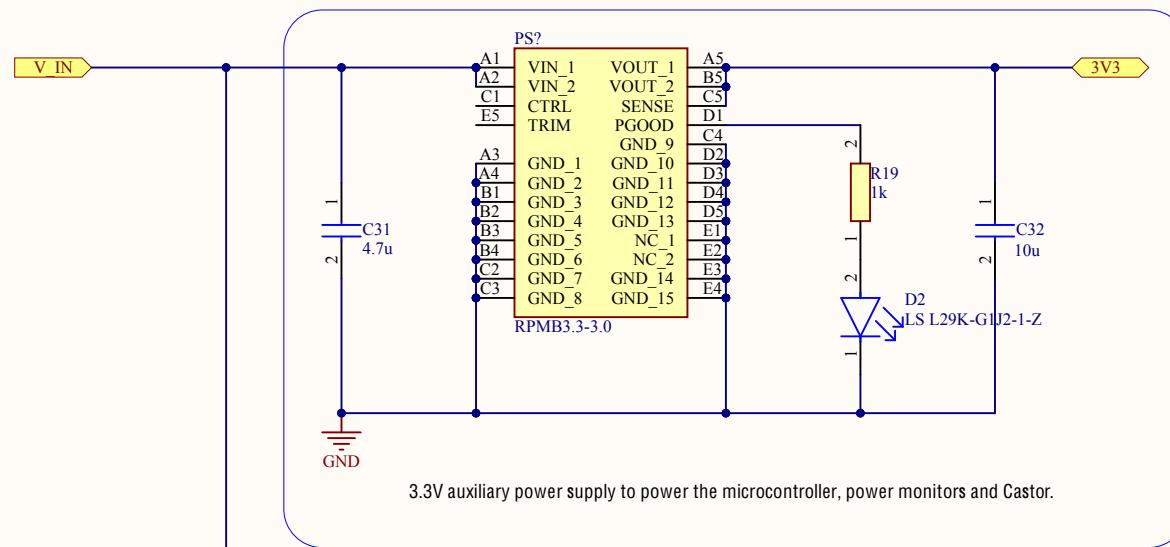
D



Title Power Connector		
Size A4	Number 1	Revision 1
Date: 4.04.2023	Sheet of EPFL Xplore	
File: \.\PowerConnector.SchDoc	Drawn By: Arion Zimmermann	

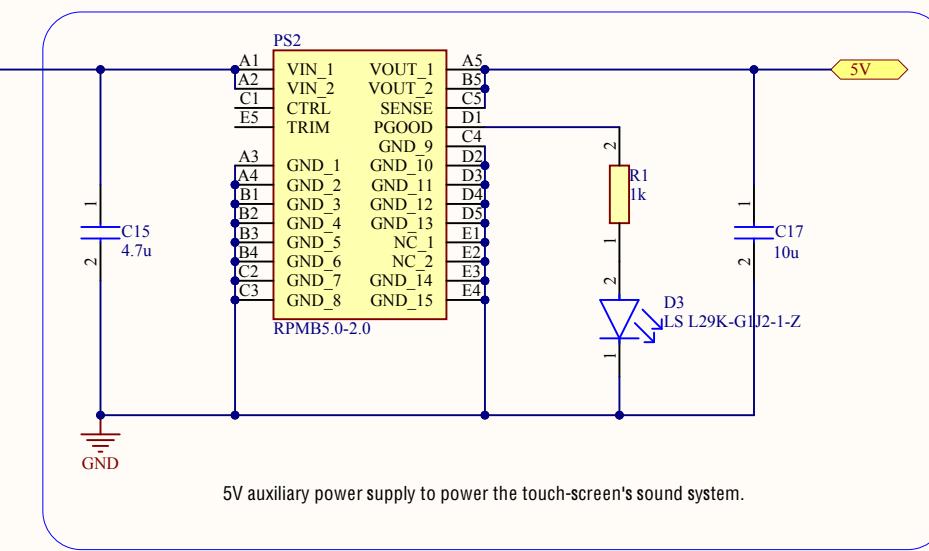
A

A



B

B



C

C

D

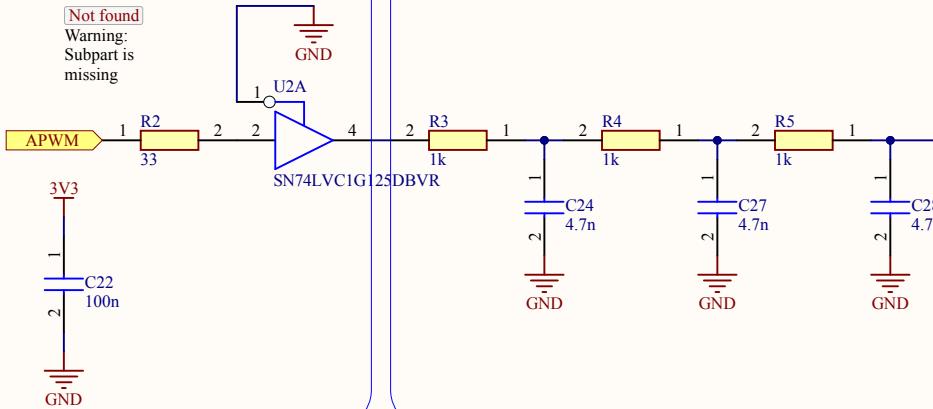
D

Title		Auxiliary Power Supplies
Size A4	Number 1	Revision 1
Date: 4.04.2023	Sheet of DC/DC converters	
File: \AuxiliaryPowerSupply.SchDoc	Drawn By:	Arion Zimmermann

A

A

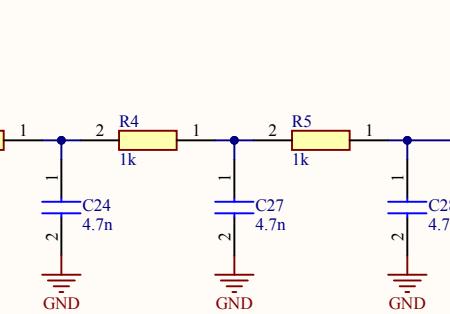
Pre-amplifier



B

B

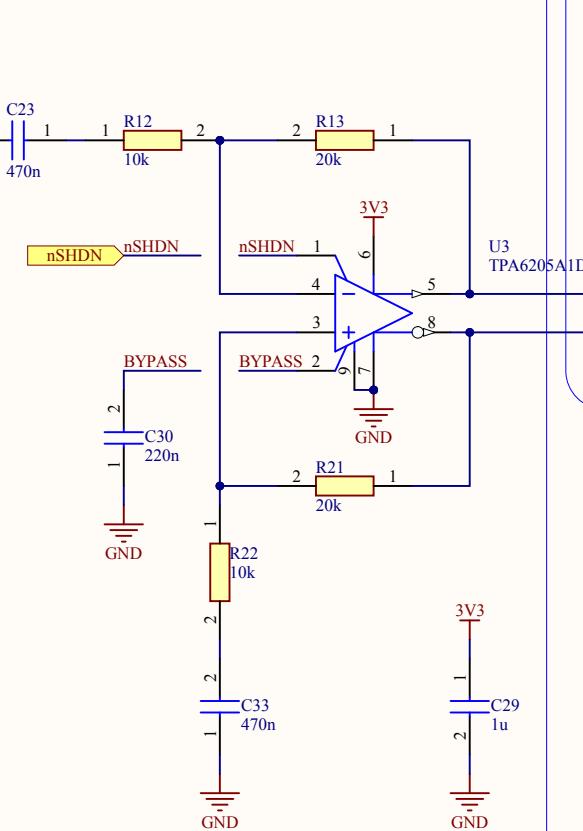
60dB RC low-pass at 33kHz cut-off



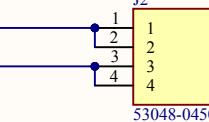
C

C

60dB RC low-pass at 33kHz cut-off



Output molex micro-fit connector



Title Audio Amplifier		
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Size A4	Number 1	Revision 1
Date: 4.04.2023	Sheet of EPFL Xplore	
File: \..\Audio.SchDoc	Drawn By: Arion Zimmermann	

