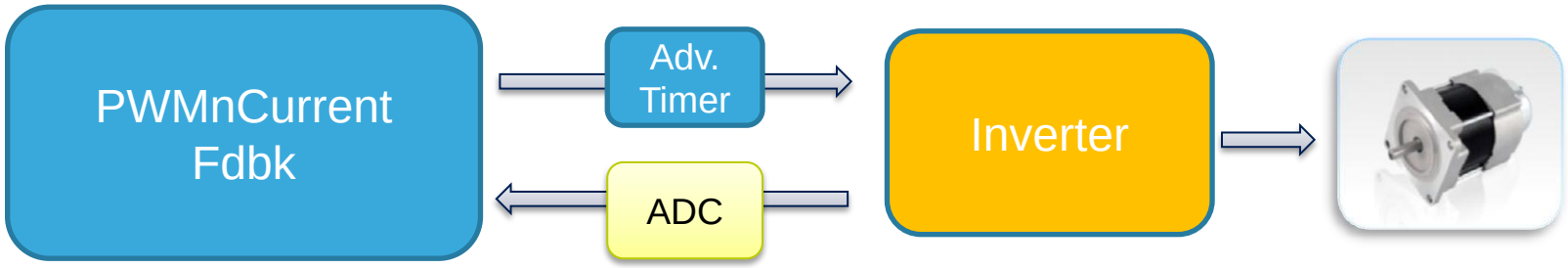
Agenda

- 1st day – Afternoon
  - MC Application
    - Interface
    - Tuning
    - Tasks
    - Classes interaction
      - Current regulation
      - Ramp-up
      - Encoder alignment
  - Speed sensors updates:
    - Sensorless algorithm improvement
  - How to create User Project Interacting with MC Application
  - Dual motor control
    - Resources sharing
    - Supported configurations
    - Code size efficiency
  - Current reading sensor update

PWMnCurrentFdbk description

- A PWMnCurrentFdbk object manages to generate the six PWM outputs and to get the motor current feedbacks.
- It is one of the most hardware-linked objects. The hardware related management (advanced timer, analog to digital converter, etc…) is implemented in the specific derivates.



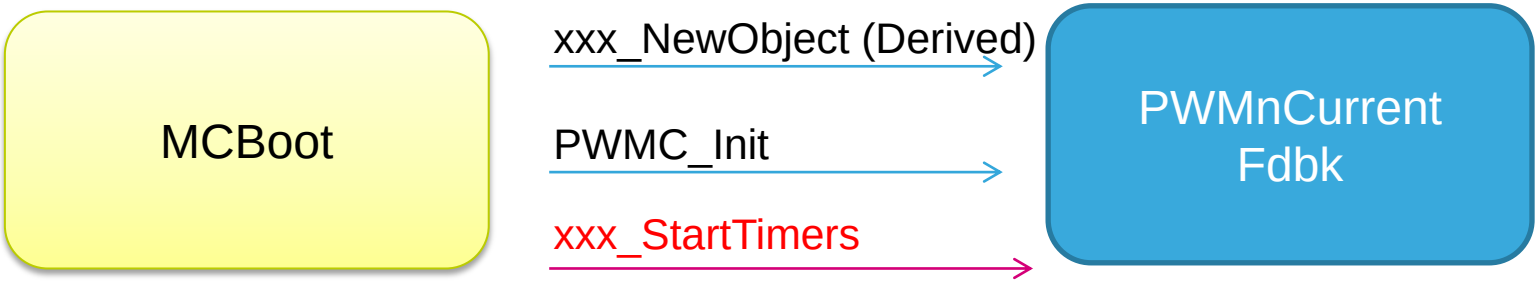
PWMnCurrentFdbk derivates

- Nomenclature

Derivate name	Current reading methodology	Drive architecture	Device
R1_LM1	Single shunt	Single drive	STM32 low and medium density
R1_VL1	Single shunt	Single drive	STM32 value line
R1_HD2	Single shunt	Dual drive	STM32 high density
R3_LM1	Three shunts	Single drive	STM32 low and medium density
R3_HD2	Three shunts	Dual drive	STM32 high density
ICS_LM1	Insulated current sensors	Single drive	STM32 low and medium density
ICS_HD2	Insulated current sensors	Dual drive	STM32 high density

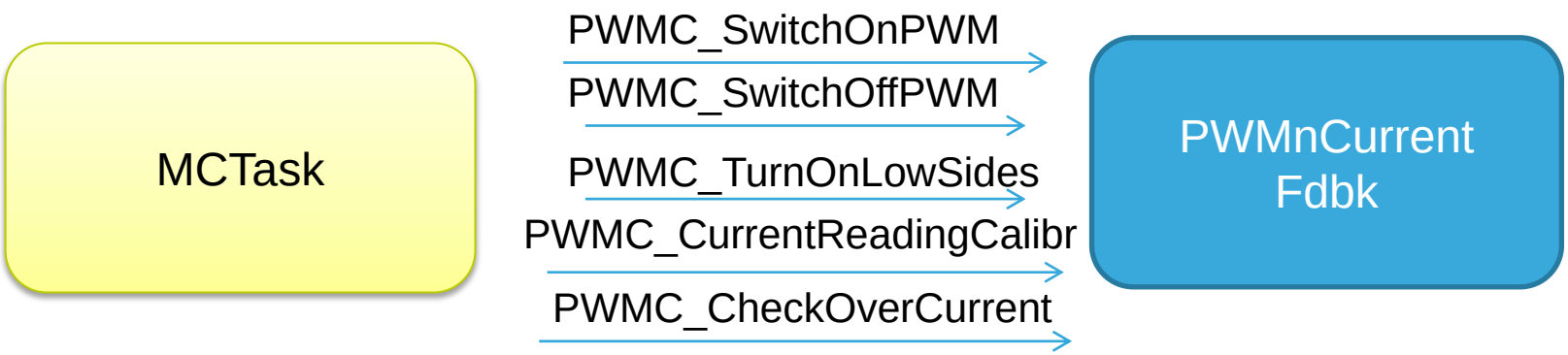
PWMnCurrentFdbk API description

- MCboot creates and initialize all the objects.
- In this case calls the derived class constructor (xxx_NewObject) passing the appropriate parameters. Base class constructor is hidden.
- Then call the object initializer (PWMC_Init).
- For dual drive configuration is required to call derived class StartTimer method. It must be call after both object are instantiated.



PWMnCurrentFdbk API description

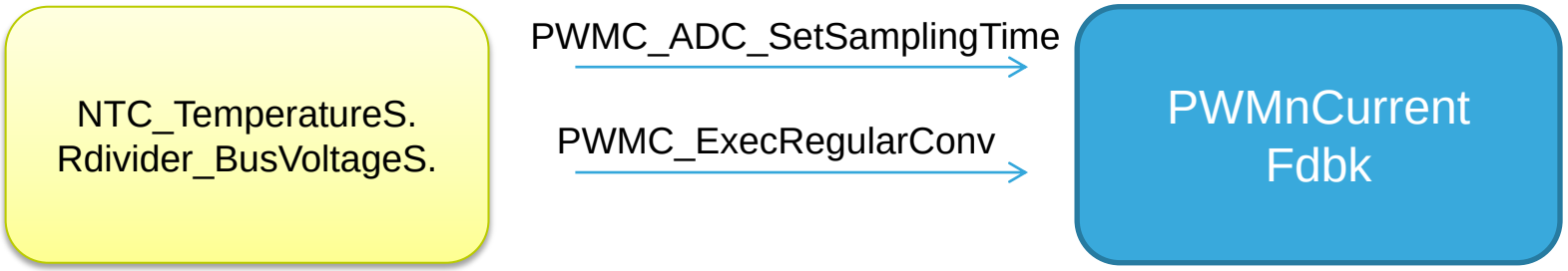
- MCTasks make use of PWMnCurrentFdbk to:
  - LF tasks and safety tasks switches on and off the PWM output (PWMC_SwitchOnPWM, PWM_SwitchOffPWM).
  - LF task turns on the low side to charge boot capacitor or to implement an active brake (PWMC_TurnOnLowSides).
  - LF task reads the offset voltage present on ADC pins when no motor current is flowing to calibrate the phase motor current measurement block (PWMC_CurrentReadingCalibr).
  - Safety task checks if an overcurrent occurred since last all (PWMC_CheckOverCurrent).



PWMnCurrentFdbk API description

- Other MC object like NTC_TemperatureSensor or Rdivider_BusVoltageSensor make use of PWMnCurrentFdbk to program and execute regular analog to digital conversions. (PWMC_ADC_SetSamplingTime, PWMC_ExecRegularConv.)

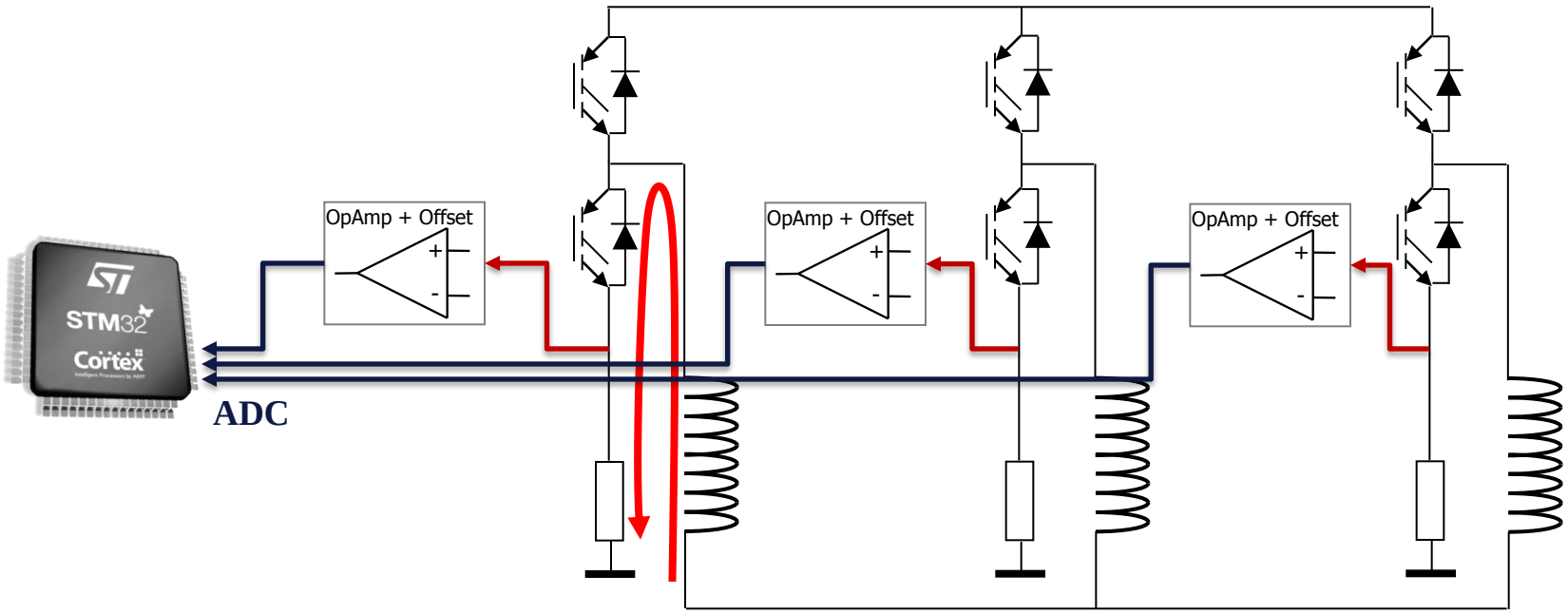
- User can make use of PWMnCurrentFdbk (throught MC_Tuning) to program and execute customized regular analog to digital conversions.



Three shunts

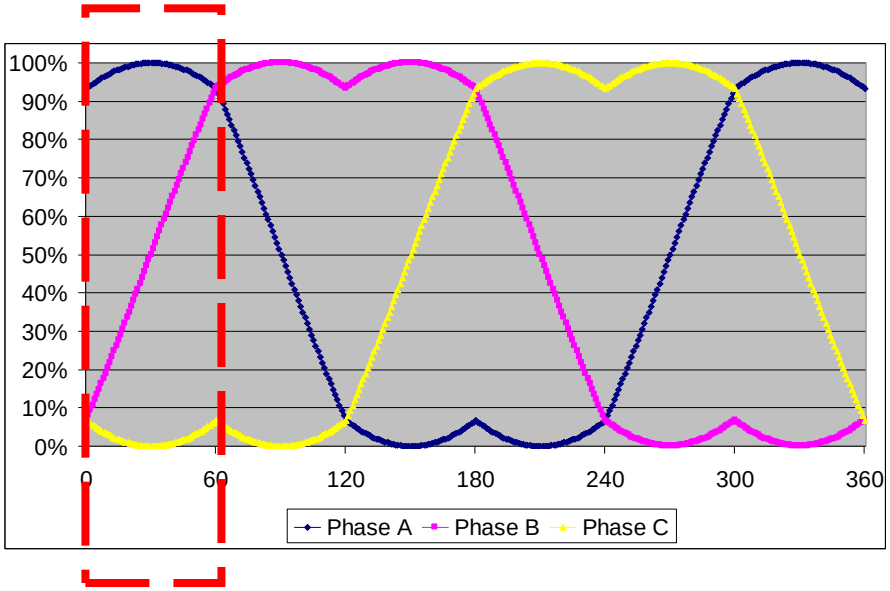
- Three shunts current reading methodology
- Three shunts current reading implementation
- Three shunts current reading used resources
- Three shunts current reading figures

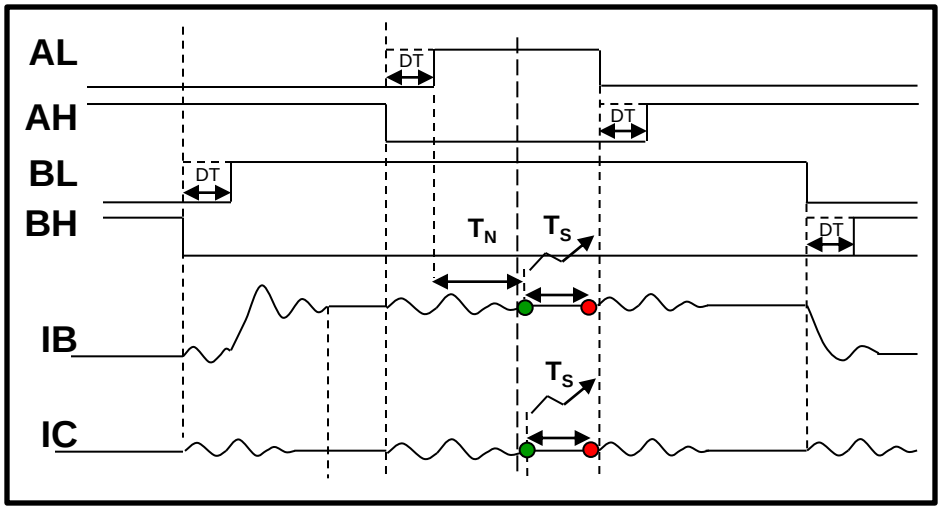
Three shunts current reading *methodology*

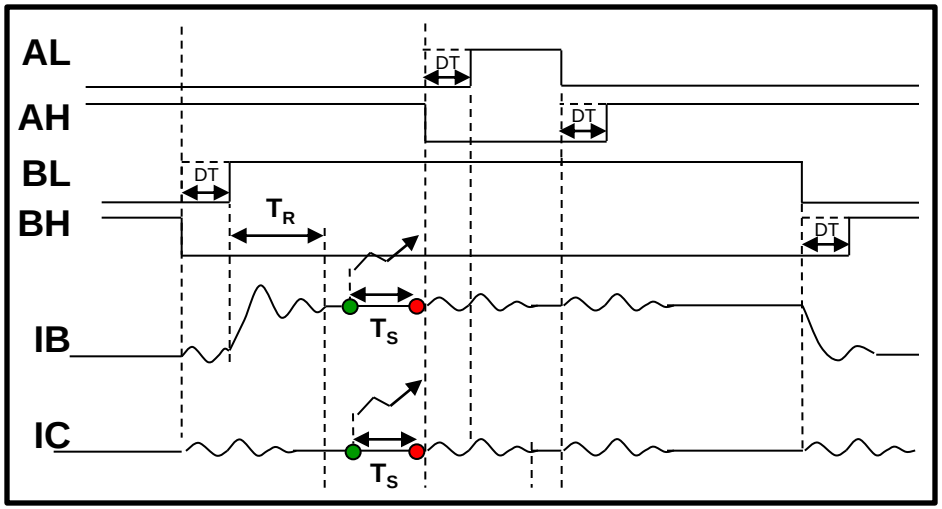


- The sampling of the currents must be performed when the corresponding low side switch is turned on.

Three shunts current reading *implementation*







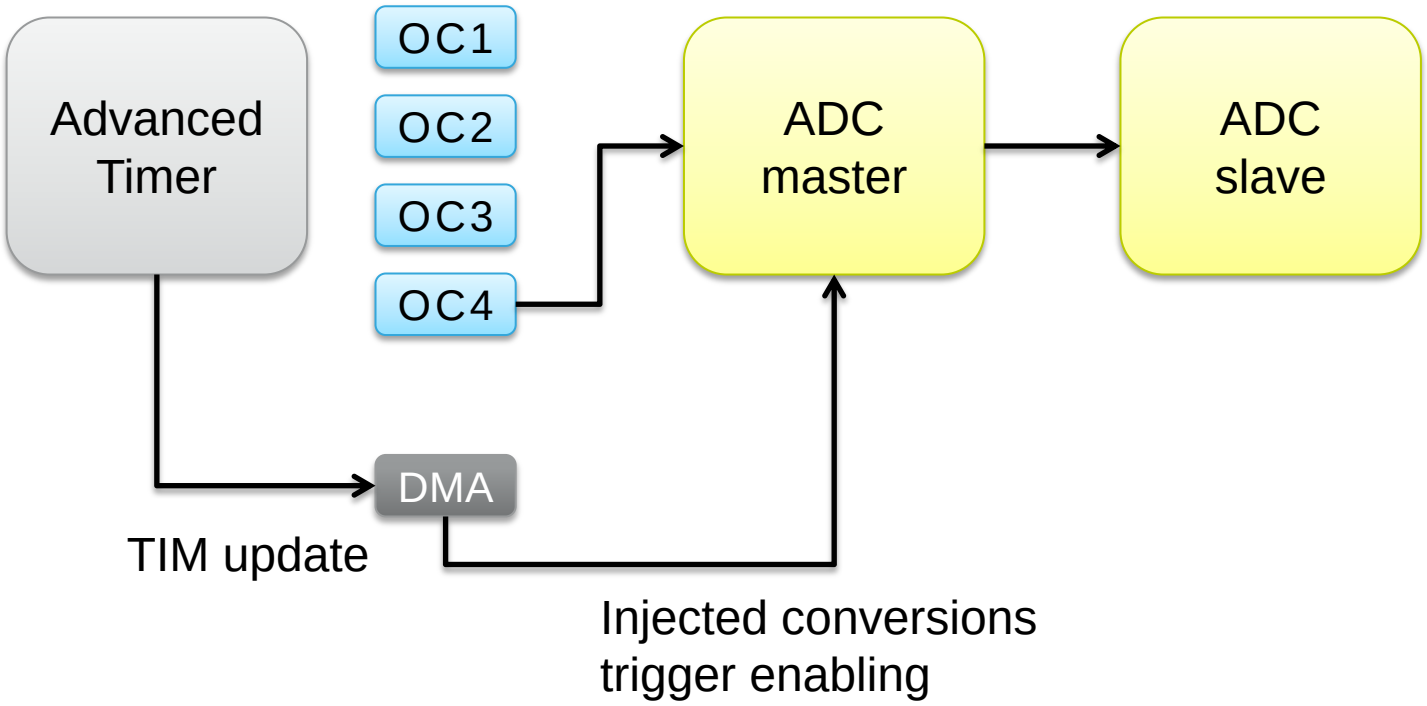
- For each sector of SVM two appropriate phases must be sampled.
- Proper sampling point definition inside the PWM period is required to avoid noise sampling.

Three shunt current reading improvement

- Enabling of injected external trigger performed using a DMA event on TIM update.
  - Advantage
    - Timer update interrupt service routine no more necessary.
  - Cost
    - Use of one DMA channel.

Three shunts current reading used resources

Adv. Timer	DMA	ISR	ADC master	ADC slave	Note
TIM1	DMA1_CH5	None	ADC1	ADC2	DMA is used to enable ADC injected conversion external trigger. Disabling is performed by software.



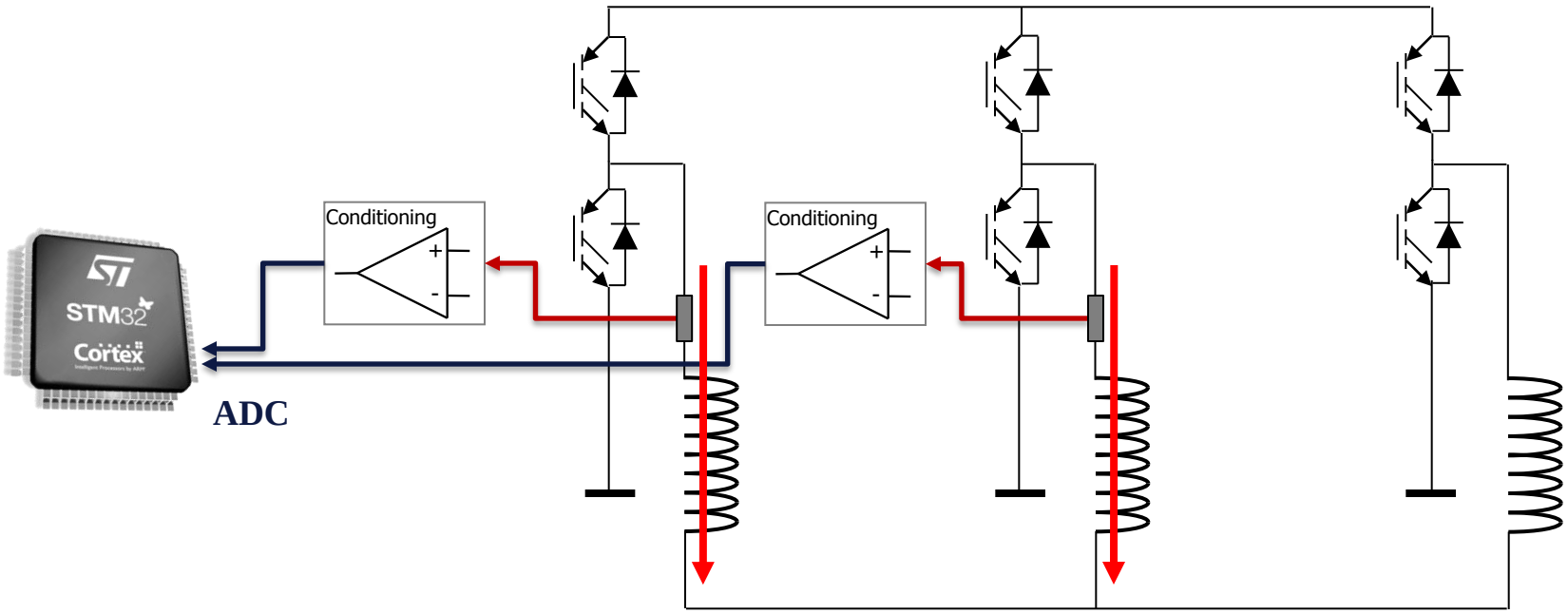
Three shunts current reading Figures

FOC Lib. 2.0			FOC Lib. 3.0		
Execution time	Flash memory	RAM	Execution time	Flash memory	RAM
4.6µs	2280b	10b	4.3s	3104b	112b

ICS current reading

- ICS current reading methodology
- ICS current reading implementation
- ICS current reading used resources
- ICS current reading figures

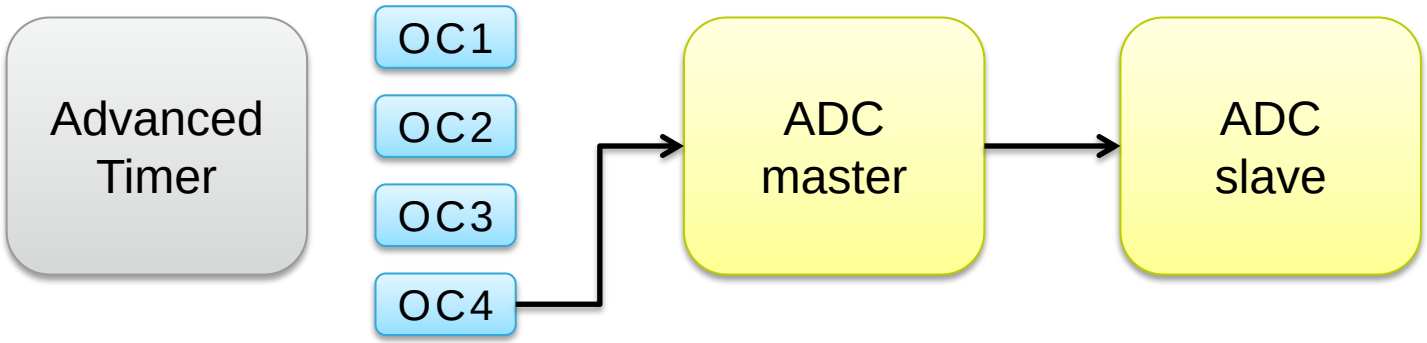
ICS current reading *methodology*



- The sampling of the currents can be performed every where in the PWM period.
- Has been chosen to sample simultaneously both current in the first crest of timer counter after the update event.

ICS current reading used resources

Adv. Timer	DMA	ISR	ADC master	ADC slave	Note
TIM1	None	None	ADC1	ADC2	OC4 value is constant.



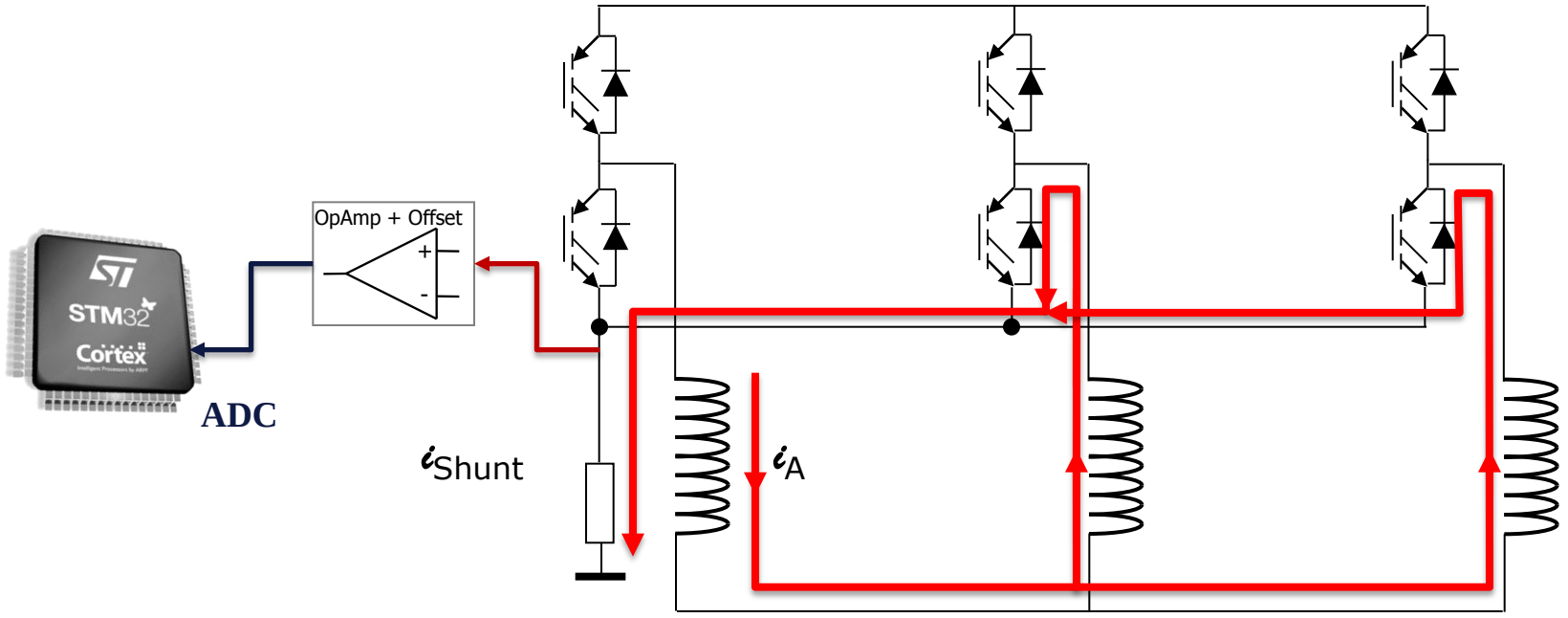
ICS current reading Figures

FOC Lib. 2.0			FOC Lib. 3.0		
Execution time	Flash memory	RAM	Execution time	Flash memory	RAM
2.1µs	1284b	6b	2.9s	2000b	104b

Single shunt current reading

- Single shunt current reading methodology
- Single shunt current reading implementation
- Single shunt current reading used resources
- Single shunt current reading figures

Single shunt current reading *methodology*

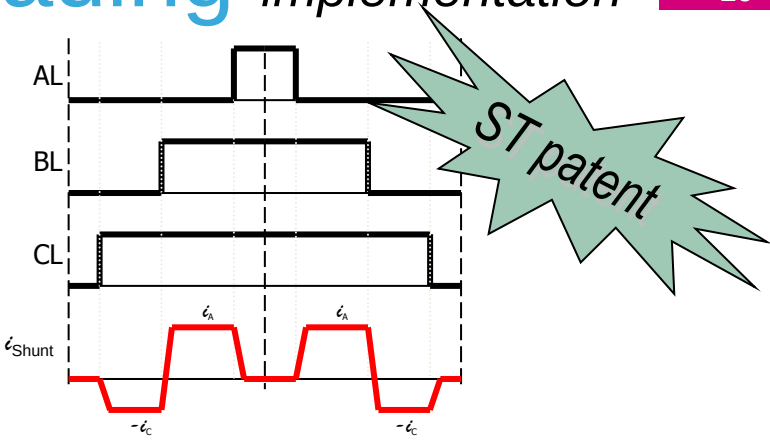


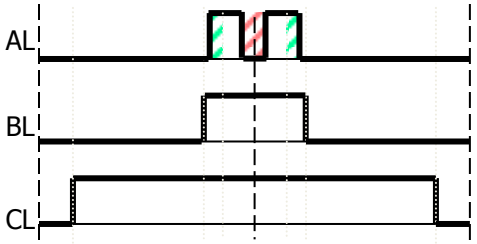
- For each configuration of the low side switches, the current that is flowing in the shunt resistor can be one of the motor phase current.

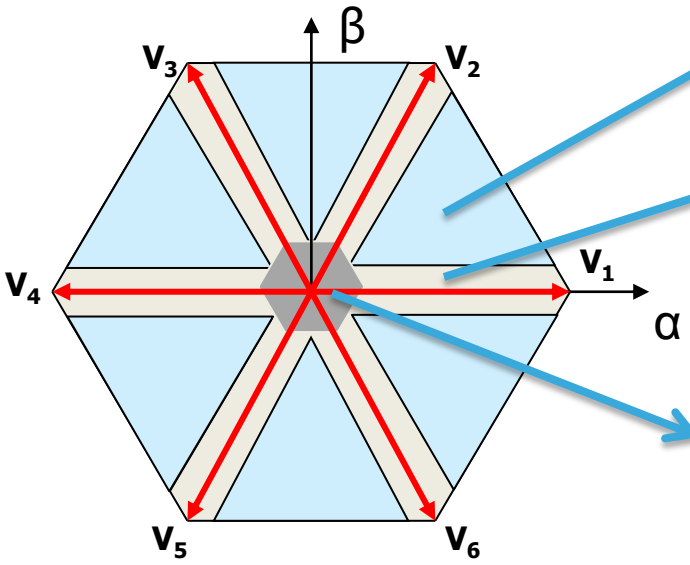
AL	BL	CL	i_{Shunt}
Open	Open	Open	0
Open	Close	Close	i_A
Open	Open	Close	$-i_C$
Close	Open	Close	i_B
Close	Open	Open	$-i_A$
Close	Close	Open	i_C
Open	Close	Open	$-i_B$
Close	Close	Close	0

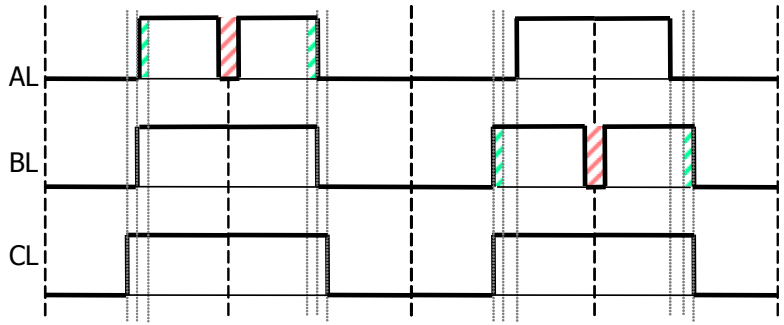
Single shunt current reading *implementation*

- The space vector plane is divided in four regions
- For each region the current sampling method is different.







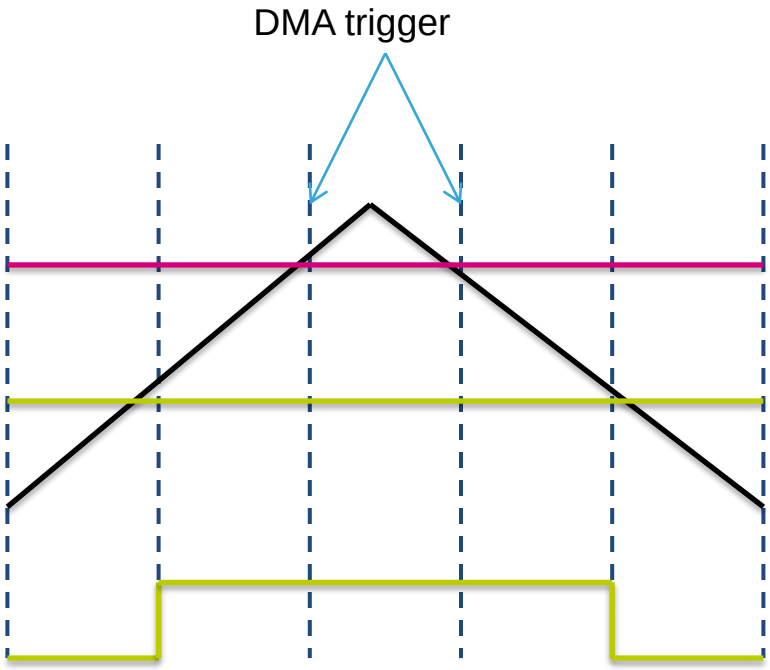


life.augmented

Single shunt current reading new implementation

Active vector insertion implementation

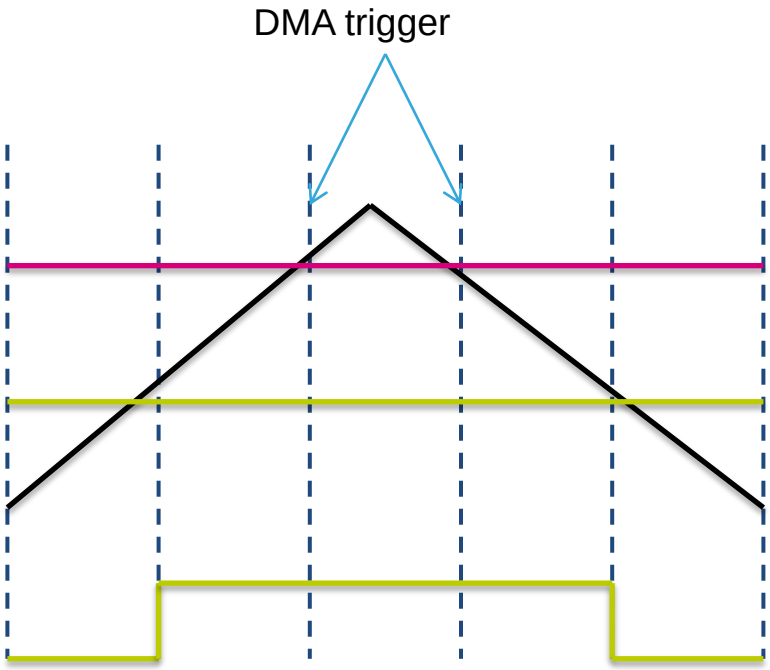
- Principle used to perform the active vector insertion is to have a DMA triggered by a timer compare event…



Single shunt current reading new implementation

Active vector insertion implementation

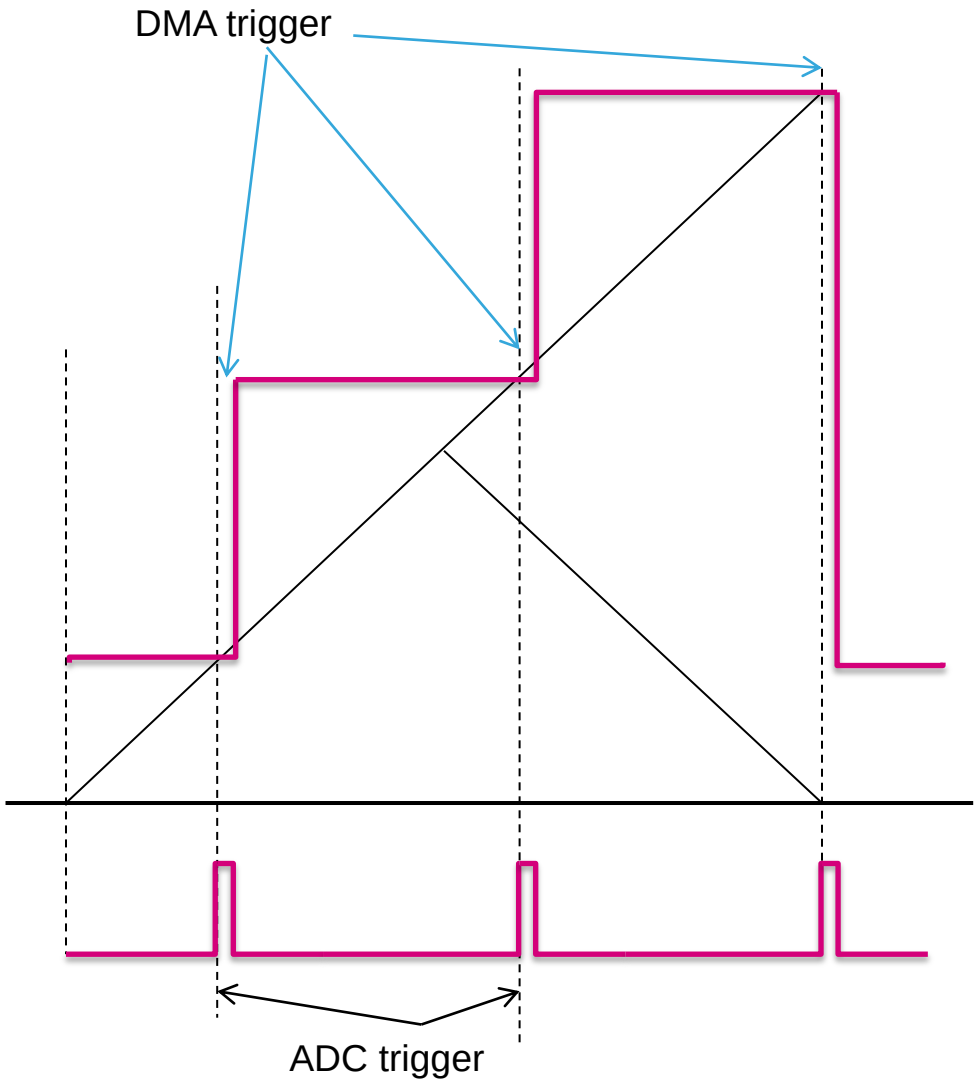
- Principle used to perform the active vector insertion is to have a DMA triggered by a timer compare event…
- … that acts on compare register of another channel able to generate the required modification in the PWM output signal.



Single shunt current reading new implementation

ADC triggering

- Current sampling is implemented using a timer output compare as ADC trigger signal.
- Dual sampling is allowed by means of DMA acting on its compare register triggered by itself match.
- Timer used for triggering is the auxiliary timer set in up-counting mode, synchronized with and having the same frequency of the advanced timer.

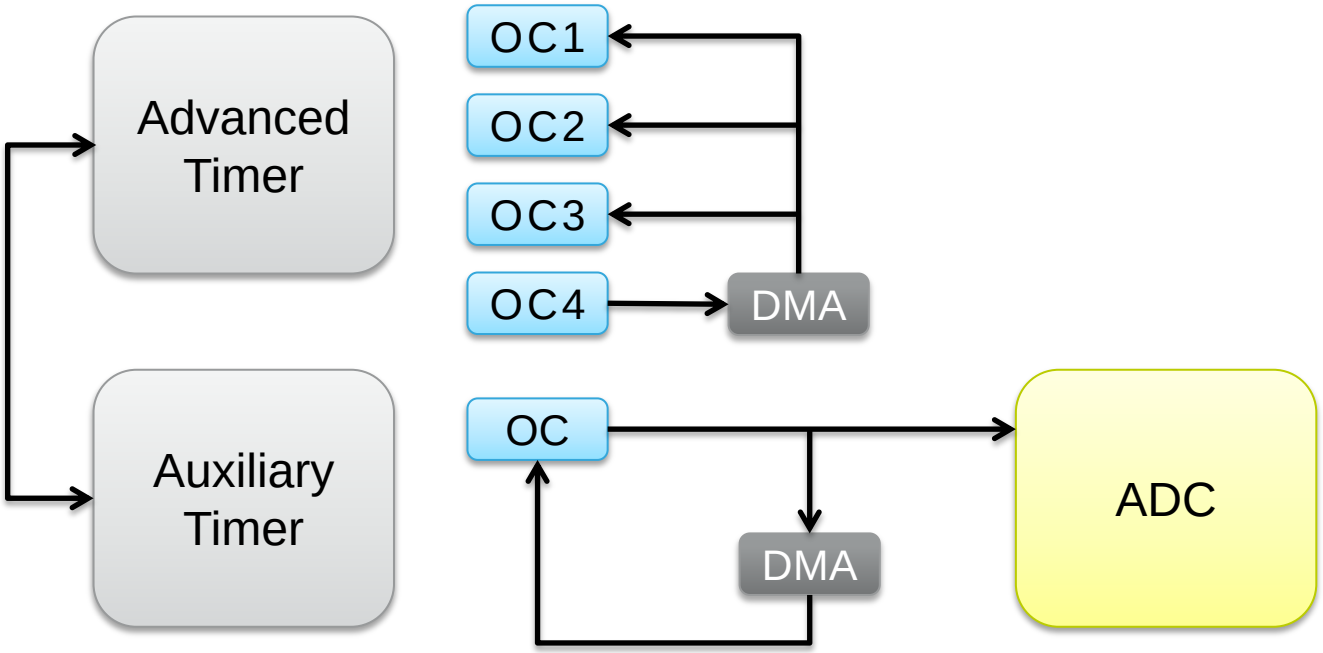


Single shunt current reading new implementation

- Advantage
  - Execution time and flash usage reduced.
  - Save 3 DMA channels.
  - Simultaneous update of the three output compare registers.
  - Critical section in timer update ISR is lighter.
- Cost
  - Use of an extra timer.

Single shunts current reading used resources

Adv. Timer	Aux. Timer	DMA	ISR	ADC	Note
TIM1	TIM3 (CH4)	DMA1_CH3 DMA1_CH4	TIM1_UP DMA1_CH4_TC(Rep>1)	ADC1	RC DAC can't be used
TIM1	TIM4(CH3)	DMA1_CH5 DMA1_CH4	TIM1_UP DMA1_CH4_TC(Rep>1)	ADC1	Not present in low density Products



Single shunts current reading Figures

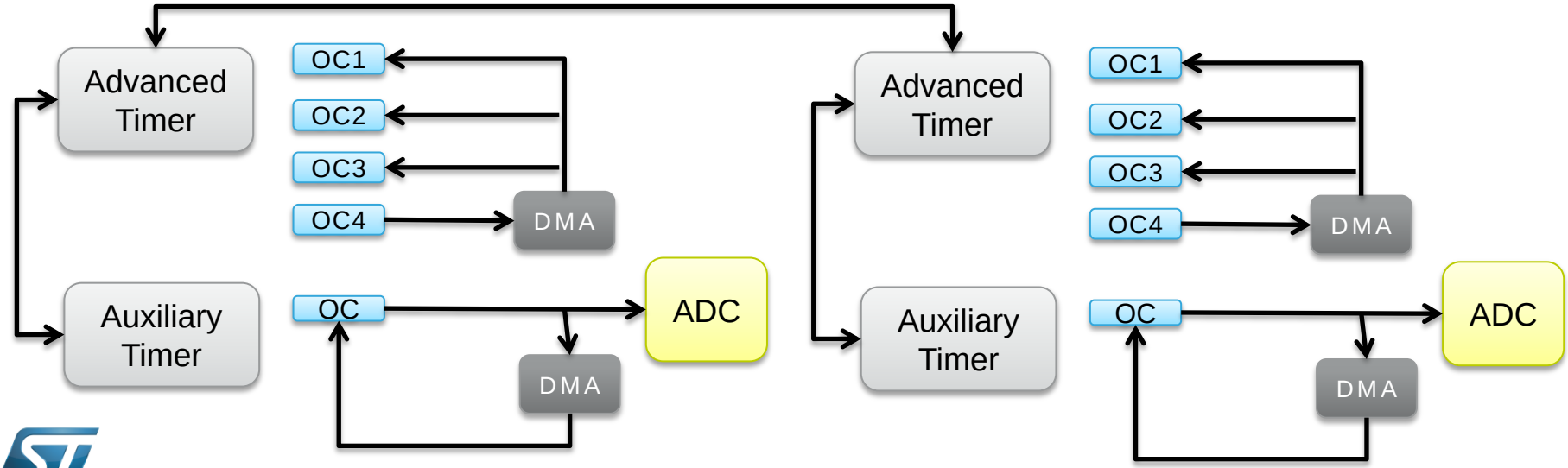
FOC Lib. 2.0			FOC Lib. 3.0		
Execution time	Flash memory	RAM	Execution time	Flash memory	RAM
9.7µs	4420b	90b	9.1us	4368b	132b
		Value line	19.7us	4368b	132b

Current reading in dual motor control

- R1_HD2 used resources
- ICS/R3_HD2 used resources

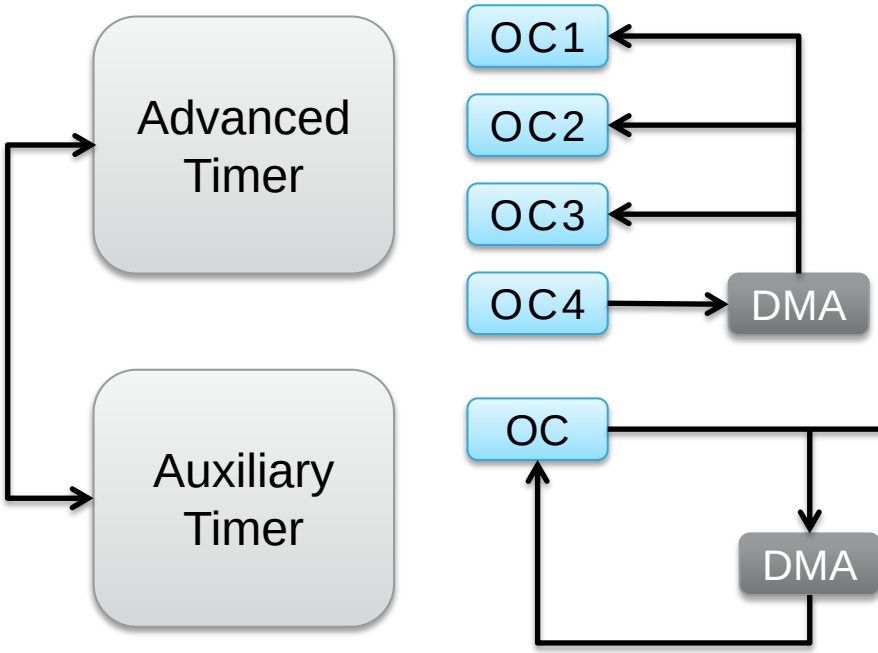
R1_HD2 used resources dual drive

Adv. Timer	Aux. Timer	DMA	ISR	ADC	Note
TIM1	TIM5 (CH4)	DMA2_CH1 DMA1_CH4	TIM1_UP DMA1_CH4_TC(Rep>1)	ADC3	First R1 instance
TIM8	TIM4(CH3)	DMA1_CH5 DMA2_CH2	TIM8_UP DMA2_CH2_TC(Rep>1)	ADC1	Second R1 instance
TIM8	TIM5 (CH4)	DMA2_CH1 DMA2_CH2	TIM8_UP DMA2_CH2_TC(Rep>1)	ADC3	First R1 instance
TIM1	TIM4(CH3)	DMA1_CH5 DMA1_CH4	TIM1_UP DMA1_CH4_TC(Rep>1)	ADC1	Second R1 instance



R1_HD2 used resources sigle drive

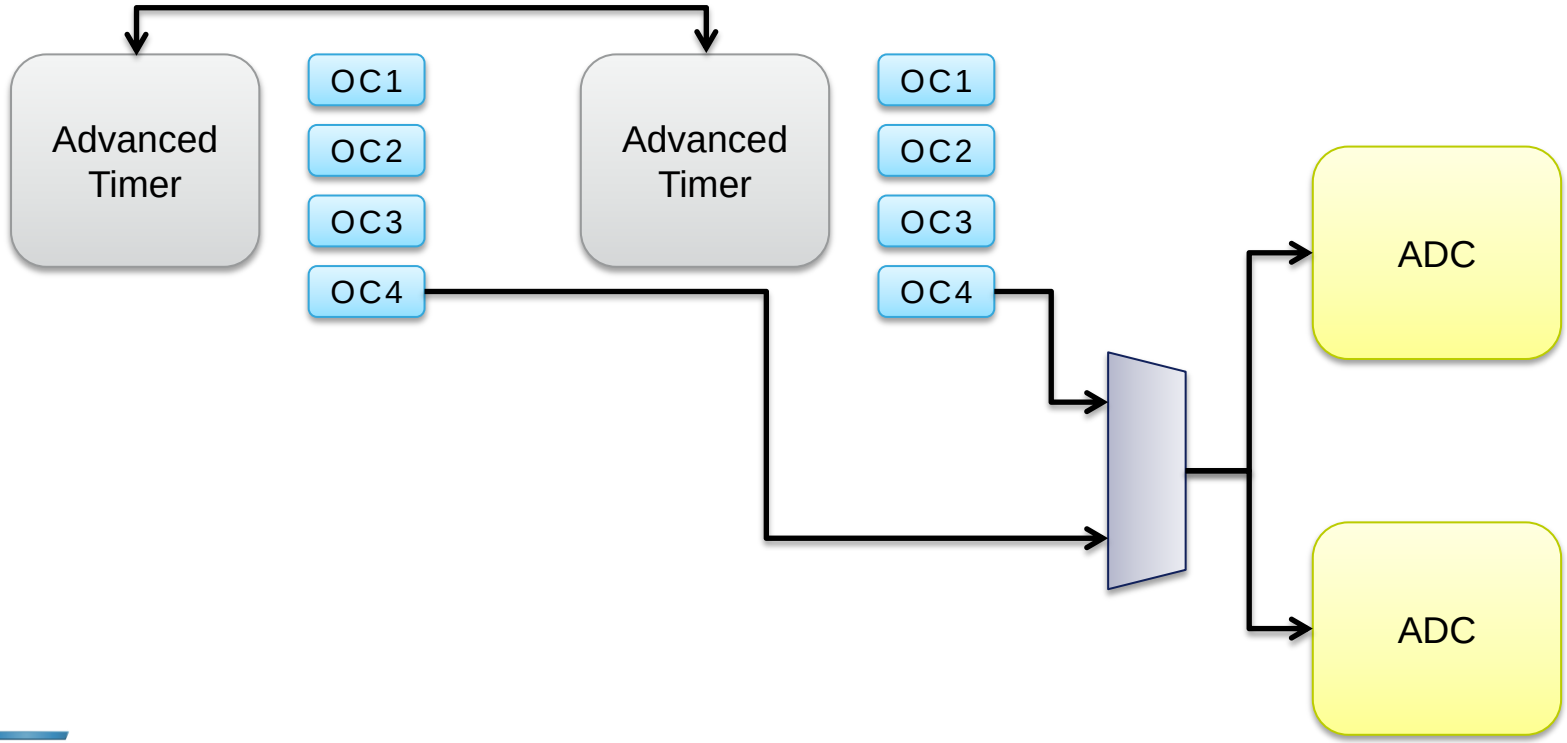
Adv. Timer	Aux. Timer	DMA	ISR	ADC	Note
TIM1	TIM5 (CH4)	DMA2_CH1 DMA1_CH4	TIM1_UP DMA1_CH4_TC(Rep>1)	ADC3	First R1 instance
TIM8	TIM5(CH4)	DMA2_CH1 DMA2_CH2	TIM8_UP DMA2_CH2_TC(Rep>1)	ADC3	First R1 instance



Same resources are required by R1_HD2 in dual motor driver when the other drive is R3_HD2 or CS_HD2.

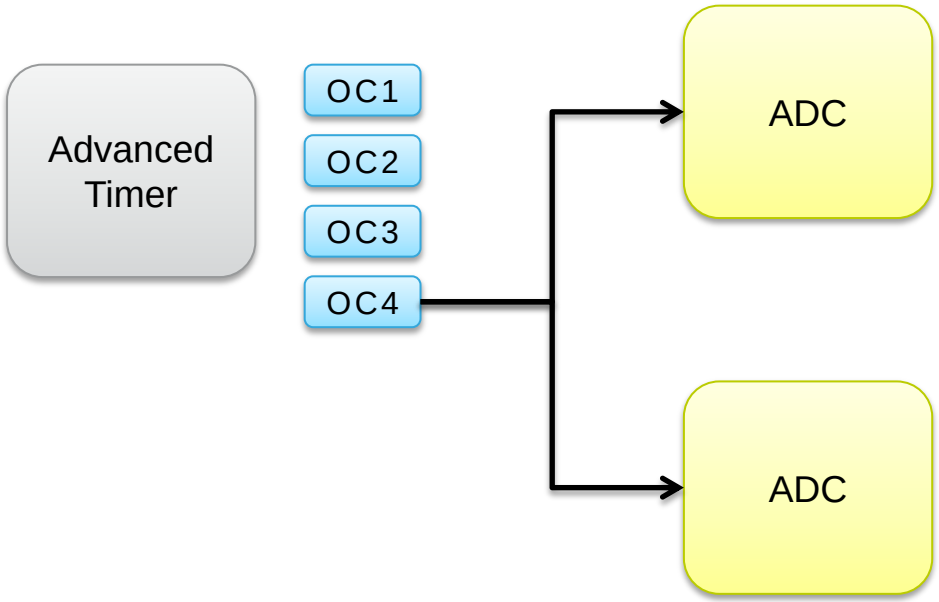
ICS/R3_HD2 used resources dual drive

Adv. Timer	DMA	ISR	ADC	Note
TIM1	None	TIM1_UP	ADC1 ADC2	ADC is used in time sharing. Trigger selection is performed in the TIM_UP ISR.
TIM8	None	TIM8_UP	ADC1 ADC2	ADC is used in time sharing. Trigger selection is performed in the TIM_UP ISR.



ICS/R3_HD2 used resources single drive

Adv. Timer	DMA	ISR	ADC	Note
TIM1	None	TIM1_UP	ADC1 ADC2	ADC is used in time sharing. Trigger selection is performed in the TIM_UP ISR.
TIM8	None	TIM8_UP	ADC1 ADC2	ADC is used in time sharing. Trigger selection is performed in the TIM_UP ISR.



Same resources are equired by R3_HD2 or ICS_HD2 in dual motor drive when the other drive is R1_HD2.

Dual motor current reading Figures

	FOC Lib. 3.0		
	Execution time	Flash memory	RAM
ICS	3.3us	2464b	138b
Single shunt	9.2us	4760b	218b
Three shunt	7us	3404b	186b

	FOC Lib. 3.0 single motor LM		
	Execution Time	Flash memory	RAM
ICS	2.9us	2000b	104b
Single shunt	9.1us	4368b	132b
Three shunt	4.3us	3104b	112b

Regular conversions

- Injected conversion are dedicated for motor phase's currents measurement.
- Regular conversion are dedicated for:
  - DC bus voltage measurement
  - Heat sink temperature measurement
  - User defined conversions
- Single regular conversions is started on-demand by the software.
- The priority of the conversions is managed in hardware by the peripheral. This means that an injected conversion stops the execution of a regular conversion. The regular conversion is performed at the end of the injected one.
- DMA is used to store the result of the regular conversion.
- It is always used the ADC1 peripheral for all PWMnCurrentFdbk derivates.

Regular conversions

- To request a regular conversion call

PWMC_ExecRegularConv (oPWMC, Channel)

- Until the end of regular conversion the execution flow is stopped unless it is interrupted by an higher level ISR. To avoid conflict the PWMC_ExecRegularConv should be called from the main or ISR with priorities lower than MC related ISR.