

Registration No.:

--	--	--	--	--	--	--	--	--

Total Number of Pages: 02

Course: B.Tech/IDD
Sub_Code: EOPC2004

3rd Semester Regular Examination: 2024-25

SUBJECT: Digital Electronics

BRANCH(S): CST, CSEAIML, CSEDS, CSEAI, CSE, CSE, CSIT, CE, IT

Time: 3 Hours

Max Marks: 100

Q.Code: R500

Answer Question No.1 (Part-I) which is compulsory, any eight from Part-II and any two from Part-III.

The figures in the right hand margin indicate marks.

Part-I

Q1 Answer the following questions: (2 x 10)

- a) Find the hexadecimal number of $(243)_8$.
- b) Explain the role of transistors as switches in digital circuits.
- c) How many OR gate and half adder are required to implement a full adder Circuit?
- d) What is race around condition?
- e) What is essential prime implicant?
- f) What is the difference between combinational circuit and Sequential circuit?
- g) Design NAND gate and XOR gate using 2 - input NOR gate.
- h) What is a hazard in a combinational circuit?
- i) Convert the 100110 binary code into gray code.
- j) A 4 bit modulo-16 ripple counter uses JK flipflops. If the propagation delay of each Flip flop is 50 ns. Then find the maximum clock frequency.

Part-II

Q2 Only Focused-Short Answer Type Questions- (Answer Any Eight out of Twelve) (6 x 8)

- a) If $X = 111.101$ and $Y = 101.110$, Calculate $X + Y$, $X - Y$, and $Y - X$ by using 2's Complement method.
- b) Use the K-Map to simplify the expression $X = \bar{A} \cdot \bar{B} \bar{C} + \bar{B} C + \bar{A} B$.
- c) Implement the function $F = A(CD + B) + B\bar{C}$ using NAND gate only.
- d) Use the Quine-McCluskey technique to minimize the following Boolean function:
$$F(A, B, C) = \sum(1, 3, 5, 7)$$
- e) Write short note on Mealey Morre Model of Finite State Machine.
- f) Design of NAND gate using CMOS.
- g) Explain the different types of Laws in Boolean function.
- h) Define and explain the operation of 4 bit shift register?
- i) Design a 3-bit binary counter using T flip flop.
- j) Design a Full adder circuit.

- k) Differentiate between decoder and demultiplexer. Under what circumstance a decoder can be converted into demultiplexer?
- l) Design and explain the Johnson Counter.

Part-III

Only Long Answer Type Questions (Answer Any Two out of Four)

- Q3** a) Design of 8×1 MUX using 2×1 MUX. (6+10)
b) Given that $f(A, B, C, D) = \sum(0, 1, 5, 7, 10, 14, 15)$. Implement this function using an appropriate Multiplexer.
- Q4** a) Derive the Characteristic Equation of D Flipflop. (6+10)
b) Convert the SR Flipflop to JK Flipflop.
- Q5** a) Minimize the Four variable logic function using K-Map. $f(A, B, C, D) = \sum m(0, 1, 2, 3, 5, 7, 8, 9, 11, 14)$ (8+8)
b) Design a simple logic circuit such that the outputs is 1 when the binary number A, B, C, D is greater than 0110.
- Q6** a) What are the salient features of an Algorithmic State Machine (ASM) chart? (6+10)
b) Design an ASM chart for a simple weighing machine.

Registration No :

--	--	--	--	--	--	--	--	--	--

Total Number of Pages : 02

B. Tech, IDD (B. Tech and M. Tech)
RCS3C001

3rd Semester Reg/Back Examination: 2023-24

Digital Logic Design

CST,CSEAI,CSEDS,CSE,CSIT,CSEAME,IT

Time : 3 Hour

Max Marks : 100

Q. Code : N456

Answer Question No.1 (Part-1) which is compulsory, any eight from Part-II and any two from Part-III.

The figures in the right hand margin indicate marks.

Part-I

- Q1** Answer the following questions: (2 x 10)
- a) Explain how a transistor can act as a switch?
 - b) Find the 16's complement of BBD5_H.
 - c) Implement a 2-input XOR gate using minimum no. of 2-input NAND gate.
 - d) State and prove DeMorgan's theorem.
 - e) Represent the Boolean expression $F = A'B + AC + BC'$ in the form of maxterms.
 - f) Derive the characteristic equations for the JK Flip-flop.
 - g) Determine the Gray code equivalent of (11100101)₂.
 - h) Convert the following number with the indicated bases to decimal: (43150)₆.
 - i) The contents of a four-bit register are initially 1011. The register is shifted six times to the right, with the serial input being 101101. What is the content of the register after sixth shift?
 - j) Implement the carry of a full adder using 2-input NOR gates only.

Part-II

- Q2** Only Focused-Short Answer Type Questions- (Answer Any Eight out of Twelve) (6 x 8)
- a) Explain error detecting and error correcting codes with an example in both cases. Also specify the application of these codes.
 - b) Given, Boolean expression $F = AB + BC + AB'C$. Express F as
 - (i) In product of sum terms only
 - (ii) In product of maxterms only
 - (iii) Implement F using NOR gates only.
 - c) Minimize and implement the following Boolean function F, together with the don't-care conditions d, using NAND gates: $F(A, B, C, D) = \sum(1, 2, 4, 6, 8, 9, 10)$ and $d(A, B, C, D) = \sum(0, 5, 9, 13, 14)$.
 - d) Implement a full subtractor circuit using a 4:1 MUX and additional logic gates.
 - e) Convert by adding external gates: (a) a D flip-flop to a J-K flip-flop. (b) a T flip-flop to a D flip-flop.
 - f) Simplify the following Boolean function, $f(W, X, Y, Z) = \sum m(2, 6, 8, 9, 10, 11, 14, 15)$ using Quine-McCluskey tabular method.
 - g) Implement a 4 to 16 decoder using 1 to 2 decoder only and explain its operation.

- h) What is a priority encoder? Show the gate level circuit diagram of a 8-to-3 priority encoder.
- i) Show that the characteristic equation for the complement output of a JK flip-flop is $Q' (t + 1) = J'Q' + KQ$
- j) Explain how to convert serial data to parallel and parallel data to serial. What type of register is needed?
- k) Draw the CMOS schematic diagram of the Boolean expression $Y = [A + BCD]'$.
- l) Show that a ring counter with 'N' flip-flops produces a sequence of 'N' states. List the 5 states produced with five flip-flops. State the application of such counter.

Part-III

Only Long Answer Type Questions (Answer Any Two out of Four)

- Q3** Design a BCD to seven segment decoder which has four input lines (A, B, C and D) and 7 output lines (a, b, c, d, e, f and g), this output is given to seven segment LED display which displays the decimal number depending upon inputs. Implement the decoder using basic logic gates. (16)
- Q4** a) Design a combinational circuit with three inputs x, y, and z, and three outputs A, B, and C. When the binary input is 0, 1, 2, or 3, the binary output is three greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is two less than the input. (8+8)
 b) What is the application of a parity bit generator? Design a 3-bit odd parity generator circuit.
- Q5** a) Design a four-bit shift register with a parallel load using D flip-flops. There are two control inputs: shift and load. When shift = 1, the contents of the register are shifted by one position to right. New data are transferred into the register when load = 1 and shift = 0. If both control inputs are equal to 0, the contents of the register do not change. (8+8)
 b) Implement a 2-bit multiplier circuit using AND gates and parallel adder with explanation
- Q6** a) A sequential circuit with two D flip-flops A and B, two inputs x and y, and one output z is specified by the following next-state and output equations:
 $A(t + 1) = x'y + x + B, \quad B(t + 1) = x'A + xB, \quad z = A + B$
 (a) Draw the logic diagram of the circuit.
 (b) List the state table for the sequential circuit.
 (c) Draw the corresponding state diagram.
 b) Design a decade counter using JK flip-flop. (8+8)

Registration No.:

--	--	--	--	--	--	--	--	--	--

Total Number of Pages: 02

Integrated Dual Degree (B.Tech and M.Tech)
REC4C002/RME4G001/REI4C002

4th Semester Regular/Back Examination: 2023-24

SUBJECT: Digital Systems Design

BRANCH(S): ECE,ELECTRONICS & CE,ETC,MECH,MMEAM,AEIE,EIE

Time: 3 Hour

Max Marks: 100

Q.Code: P313

Answer Question No.1 (Part-I) which is compulsory, any eight from Part-II and any two from Part-III.

The figures in the right hand margin indicate marks.

Part-I

- Q1** Answer the following questions: (2 x 10)
- a) Convert $(5064)_9$ into base 5.
 - b) Show that $A+B \cdot C = (A+B) \cdot (A+C)$
 - c) What is the importance of parity bit?
 - d) State the need for a tristate buffer.
 - e) How race condition in JK flipflop can be resolved?
 - f) Differentiate between level clocking and edge triggering.
 - g) List the advantages of CMOS.
 - h) What problem could occur when the counter circuit is powered-up?
 - i) Write any three differences between EEPROM and UVEPROM.
 - j) Define access time and word length of a memory chip.

Part-II

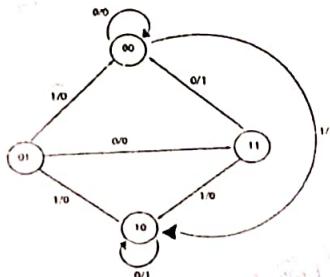
- Q2** Only Focused-Short Answer Type Questions- (Answer Any Eight out of Twelve) (6 x 8)
- a) Perform the arithmetic operation $(+42) + (-13)$ and $(-42) - (-13)$ in binary using the signed 2's-complement representation for negative numbers.
 - b) Consider a 4-input Boolean function that outputs a binary 1 whenever an odd number of its inputs are binary 1. Using Boolean logic or otherwise, show how the above function can be implemented using only 2-input XOR gates.
 - c) How parity checkers help in finding errors in digital data transmission?
 - d) What is associative memory? Draw and explain its block diagram.
 - e) Find the POS for the function $F(x, y, z) = \pi(0, 1, 4, 5)$.
 - f) Design a BCD to decimal decoder.
 - g) Design a 5×32 decoder with four 3×8 decoder with enable and one 2×4 decoder. Use block diagrams only.

- h) A sequential circuit with 2 JK Flip Flops A and B, two inputs X and Y, and one output Z. The Flip Flop input equations and circuit output equations are
 $J_A = B'Y' + BX$, $K_A = B'XY'$, $J_B = A'X$, $K_B = A + XY'$ and $Z = AX'Y' + BX'Y$
 Draw the logic diagram of the circuit with the state table.
- i) With the aid of block and example state diagrams, describe the main features of Moore and Mealy implementations of finite state machines.
- j) What is asynchronous counter? Design asynchronous counter that counts the sequence of 0-1-4-6-7 using T flip-flop.
- k) Explain the working of R-2R ladder type DAC.
- l) Implement a 4:1 MUX circuit using VHDL.

Part-III

Only Long Answer Type Questions (Answer Any Two out of Four)

- Q3 a) Prove that a positive-logic AND gate is a negative-logic OR gate and vice-versa. (4)
 b) A priority encoder has $2N$ inputs. It produces an N-bit binary output indicating the most significant bit of the input that is TRUE, or 0 if none of the inputs is TRUE. It also produces an output NONE that is TRUE if none of the inputs is TRUE.
 (i) Write down the Truth table showing all inputs and all outputs for an eight-input priority encoder.
 (ii) Give simplified Boolean expressions for all outputs of the eight-input priority encoder. (12)
- Q4 a) Design a combinational circuit with three inputs and six outputs. The output binary number should be the square of the input binary number. (8)
 b) Draw a neat diagram of TTL NAND gate and explain its operation. What is meant by sourcing and sinking? (8)
- Q5 a) Draw the block diagram of a 4 bit ALU, and explain it, showing its inputs and outputs. (6)
 b) (10)



Design the sequential circuit with respect to the above state diagram using J-K flip flops.

- Q6 a) Implement the circuit of a PLA with 3 input, 2 output, and 4 product terms
 $F_1(A, B, C) = \sum(3, 5, 6, 7)$, $F_2(A, B, C) = \sum(0, 2, 4)$ (8)
 b) What is the difference between a serial and a parallel transfer? Explain how to convert serial data to parallel and parallel data to serial. What type of register is needed? (8)

Registration No.:

--	--	--	--	--	--	--	--	--	--

Total Number of Pages : 02

Course: Integrated Dual Degree (B.Tech and M.Tech)
Sub_Code: REL4C001/REE4C001/RBM4C001

4th Semester Regular/Back Examination: 2023-24

SUBJECT: DIGITAL ELECTRONICS

BRANCH(S): ELECTRICAL, EE, EEE, BIOMED

Time : 3 Hour

Max Marks : 100

Q.Code: P056

Answer Question No.1 (Part-1) which is compulsory, any eight from Part-II and any two from Part-III.

The figures in the right hand margin indicate marks.

Part-I

Q1 Answer the following questions : (2 x 10)

- a) Find out the hexadecimal equivalent of $(707.77)_8$.
- b) Write down any two applications of EX-OR gate.
- c) What will be $a \oplus b$, If $ab = 0$?
- d) How many 3 to 8 line decoders with an enable input are needed to construct a 6 to 64 line decoder without using any other logic gates?
- e) Write the difference between synchronous inputs and asynchronous inputs.
- f) The output of a J-K flip-flop is 0. Its output does not change when a clock pulse is applied. What can be the inputs J and K respectively?
- g) What is ALU?
- h) Differentiate between PLA & PAL.
- i) What is sequential circuit? Also draw a 1-bit memory circuit.
- j) What is FPGA?

Part-II

Q2 Only Focused-Short Answer Type Questions- (Answer Any Eight out of Twelve) (6 x 8)

- a) Implement EX-OR gate using minimum number of NAND gates.
- b) Obtain the simplified form for the given maxterm expression using K-map.
$$f(A, B, C, D) = \prod(0, 1, 4, 5, 6, 7, 9, 14) \cdot d(13, 15)$$
- c) Implement the given functions using single 3:8 decoder.
$$f_1(A, B, C) = \prod(2, 3, 4, 5, 7)$$

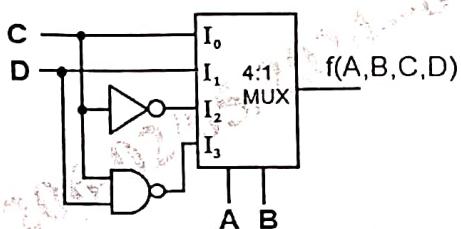
$$f_2(A, B, C) = \sum(1, 3, 5)$$
- d) Illustrate CCD memory and write its few applications.
- e) Explain any one of the error detecting & error correcting coding scheme.
- f) Explain Mod-5 ripple counter using JK-FF with its output wave forms.
- g) Explain operation of 4-bit SIPO with necessary diagram.
- h) Write down the specifications for D/A converter and also explain it.

- i) Design a magnitude comparator to compare two 3-bit binary numbers.
- j) Give an example of A/D converter and mention its few important characteristics.
- k) Design S-R flip-flop to D flip-flop conversion. Find the conversion table.
- l) Explain the operation of TTL with required diagram.

Part-III

Only Long Answer Type Questions (Answer Any Two out of Four)

- Q3** a) Simplify the given function using K-map. Also find its POS result. (8+8)
 $f(A, B, C) = \sum m(0, 2, 4, 6, 7, 8, 10, 12, 13, 15)$
- b) Find the Boolean function implemented in the figure using 4:1 MUX.



- Q4** a) Design a BCD adder with proper explanation. (8+8)
 b) Discuss the working of CMOS circuit as a digital logic operation.
- Q5** Design a decade counter using T-FF. Also draw its waveforms. (16)
- Q6** a) Explain the design principle of ROM. Mention its differences than RAM. (8+8)
 b) Explain A/D converter using voltage-to-frequency conversion with proper circuit and waveforms.

Registration No :

--	--	--	--	--	--	--	--	--

Total Number of Pages : 02

B.Tech

RBM4C001/REE4C001/REL4C001

4th Semester Regular/Back Examination: 2023

SUBJECT: Digital Electronics

BRANCH(S): BIOMED, EEE, ELECTRICAL

Time : 3 Hour

Max Marks : 100

Q.Code : M217

Answer Question No.1 (Part-I) which is compulsory, any eight from Part-II and any two from Part-III.

The figures in the right hand margin indicate marks.

Part-I

Q1 Answer the following questions: (2 x 10)

- a) Write the binary equivalent of $(101.11)_8$
- b) What is the importance of Priority encoder?
- c) Draw CMOS logic circuit & write its one application.
- d) What is the specialty of EX-OR gate?
- e) Compare synchronous counter with asynchronous counter.
- f) What is the minimum number of flip-flops needed to design a mod-16 counter?
- g) Define PLA & PAL.
- h) Write some applications of MUX & DMUX.
- i) How JK Flipflop is converted to T-Flipflop?
- j) What is FPGA?

Part-II

Q2 Only Focused-Short Answer Type Questions- (Answer Any Eight out of Twelve) (6 x 8)

- a) Draw TTL circuit & explain its operation.
- b) Draw the truth table & circuit for full Adder. Also mention its output equations.
- c) Implement the given functions using single 3:8 decoder.

$$f_1(A, B, C) = \prod(2, 3, 4, 5, 7)$$

$$f_2(A, B, C) = \sum(1, 3, 5)$$

- d) Do a conversion of SR-FF to D-FF with detailed truth table & K-Map analysis.
- e) Discuss any two error detecting codes & also any two correcting codes with examples.

- f) Design a 2-bit synchronous up counter.
- g) Write down two applications of each for MUX, Flipflop, Counter, Ex-OR gate, shift register & CMOS.
- h) Simplify the expression using K-maps: $F(x, y, z) = \pi(0, 2, 4, 5, 7)$
- i) Explain operation of ring counter with suitable output wave diagram.
- j) The initial contents of the 4-bit serial in parallel out shift register is 1011. What will be contents of the given shift register after 5 clock pulses applied?
- k) Explain operation of successive approximation A/D converter.
- l) Draw a ROM structure & discuss its function.

Part-III

Only Long Answer Type Questions (Answer Any Two out of Four)

- Q3** a) Discuss operation of the carry look ahead adder with the proper logic flows. (8)
 b) Obtain the simplified form for the given expression using K-map.
 Also, draw the minimization result using NAND gate only.

$$F(A, B, C, D) = \sum m(1, 3, 4, 6, 8, 9, 11, 13, 15) + \sum d(0, 2, 14)$$
- Q4** a) A majority circuit is a combinational circuit whose output is equal to 1 if the input variables have more 1's than 0's. The output is 0 otherwise. Design a 3 input majority circuit. (8)
 b) Find the Boolean function for 8:1 MUX. (8)
- Q5** a) Design a decade counter by using JK-FF or T-FF. (8)
 b) Explain shifting of data in serial left & serial right manner with suitable logic circuits. (8)
- Q6** a) How analog to digital conversion happens, Show it stepwise. (8)
 b) Explain PLD & CPLD. (8)

Registration No :

--	--	--	--	--	--	--	--	--	--

Total Number of Pages : 02

Course: B.Tech
Sub_Code: RCS3C001

3rd Semester Regular/Back Examination: 2022-23

SUBJECT: DIGITAL LOGIC DESIGN

BRANCH(S): CSE,CSEAI,CSEAIIME,CSIT,CST,IT

Time : 3 Hour

Max Marks : 100

Q.Code : L421

Answer Question No.1 (Part-1) which is compulsory, any eight from Part-II and any two from Part-III.

The figures in the right hand margin indicate marks.

Part-I

Q1

Answer the following questions :

(2 x 10)

- a) Determine the hexadecimal equivalent number of $(256.5)_8$.
- b) What is the equivalent simplified result of the Boolean function $z=x'y' + xy + x'y$?
- c) What are major differences between MUX with DMUX.
- d) How many 3 to 8 line decoders with an enable input are needed to construct a 6 to 64 line decoder without using any other logic gates?
- e) Compare synchronous counter with asynchronous counter.
- f) Find the Gray code of 1101 & find its 2's compliment.
- g) What is the minimum number of flip-flops needed to design a mod-21 counter ?
- h) Define Prime implicant & mention its importance.
- i) What is specialty of EX-OR gate ?
- j) Draw the circuit diagram of clocked T-flip flop.

Part-II

Q2

Only Focused-Short Answer Type Questions- (Answer Any Eight out of Twelve) (6 x 8)

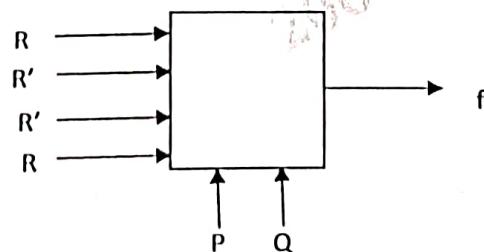
- a) Simplify $f(A, B, C) = \sum m(0, 2, 4, 6, 7, 8, 10, 12, 13, 15)$ using K-map.
- b) Show a two bit multiplier circuit design with an example.
- c) Implement the given functions using single 3:8 decoder.

$$f_1(A, B, C) = \prod(2, 3, 4, 5, 7)$$

$$f_2(A, B, C) = \sum(1, 3, 5)$$

- d) Find out the POS result of $x=a'b'+ab$.

e) What is the Boolean expression for the output of the 4:1 MUX shown below.



- f) Using T-Flip Flops, design a 2 bit synchronous up/down counter.

- g) Explain operation of 4-bit SISO shift register with necessary diagram.
 h) Simplify $X(p,q,r)=p'+qr'$ using K-map.
 i) Design a magnitude comparator to compare two 2-bit binary numbers: $A=A_1A_0$ and $B=B_1B_0$. There should be three outputs: $A>B$, $A=B$, $A<B$.
 j) Explain CMOS circuit as an inverter.
 k) Design S-R flip-flop to D-flip flop conversion. Find its conversion table.
 l) Draw full subtractor logic circuit & find its truth table. Also formulate the outputs of it by using K-map.

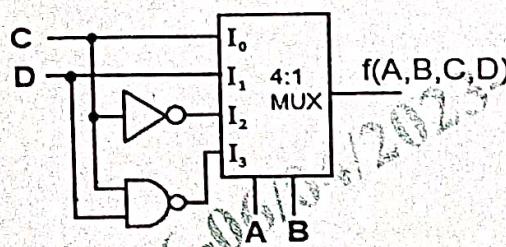
Part-III

Only Long Answer Type Questions (Answer Any Two out of Four)

Q3

- i) Obtain the simplified form for the given expression using K-map. (8+8)
 Also draw the minimization result using any one type universal gate only.
- $$f(A, B, C) = \sum m(0, 2, 4, 6, 7, 8, 10, 12, 13, 15) + \sum d(1, 9)$$

- ii) Find the Boolean function implemented in the figure using 4:1 MUX.



Q4

(8+8)

- i) A majority circuit is a combinational circuit whose output is equal to 1 if the input variables have more 1's than 0's. The output is 0 otherwise. Design a 3 input majority circuit.
 ii) Explain BCD adder with necessary diagram.

Q5

(10+6)

- i) Design Mod-3 synchronous counter using JK-flip flop.
 ii) Discuss the working of 4-bit ring counter with circuit diagram and timing diagram.

Q6

(8+8)

- i) Highlight the salient features of ASM chart & explain it by taking a suitable example.
 ii) Illustrate the operation of a serial Decade counter & its timing diagram

Registration No :

--	--	--	--	--	--	--	--	--	--

Total Number of Pages : 02

Course: B.Tech

REC4C002/ REI4C002/ RME4G001

4th Semester Regular/ Back Examination: 2022-23

SUBJECT: Digital Systems Design

BRANCH(S): ECE, ELECTRONICS & C.E, ETC, AEIE, EIE, MMEAM, MECH

Time : 3 Hour

Max Marks: 100

Q.Code : M160

Answer Question No.1 (Part-1) which is compulsory, any eight from Part-II and any two from Part-III.

The figures in the right hand margin indicate marks.

Part-I

- Q1 Answer the following questions: (2 x 10)
- a) Differentiate between Analog and Digital system. What are the advantages of a digital system?
 - b) Using 2's complement perform subtraction ($1000100 - 1010100$).
 - c) Define integrated circuit. What are the characteristics that describe the performance of IC digital logic families?
 - d) Explain why NAND-NAND realization is preferred over AND-OR realization?
 - e) When did the first PLD appear?
 - f) What are gate primitives?
 - g) What are Fan-in and Fan-out?
 - h) The initial state of MOD-16 down counter is 0110. What state will it be after 37 clock pulses?
 - i) In a positive edge triggered JK flip flop, J = 1, K = 0 and clock pulse is rising Q will be _____.
 - j) Which are the basic refresh modes for dynamic RAM?

Part-II

- Q2 Only Focused-Short Answer Type Questions- (Answer Any Eight out of Twelve) (6 x 8)
- a) Explain parity generator and checker with suitable example.
 - b) Design a half adder using at most three NOR gates.
 - c) Describe the read and write cycle of a DRAM. Also describe about the fast page mode.
 - d) Design a combinational circuit that accepts a three-bit binary number and generates an output binary number equal to the square of the input number.
 - e) Calculate analog output of 4-bit DAC for digital input 1011. Assume $V_{FS} = 5V$.
 - f) Design a counter with the following binary sequence. 0, 4, 2, 1, 6 and repeat. Use JK flip-flops.
 - g) With an example explain in detail the test bench creation.
 - h) Discuss the TTL parameters. Draw the TTL inverter circuit.

- i) Design a MOD-10 synchronous counter using T flip flops.
- ii) Compare TTL and CMOS logic families based on following:
 - (a) Propagation delay
 - (b) Power dissipation
- iii) Briefly explain the pulse mode asynchronous sequential circuit.
- iv) Explain the different methods of state assignment.

Part-III

Only Long Answer Type Questions (Answer Any Two out of Four)

- | | | |
|----|---|------|
| Q3 | (a) Design a combinational circuit with four input lines that represent a decimal digit in BCD and four output lines that generate the 9's complement of the input digit. | (08) |
| | (b) Draw and explain logic diagram of arithmetic logic unit (ALU). | (08) |
| Q4 | (a) Using a decoder and external gates, design the combinational circuit defined by the following three Boolean functions:
$F_1 = x'y'z + xz'$
$F_2 = x'yz' + xy'$
$F_3 = xyz' + xy$ | (09) |
| | (b) Explain various steps in the analysis of synchronous sequential circuits with suitable example. | (07) |
| Q5 | (a) Design a 4-bit synchronous 8421-decade counter with ripple carry. | (08) |
| | (b) With respect to Register Transfer logic, explain Inter register transfer with necessary diagrams. | (08) |
| Q6 | (a) Write VHDL program for 4:1 MUX using behavioral modeling. | (10) |
| | (b) Explain PLA with necessary diagrams. | (06) |

Registration No :
206 206

	206			206			206	
--	-----	--	--	-----	--	--	-----	--

Total Number of Pages : 02

B.Tech
RCS3C001

3rd Semester Regular / Back Examination: 2021-22

DIGITAL LOGIC DESIGN

BRANCH(S):CSE, CSEAIME, CST, IT

206 Time : 3 Hour 206

Max Marks : 100

Q.Code : OF748

Answer Question No.1 (Part-I) which is compulsory, any eight from Part-II and any two from Part-III.

The figures in the right hand margin indicate marks.

Q1 206

206 Answer the following questions :

Part-I 206

206

206

206

(2x10)

- a) Define the Figure of Merit of logic families. What is unit to measure the Figure of Merit?
- b) Draw the CMOS circuit for $Y=(a+b)c$.
- c) Represent the decimal number 6027 in BCD, excess-3 and 2421 code.
- d) Perform the following arithmetic operation using 8 bit 2's complement method.
(i) $(-27)+(-61)$, (ii) $(-27)+(+61)$
- e) Draw the logic diagram using only two-input NAND gates to implement the following expression:
$$F=(AB+A'B')(CD'+C'D)$$
- f) A majority circuit is a combinational circuit whose output is equal to 1 if the input variables have more 1's than 0's. The output is zero otherwise. Design a 3 input majority circuit.
- g) Determine the base for the arithmetic operation $\sqrt{41} = 5$.
- h) Construct a 16×1 multiplexer with two 8×1 and one 2×1 multiplexer. Use block diagram.
- i) Explain the Master-slave flipflop. Design a master-slave flipflop using D-FF.
- j) Design a parallel input serial output shift register.

Part-II

Q2

Only Focused-Short Answer Type Questions- (Answer Any Eight out of Twelve)

(6x8)

- a) Define the different characteristics of Digital ICs in detail.
- b) Simplify the function
$$AB'C+B+BD'+ABD'+A'C=B+C$$
- c) Simplify the following Boolean functions using K-map
(i) $F_1(A, B, C, D)=\sum(1,3,4,5,10, 11,12,13,14,15)$
(ii) $F_2(A, B, C, D)=\sum(0,2,3,5,7,8,10,11,14,15)$
- d) Design a Full adder and Full Subtractor circuit with truth table.
- e) Design a sequential circuit with two D flip-flop A and B, and one input 'x'. When $x=0$, the states of the circuit remain the same. When $x=1$, the circuit goes through the state transitions from 00 to 01 to 11 to 10 back to 00, and repeats.

206

206

206

206

206

206

206

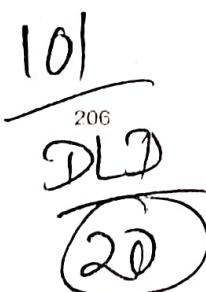
- f) Design S-R flip-flop to J-K flipflop conversion. Find the conversion table. 206
 g) Implement the full subtractor Using single 3:8 decoder. 206 206
 h) Design the ASM charts for the following state transitions:
 (i) If $x=0$, control goes from state T_1 to state T_2 ; if $x=1$, generate a conditional operation and go from T_1 to T_2 .
 (ii) If $x=1$, control goes from T_1 to T_2 and then to T_3 ; if $x=0$, control goes from T_1 to T_3 .
 (iii) Start from state T_1 ; then: if $xy=00$, go to T_2 ; if $xy=01$, go to T_3 ; if $xy=10$, go to T_1 ; otherwise, go to T_3 . 206 206 206
 i) Design a Full adder circuit using two 4 x 1 multiplexers.
 j) Design a 4 bit ring counter and find out it's truth table.
 k) Design a combinational circuit with three inputs x , y , and z , and three outputs, A, B, and C. When the binary Input Is 0, 1, 2, or 3, the binary output is greater than the input. When, the binary Input Is 4, 5, 6, or 7, the binary output is less than the input.
 l) Find out the excitation table and characteristic equation for J-K Flipflop..
 206 206 206 206 206 206

Part-III

Only Long Answer Type Questions (Answer Any Two out of Four)

- Q3 A sequential circuit has two J K FFs A and B, two inputs x and y and one output z . The FF Input equations and circuit output equations are : (16)
 $J_A = Bx + B'y$, $K_A = B'xy'$, $J_B = A'x$, $K_B = A + xy'$, $z = Ax'y' + Bx'y'$
 (i) Draw the logic diagram if the circuit
 (ii) Tabulate the state table
 (iii) Derive the state equations for A and B 206 206 206
- Q4 Design a BCD counter using J-K FF. Design it's excitation table and draw the state diagram. (16)
- Q5 a) Realize $f(a,b,c,d) = \sum(1,3,5,6,8,12,14)$ using 8:1 MUX considering b, c, and d as selection lines. (8)
 b) Using a decoder and external gates, design the combinational circuit using following function. (8)
 $F1 = (y' + x)z$, $F2 = y'z + xy' + y'z$
- Q6 Design a combinational digital circuit for BCD to Excess-3 (XS-3) code converter (16)

206 206 206 206 206 206
 206 206 206 206 206 206
 206 206 206 206 206 206
 206 206 206 206 206 206
 206 206 206 206 206 206



206 206 206 206 206 206
 206 206 206 206 206 206

Registration No.:

206	206	206	206	206	206	206
-----	-----	-----	-----	-----	-----	-----

Total Number of Pages: 02

206 206 206 206

B.Tech

RAE4G001 / REC4C002 / REI4C002 / RME4G001

4th Semester Regular / Back Examination: 2021-22

DIGITAL SYSTEMS DESIGN

BRANCH(S): AERO / ECE, ELECTRONICS & C.E, ETC /
AEIE / MECH, MMEAM

206 206 206

Time: 3 Hour

Max Marks: 100

Q.Code: J449

Answer Question No.1 (Part-I) which is compulsory, any eight from Part-II and any two from Part-III.

The figures in the right hand margin indicate marks.

Q1

Answer the following questions:

(2 × 10)

- What is the largest binary number that can be expressed with 14 bits? Determine the equivalent decimal and hexadecimal numbers.
- Find the complement of $F = wxyz$ and then show that $FF' = 0$.
- Convert decimal 8723 to both BCD and ASCII codes. For ASCII an even parity bit is to be appended at the left.
- What is the significance of state assignment?
- Differentiate between a priority encoder and conventional encoder.
- What is a programmable logic array? How it is different from ROM?
- How many flip-flops will be complemented in a 10-bit ripple counter to reach the next count after the count of '1001100111'.
- Outline critical race.
- List any two specifications of IC-DAC 0808.
- A standard TTL has following specification:
 $I_{OH} = 400\mu A$, $I_{OL} = 40\mu A$, $I_{OL} = 16mA$, $I_L = 1.6mA$. calculate the fanout.

Part-I

Q2

Only Focused-Short Answer Type Questions- (Answer Any Eight out of Twelve) (6 × 8)

- Implement the Boolean function $F = xy + x'y' + y'z$ using NOR and inverter gates.
- How is the error detection and correction carried out using parity method in digital data transmission?
- Design a four-bit BCD adder using IC 7483 and NAND gates only.
- Implement a 4:1 MUX circuit using VHDL.
- A computer uses RAM chips of 1024x1 capacity. How many chips are needed and how should their address lines be connected to provide a memory capacity of 1024 bytes.
- Implement the Boolean function with PLA
 $F_1(A, B, C) = \Sigma(0, 1, 2, 4)$
- Explain a CMOS NAND gate.
- A clocked sequential circuit with single input X and single output Z produces $Z=1$ whenever X completes the sequence 1011 and overlapping is allowed. Obtained

206

206

206

206

206

206

206

the state diagram.

- i) Design a 3-bit synchronous counter and draw the output waveform. 206
j) Design a sequence detector that may detect both 110 and 101 using Moore model. 206
k) Compare TTL and CMOS logic families based on following:
(a) Propagation delay (b) Power dissipation
l) Calculate analog output of 4-bit DAC for digital input 1011. Assume $V_{FS} = 5V$. 206

Part-III

- Q3 206 Only Long Answer Type Questions (Answer Any Two out of Four) 206 206
a) The logical sum of all the minterms of Boolean function of n variables is 1. Prove the above statement for n=3. (7)
b) Minimize the Boolean expression $F = AB'C' + C'D + BD' + A'C$ using K-map and implement the logic circuit using NAND gates only. (9)
- Q4 a) Implement the following function with a MUX 6
 $F(A, B, C, D) = \Sigma(0, 1, 3, 4, 8, 9, 15)$
b) Construct a 5-to-32-line decoder with four 3-to-8-line decoders with enable and a 2-to-4-line decoder. Use block diagrams for the components. 10 206
- Q5 a) Describe the read and write cycle of a DRAM. Also describe about the fast page mode? (8)
b) What is a glitch? Show the timing diagram for a Mod 6 asynchronous counter showing the glitches in the diagram. (8)
- Q6 a) Design a counter with the following repeated binary sequence: 0, 1, 2, 4, 6. Use D flip-flops. 10 206
b) The output of 8-bit DAC varies between +10V and -10V. Calculate the following:
i) Resolution ii) Percentage resolution. (6)

206

206

206

206

206

206

206

206

206

206

206

206

206

206

206

206

206

206

206

206

206

206

206

206

206

206

206

206

Registration No :
206

206	206	206	206	206	206	206
-----	-----	-----	-----	-----	-----	-----

206

Total Number of Pages : 02

B.Tech

RBM4C001 / REE4C001 / REL4C001

4th Semester Regular / Back Examination: 2021-22

DIGITAL ELECTRONICS

BRANCH(S): BIOMED / EEE / ELECTRICAL

206

206

206

Time : 3 Hour

206

206

206

Max Marks : 100

Q.Code : J522

Answer Question No.1 (Part-1) which is compulsory, any eight from Part-II and any two from Part-III.

The figures in the right hand margin indicate marks.

Q1 Answer the following questions : (2 x 10)

- a) Determine the octal equivalent number of $(A \cdot B)_{16}$.
- b) What is the equivalent simplified result of the Boolean function $z=a'b' + ab + a'b$?
- c) Why 1's & 2's compliments are required in digital electronics.
- d) How many 3 to 8 line decoders with an enable input are needed to construct a 6 to 64 line decoder without using any other logic gates?
- e) Compare MUX with DMUX.
- f) The output of a J-K flip-flop is 0. Its output does not change when a clock pulse is applied. What can be the inputs J and K are respectively ?
- g) What is the minimum number of D flip-flops needed to design a mod-25 counter?
- h) Compare PLA & PAL.
- i) What are the applications of EX-OR gate?
- j) What is the drawback of SR-FF & draw the required circuit diagram overcome to it.

Part-II

Q2 Short Answer Type Questions- (Answer Any Eight out of Twelve) (6 x 8)

- a) Simplify $f(x, y, z) = \prod M(0, 4, 6, 7, 8, 10, 12, 13, 15)$ using K-map
- b) Draw the truth table & circuit for full subtractor.
- c) Implement the given functions using single 3:8 decoder.

$$f_1(A, B, C) = \prod(2, 3, 4, 5, 7)$$

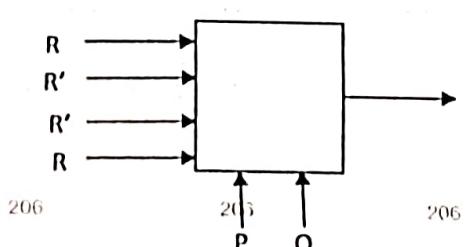
$$f_2(A, B, C) = \sum(1, 3, 5)$$

- d) What is the Boolean expression for the output of the 4:1 MUX shown below.

206

206

206



206

206

206

206

206

206

206

206

206

206

206

- e) Find out the POS result of $x = a'b' + ab$ 206 206 206 206
- f) Design a 2 bit synchronous up/down counter
- g) Explain operation of 4-bit SIPO register with necessary diagram.
- h) Explain Mod-3 ripple counter operation with neat diagram & waveform.
- i) Design a magnitude comparator to compare two 2-bit binary numbers: A=A₁A₀ and B=B₁B₀. There should be three outputs: A>B, A=B, A<B.
- j) Convert D-Flipflop to SR-Flip flop with required Truth table & K-map analysis.
- k) Explain Sample & hold circuit with neat diagram. 206 206 206
- l) Explain operation of CMOS logic circuit with required diagram.

Part-III

Long Answer Type Questions (Answer Any Two out of Four)

- Q3** a) Obtain the simplified form for the given expression using K-map. Draw the minimization result using any one type universal gate only. (8)
206 $f(A, B, C) = \sum m(0, 2, 4, 6, 7, 8, 10, 12) + \sum d(1, 9)$ 206 206
- b) Find the Boolean function for 1:4 DMUX. Implement it using basic logic gates (8)
- Q4** a) A majority circuit is a combinational circuit whose output is equal to 1 if the input variables have more 1's than 0's. The output is 0 otherwise. Design a 3 input majority circuit. (8)
- b) Explain BCD adder with necessary diagram. (8)
- Q5** a) Design Mod-5 synchronous counter 206 206 206 206 (8)
b) Discuss the working of 4-bit Ring counter with circuit diagram and timing diagram. (8)
- Q6** a) Design A/D converter using voltage to frequency converter with required wave form analysis. (8)
- b) Discuss ROM organization structure & FPGA in details. (8)

206 206 206 206 206 206 206 206

206 206 206 206 206 206 206 206

206 206 206 206 206 206 206 206

Registration No :

--	--	--	--	--	--	--	--

Total Number of Pages : 02

B.Tech
RCS3C001

206 3rd Semester Regular Examination 2019-20

DIGITAL LOGIC DESIGN

BRANCH : CSE, IT

Max Marks : 100

Time : 3 Hours

Q.CODE : HR837

Answer Question No.1 (Part-I) which is compulsory, any EIGHT from Part-II and any TWO from Part-III.

The figures in the right hand margin indicate marks.

Q1

Part-I

Only Short Answer Type Questions (Answer All-10)

(2 x 10)

a) The solutions to the quadratic equation $x^2 - 11x + 22 = 0$ are $x = 3$ and $x = 6$.

b) What is the base of the numbers?

c) In K-Map, the larger number of cells that we group will produce better results. Why?

d) What is the difference between standard form (sum of product) and canonical form (sum of minterm)?

e) What is the function of XOR properties that are useful in digital logic?

f) State the uses of decoders.

g) Draw a combinational logic circuit, which can compare whether two bits binary numbers are same or not?

h) Define race around condition.

i) Explain the flip-flop excitation tables for T flip-flop.

j) Give the comparison between synchronous & asynchronous sequential circuits?

k) What is the cause for essential hazards?

Part-II

Q2

Only Focused-Short Answer Type Questions- (Answer Any Eight out of Twelve)

(6 x 8)

a) Design an 8421 to gray code converter.

b) Simplify the following Boolean expressions, using four-variable maps:
 $A'B'C'D' + BC'D + A'C'D + A'BCD + ACD'$

c) Implement the following Boolean function with a 4 x 1 multiplexer and external gates:
 $F(A, B, C, D) = \Sigma(1, 3, 4, 11, 12, 13, 14, 15)$.

d) Differentiate between a MUX and DEMUX.

e) Design a Half subtractor using only NOR gates.

f) Draw a logic diagram of a 4 bit ripple counter using D- flip flop.
List some applications of ripple counter.

g) Design a synchronous 3-bit gray code up counter with the help of excitation table.

h) What are the various types of shift registers?

i) Explain each

j) Explain various steps in the analysis of synchronous sequential circuits with suitable example.

k) Explain the Master-slave S-R Flip-flop with logic diagram, truth table and timing diagram.

l) What are the steps in the analysis and design of asynchronous sequential circuits?
Explain with an example.

m) Find a circuit that has no static hazards and implements the Boolean function :

$F(A,B,C,D) = \Sigma(0,2,6,7,8,10,12)$

Part-III

Only Long Answer Type Questions (Answer Any Two out of Four)

- Q3** a) State and prove De-Morgan's theorem 1st and 2nd with logic gates and truth table. (8)
b) Which gates can be used as inverters in addition to the NOT gate and how? Explain and justify your answer. (8)
- Q4** a) Draw a block diagram, truth table and logic circuit of a 16 x 1 multiplexer and explain its working principle. (8)
b) Design a half adder logic using only NOR gate. (8)
- Q5** a) Design the 4 bit Synchronous up/down counter with timing diagram, logic diagram and truth table. (8)
b) Explain the Master-slave S-R Flip-flop with logic diagram, truth table and timing diagram. (8)
- Q6** a) Discuss salient features of ASM chart. (8)
b) Discuss Quine-McCluskey Design Procedure. (8)

Registration No :

--	--	--	--	--	--	--	--	--

Total Number of Pages : 02

B.Tech
PEE4I103

4th Semester Regular / Back Examination 2018-19

DIGITAL ELECTRONICS CIRCUITS

BRANCH : ELECTRICAL

Max Marks : 100

Time : 3 Hours

Q.CODE : F486

Answer Question No.1 (Part-I) which is compulsory, any eight from Part-II and any two from Part-III.

The figures in the right hand margin indicate marks.

Part- I

- Q1 Only Short Answer Type Questions (Answer All-10) (2 x 10)**
- a) What is a single precision-Floating-point representation of numbers?
 - b) Differentiate between active high and active low terms associated with inputs and outputs.
 - c) According to you, which circuits are called as universal combinational circuits?
 - d) Design a 2-bit equality detector, mention the functions used.
 - e) How can you convert a decoder to demultiplexer?
 - f) Among RAM and ROM which is widely used in current applications of data storage?
 - g) Write the significance of Boolean algebra in digital circuits.
 - h) How D/A conversion takes place?
 - i) Explain the significance of gray and binary code.
 - j) Prove the identity, $1+X+Y+\dots = 1$, using truth-table.

Part- II

- Q2 Only Focused-Short Answer Type Questions- (Answer Any Eight out of Twelve) (6 x 8)**
- a) Explain the operation of a 4-bit SIPO shift register using flip-flops and the timing diagram.
 - b) Design a 32:1 MUX using 4:1 MUX(s) only. Mention the LSB and MSB in the diagram.
 - c) Using NOR gates only, design Y (A,B,C)= AB+ BC' + ABC.
 - d) Design a Decade counter that counts up.
 - e) Design a 4-bit active low input decoder circuit. Show the truth table. Draw the necessary circuit.
 - f) Express the complement of the following function in product-of-sum form.
 $F(A, B, C, D)= \pi(1,5,6,7,9,11,12)$
 - g) Explain the properties of TTL logic family in details.
 - h) How will you convert a SR flip-flop to T flip-flop and vice-versa? Show the necessary tables and draw the diagrams.
 - i) Given two numbers, A= 1110100 and B= 1011011, perform the subtraction A-B and B-A using 1's complement method.
 - j) Design a 4x3 binary multiplier circuit.
 - k) Explain the Master-Slave operation using D flip-flop. Draw the necessary circuit diagrams.
 - l) Differentiate between registers and shift registers. Give examples.

206 206 206 206 206 206 206

Part-III

- Q3** **a)** Only Long Answer Type Questions (Answer Any Two out of Four) **(8)**
Find all the prime implicants of the following function :
 $F(A, B, C, D) = \sum(0, 2, 4, 5, 6, 7, 8, 10, 13, 15)$. Mention all the desired minimizations. **(8)**
- b)** Minimize the function: $F(w, x, y, z) = \sum(4, 5, 6, 7, 12, 13, 14)$, $d(w, x, y, z) = \sum(1, 9, 11, 15)$ **(8)**
- Q4** Design a 4-bit up-down asynchronous counter using a negative edge-triggered JK flip-flop. Consider the two asynchronous inputs and a synchronous clock. Draw the state diagram, necessary tables and final circuit diagram. **(16)**
- Q5** Using CMOS logic, implement the function $F(A, B, C) = (A+B)(B+C)(A+C)$. Draw the circuit diagram. Explain the operation. **(16)**
- Q6** **a)** Explain the A/D and D/A conversion. **(10)**
b) Differentiate between PAL and PLA. **(6)**

206 206 206 206 206 206 206 206

206 206 206 206 206 206 206 206

206 206 206 206 206 206 206 206

206 206 206 206 206 206 206 206

206 206 206 206 206 206 206 206

206 206 206 206 206 206 206 206