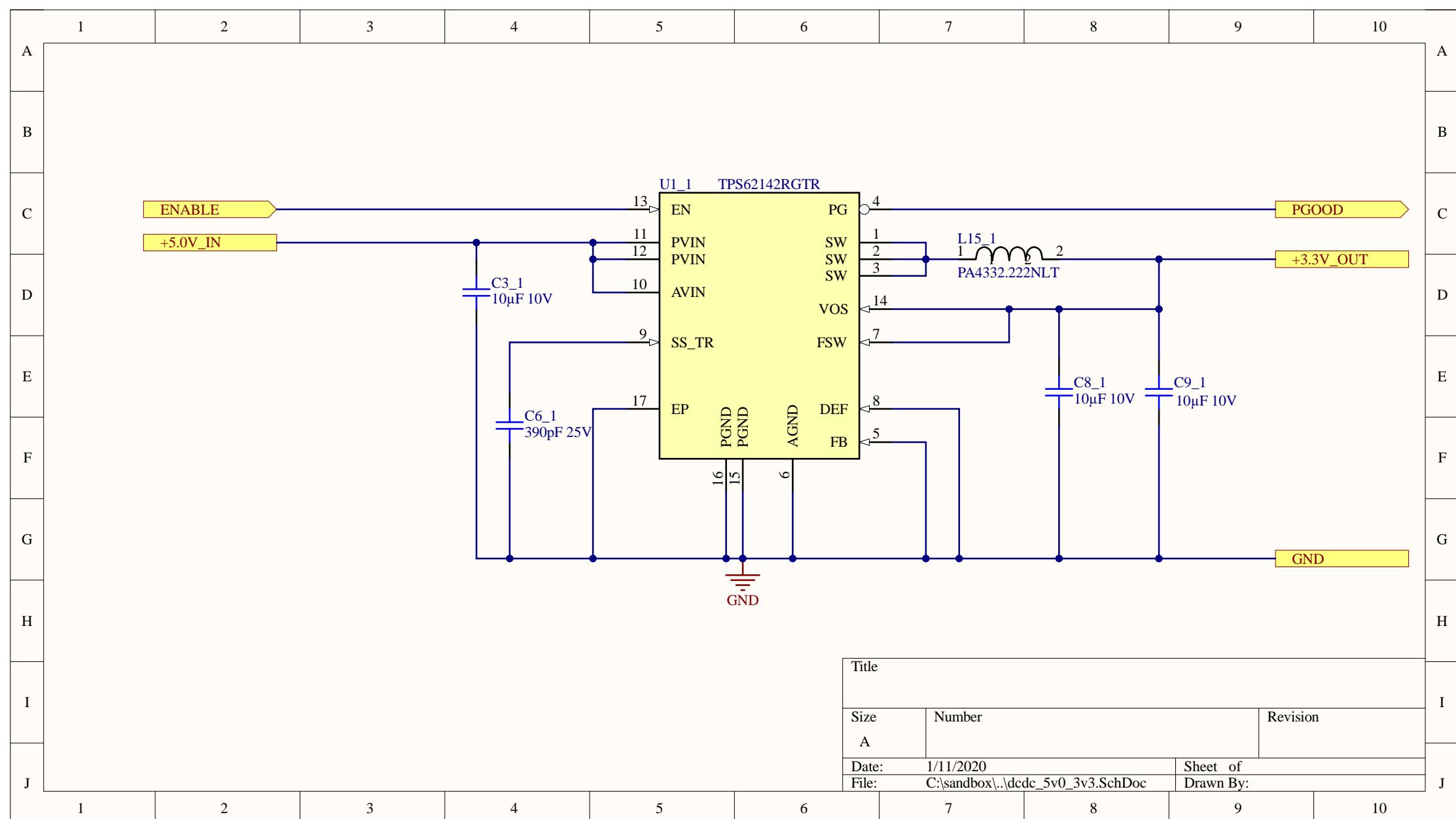
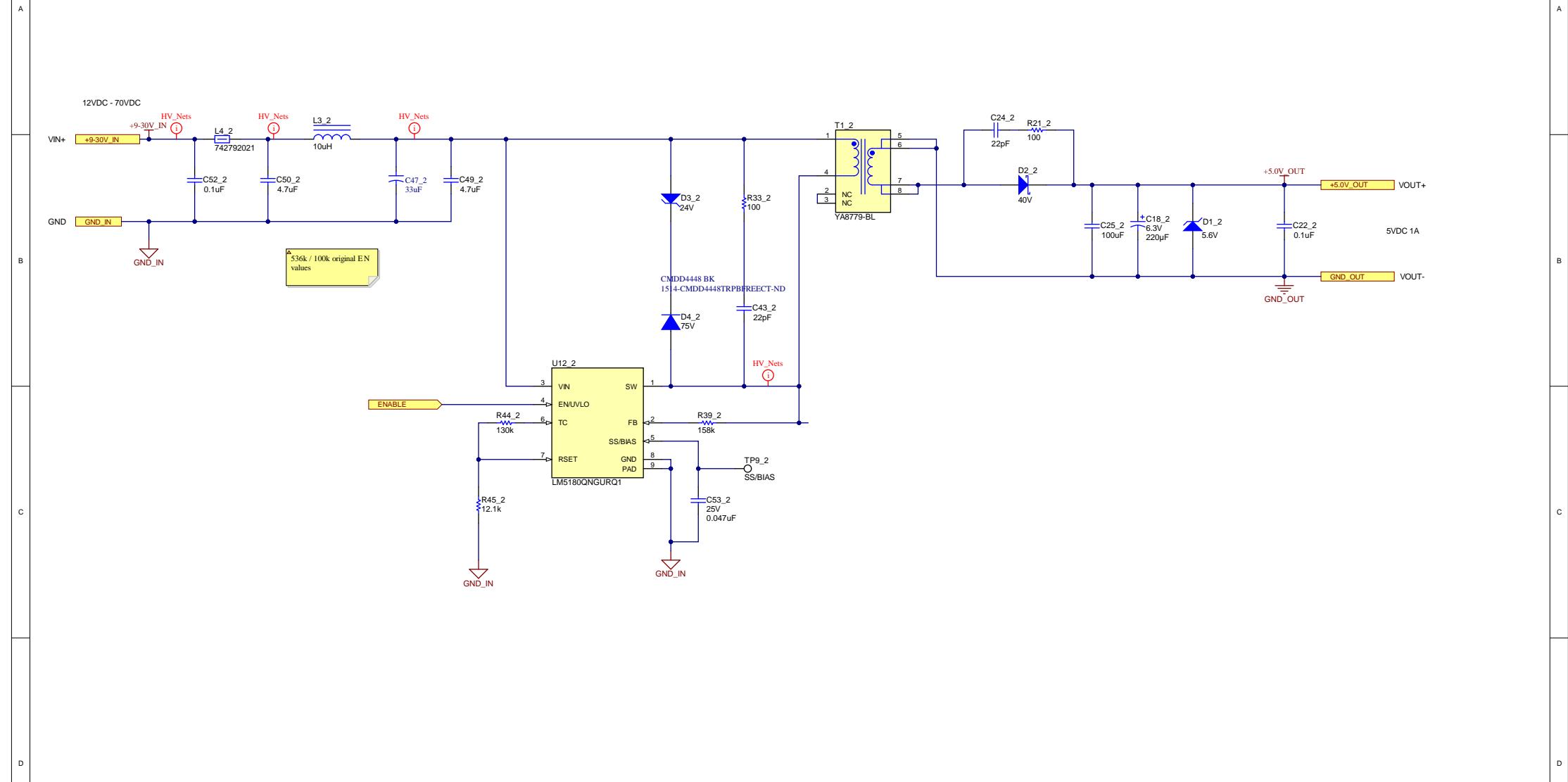


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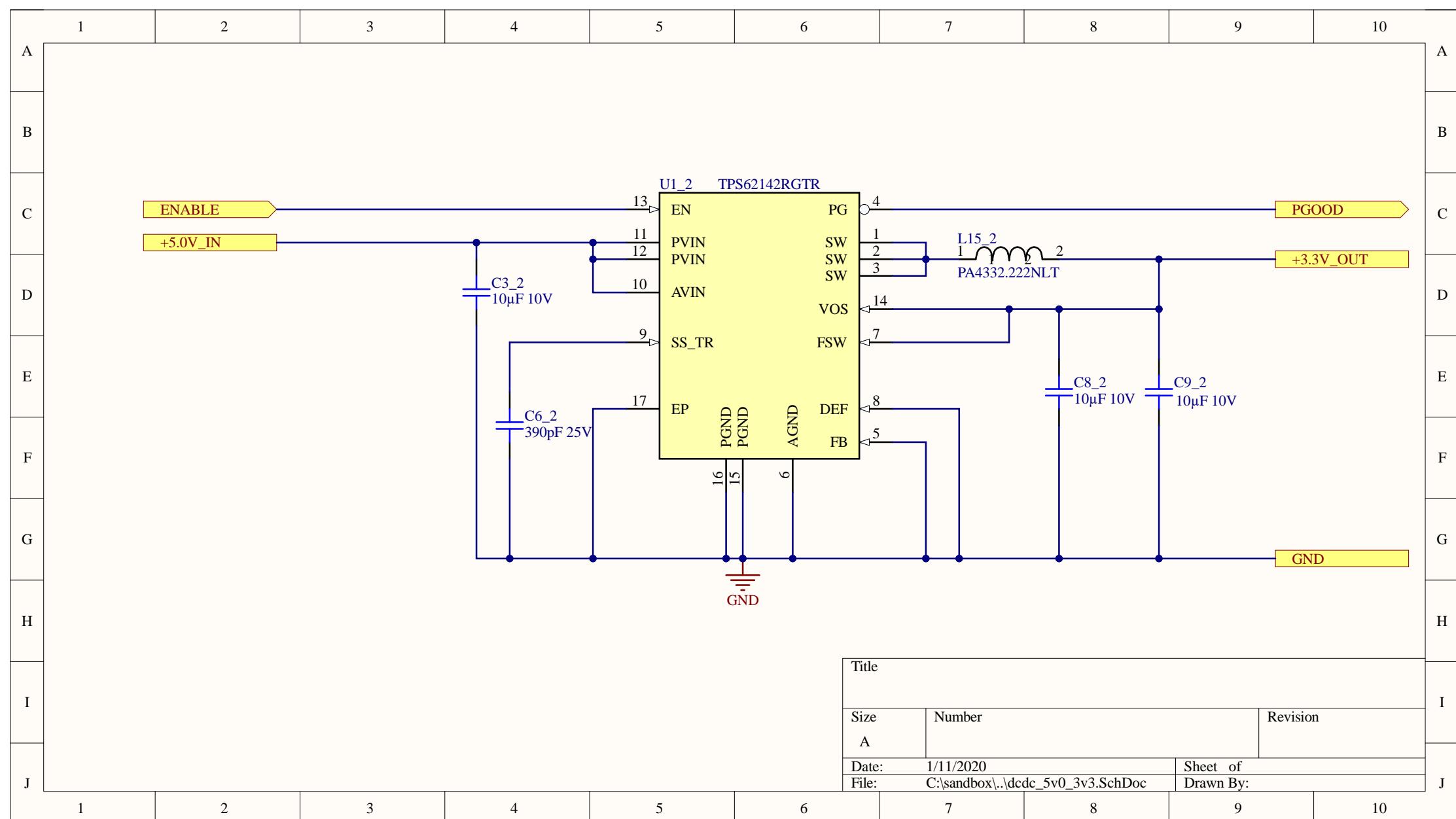
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Drawn By: K Nielson	File: IsoDcDc-BSR033A.SchDoc	Size: B
Engineer:	Contact:	© Texas Instruments http://www.ti.com

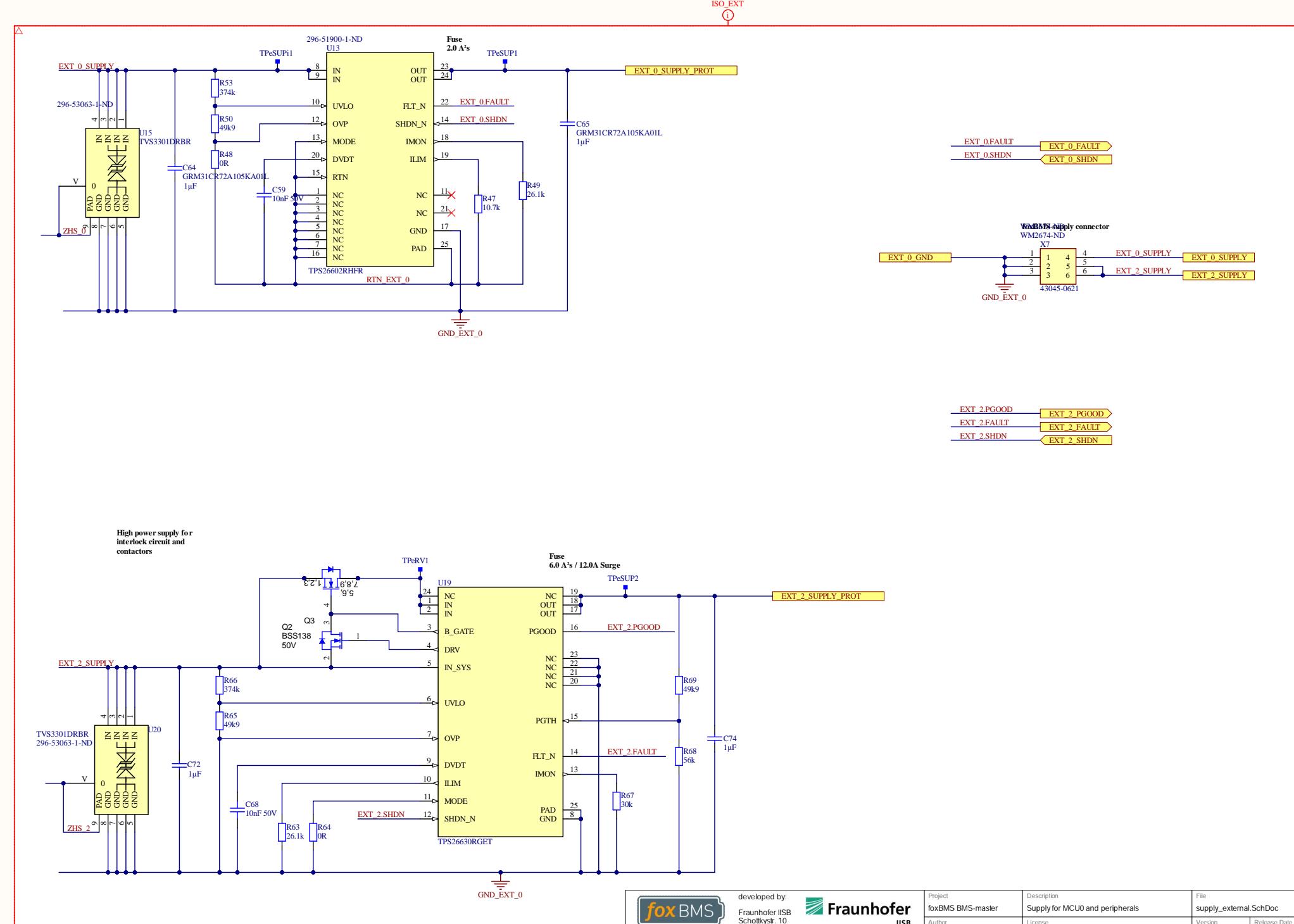




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SVN Rev:	458e69da68d0267e2b11 [Version: 458e69da68d0267e2b11 (Locally Modified)]	Sheet 1 of 2
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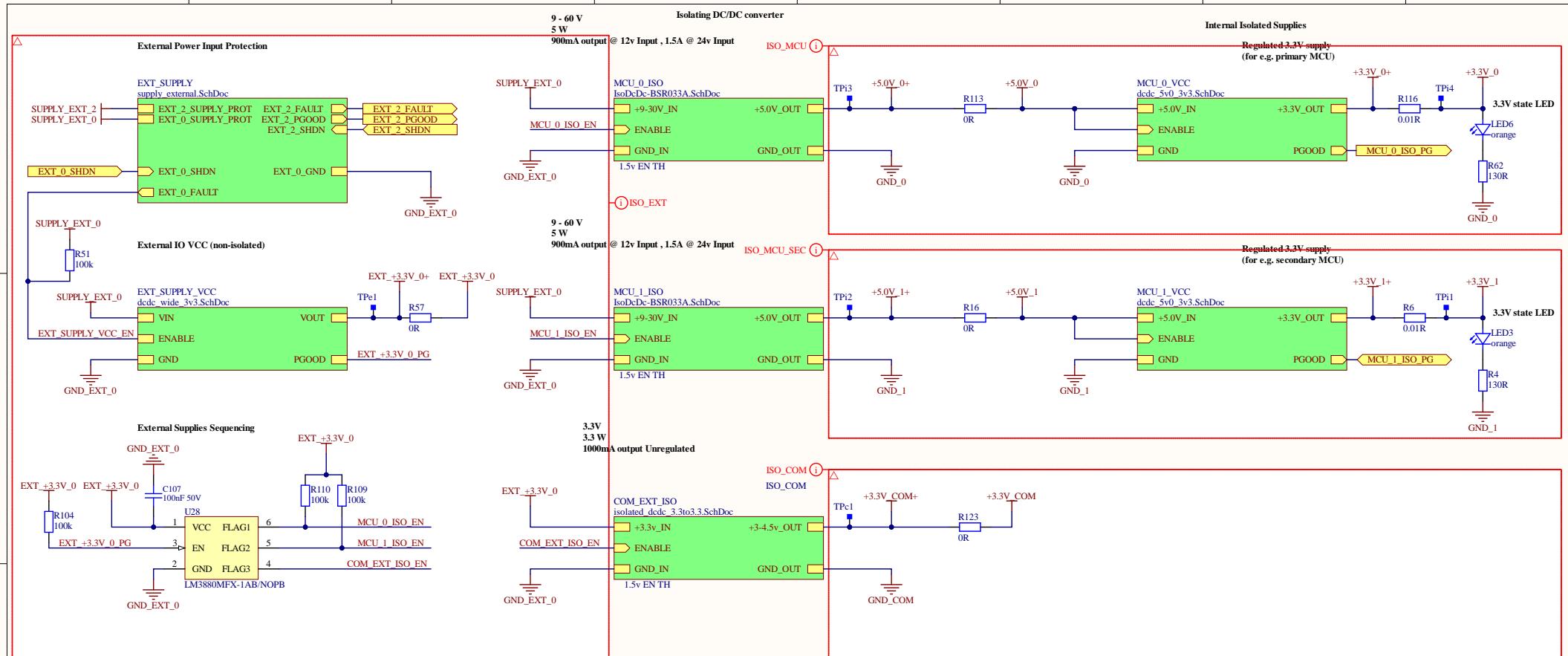
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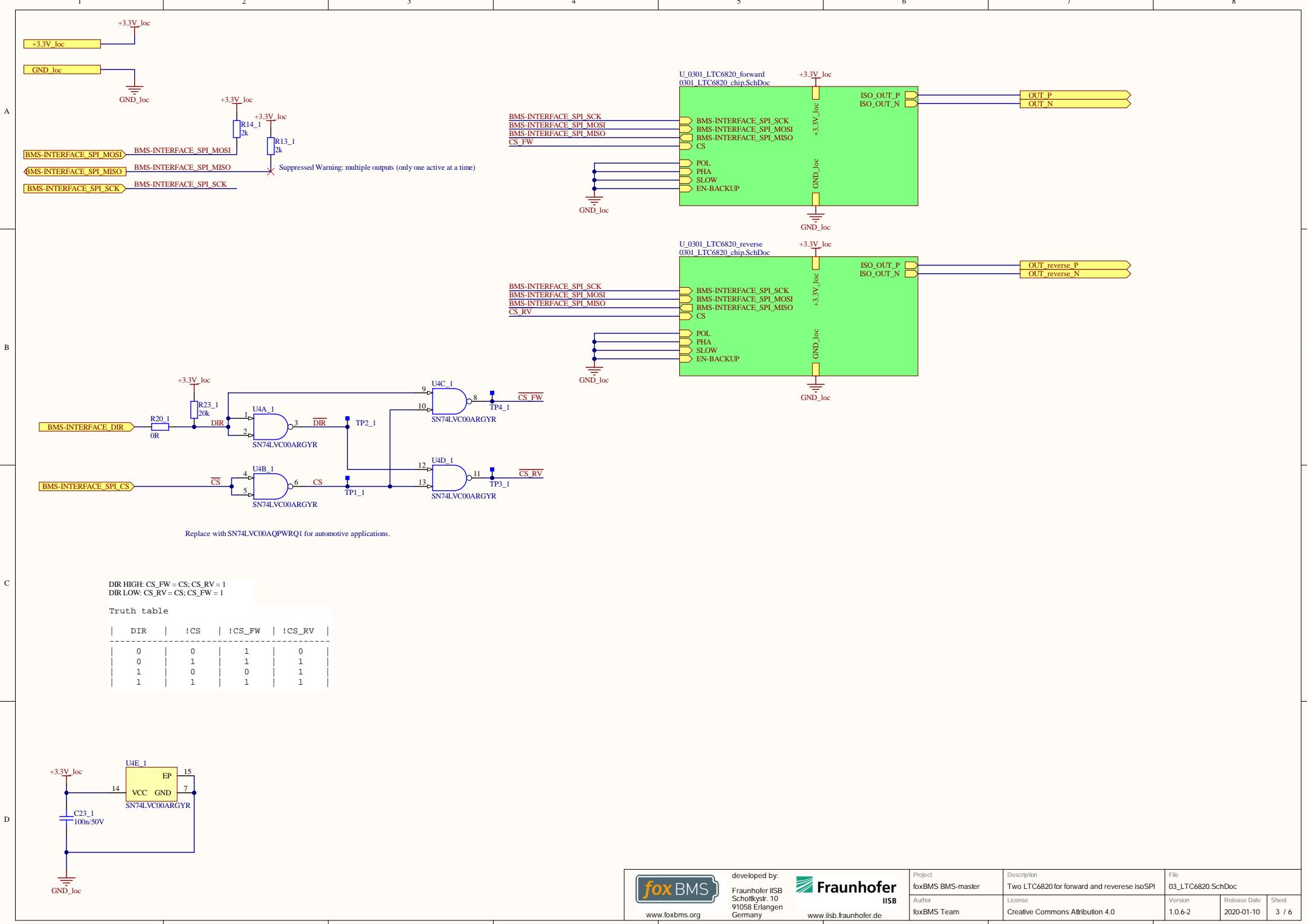
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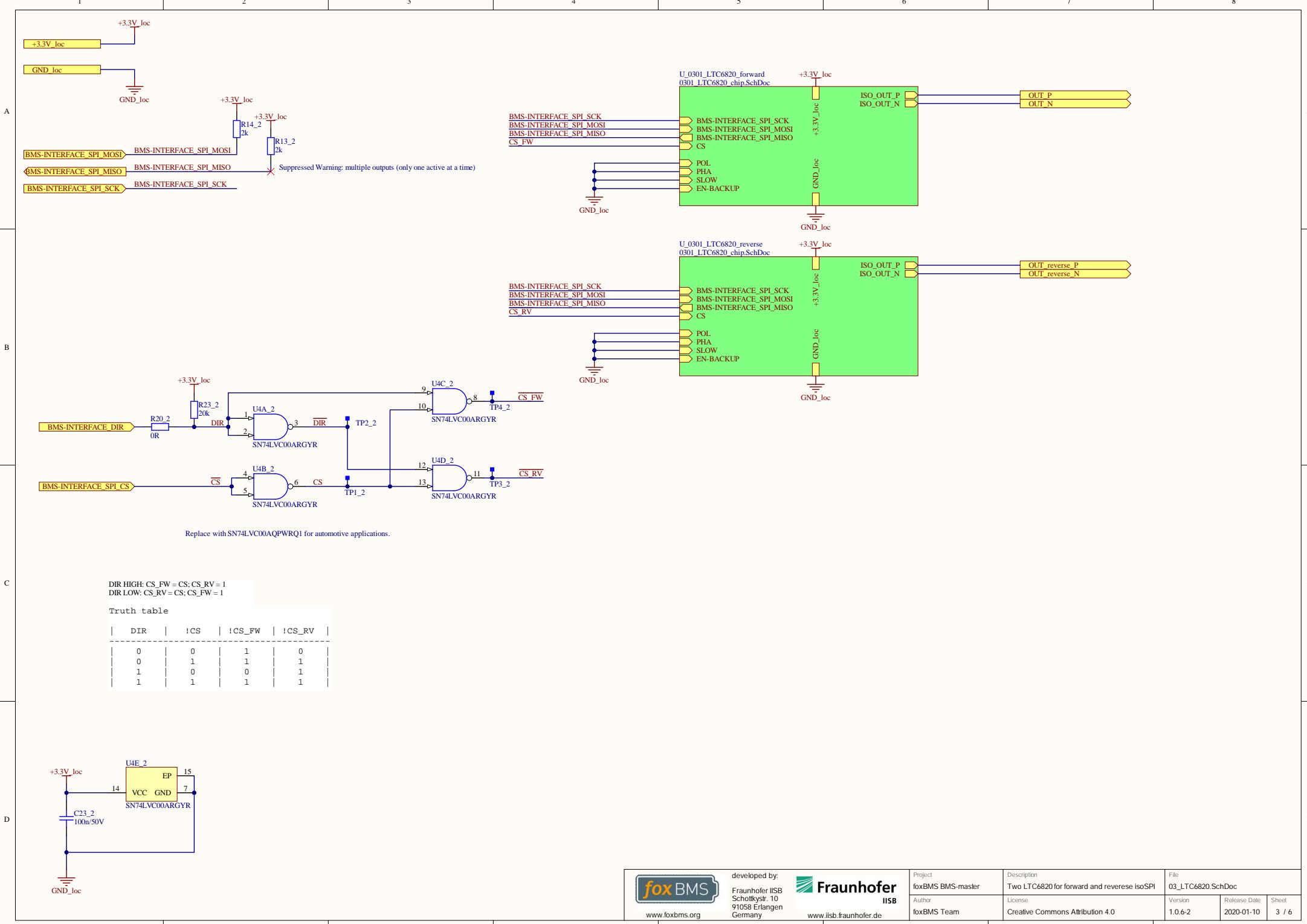
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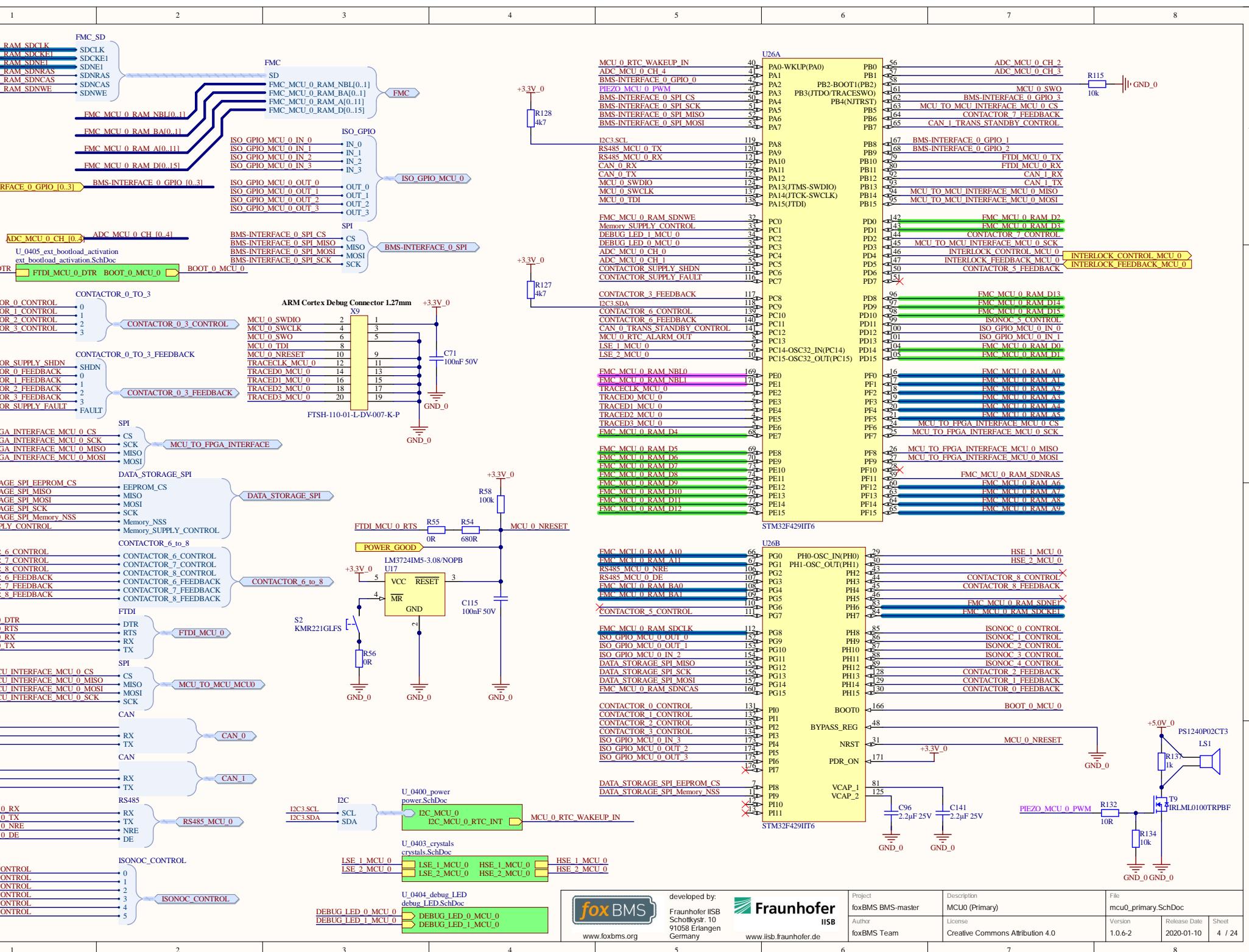
Fraunhofer
IISB

developed by:	Project	Description	File
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Author	License	Version	Release Date
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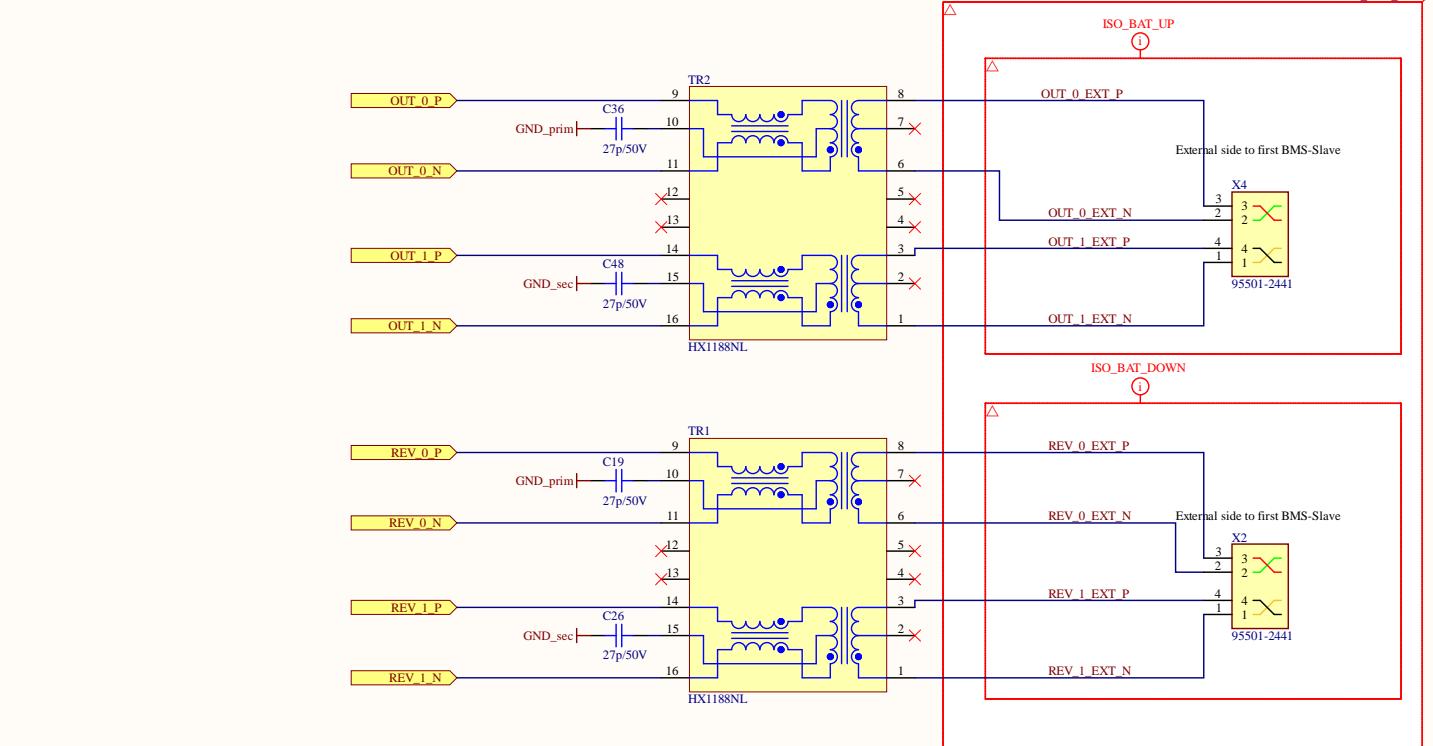








GND_prim — GND_prim
GND_sec — GND_sec



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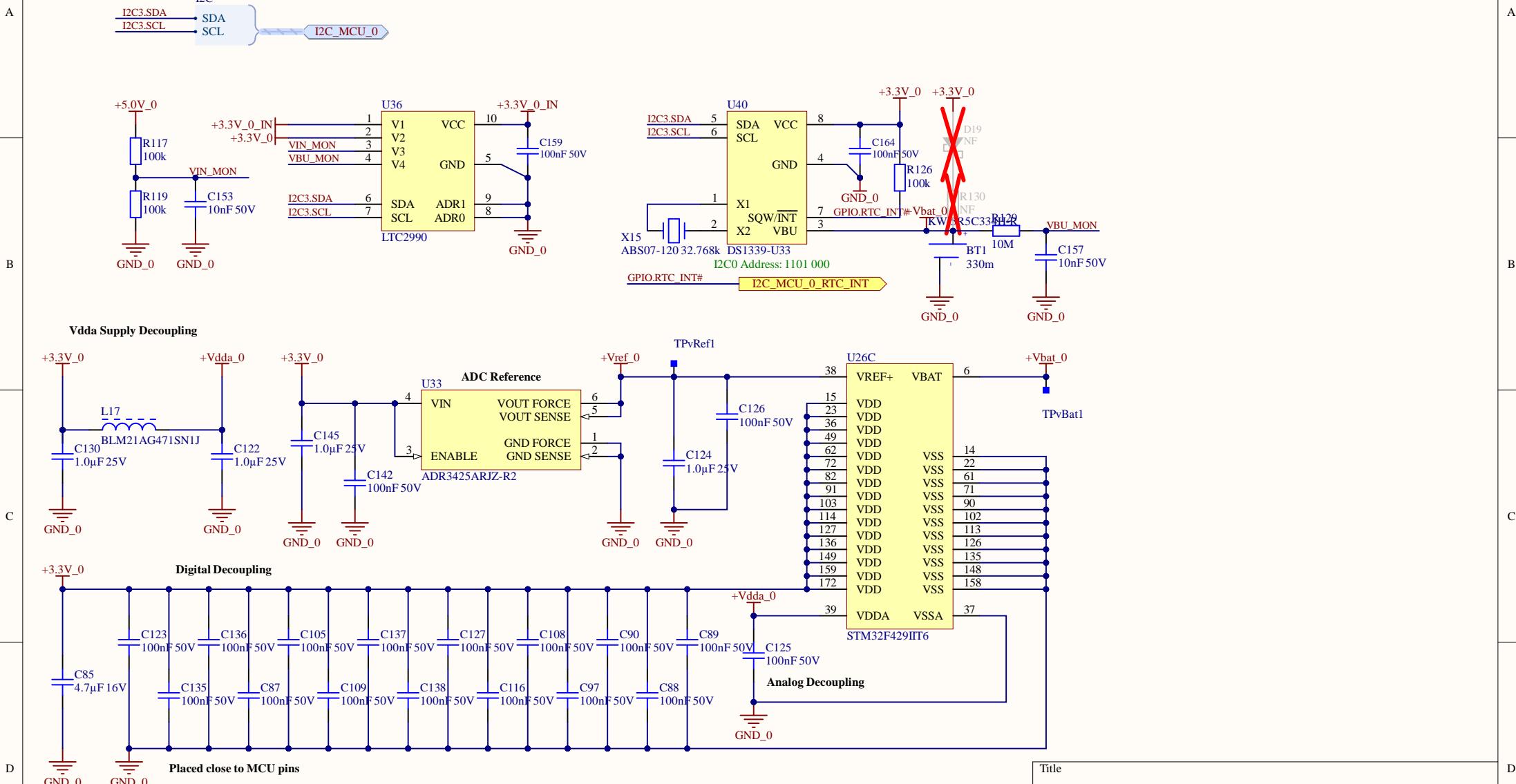
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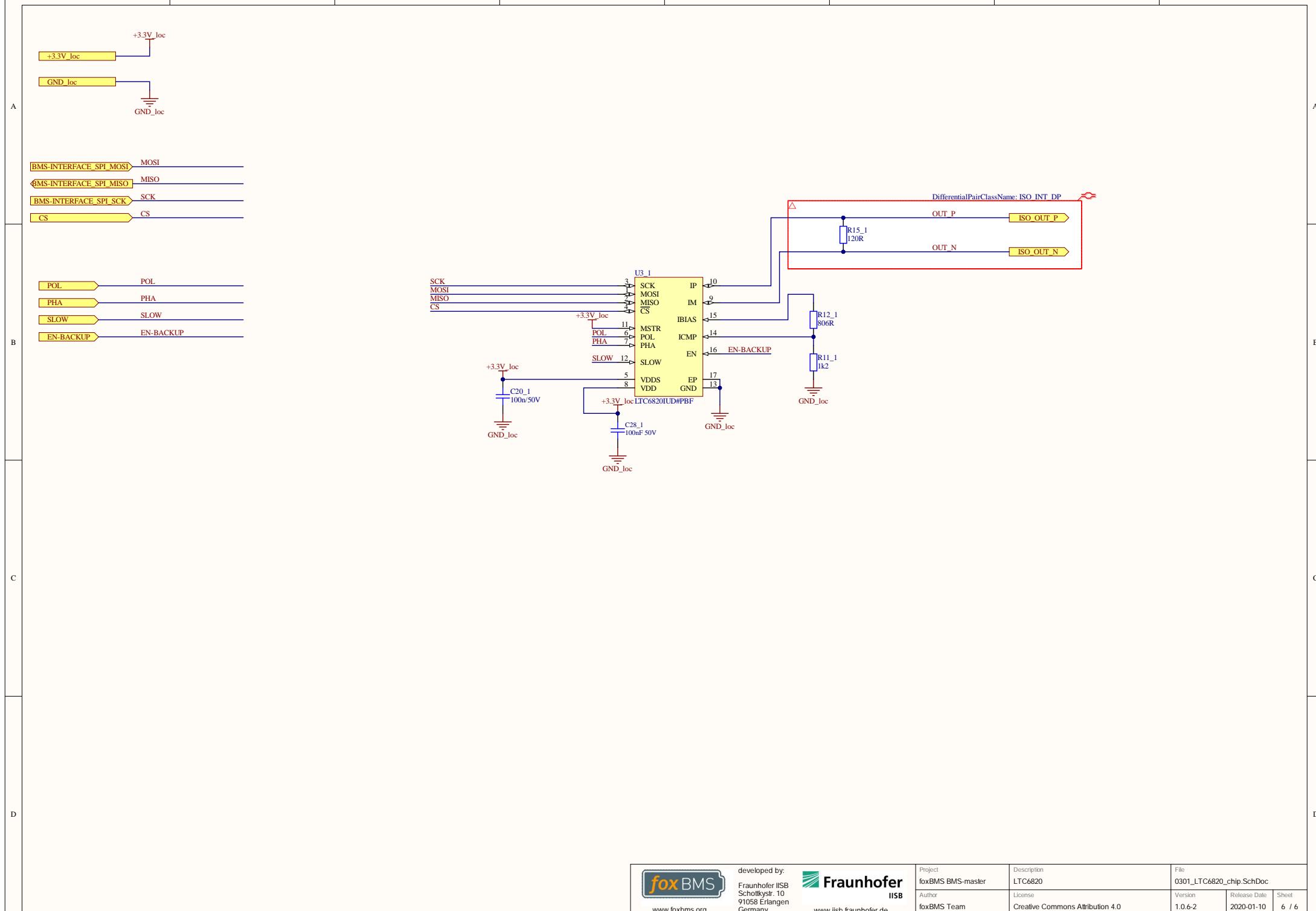
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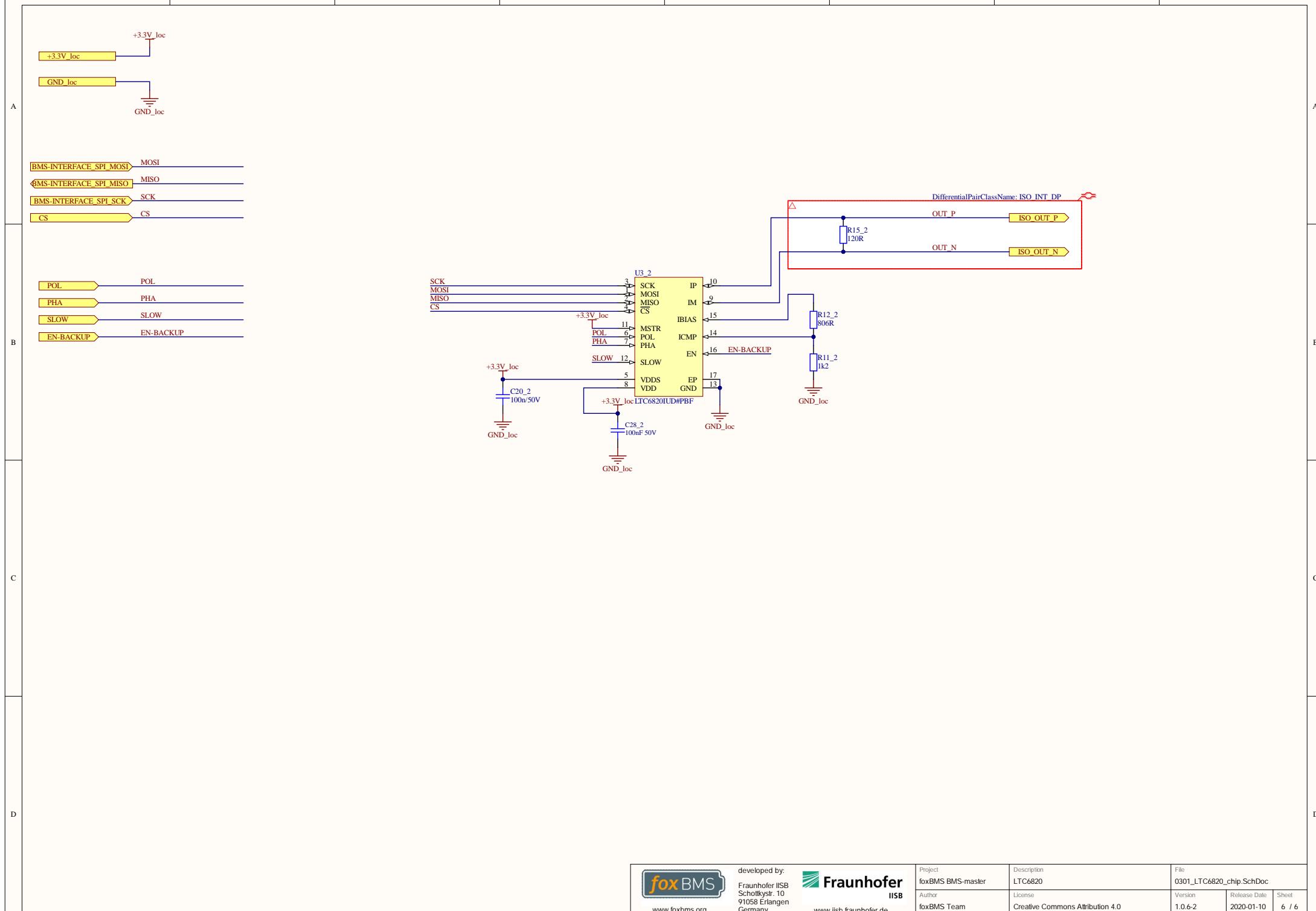
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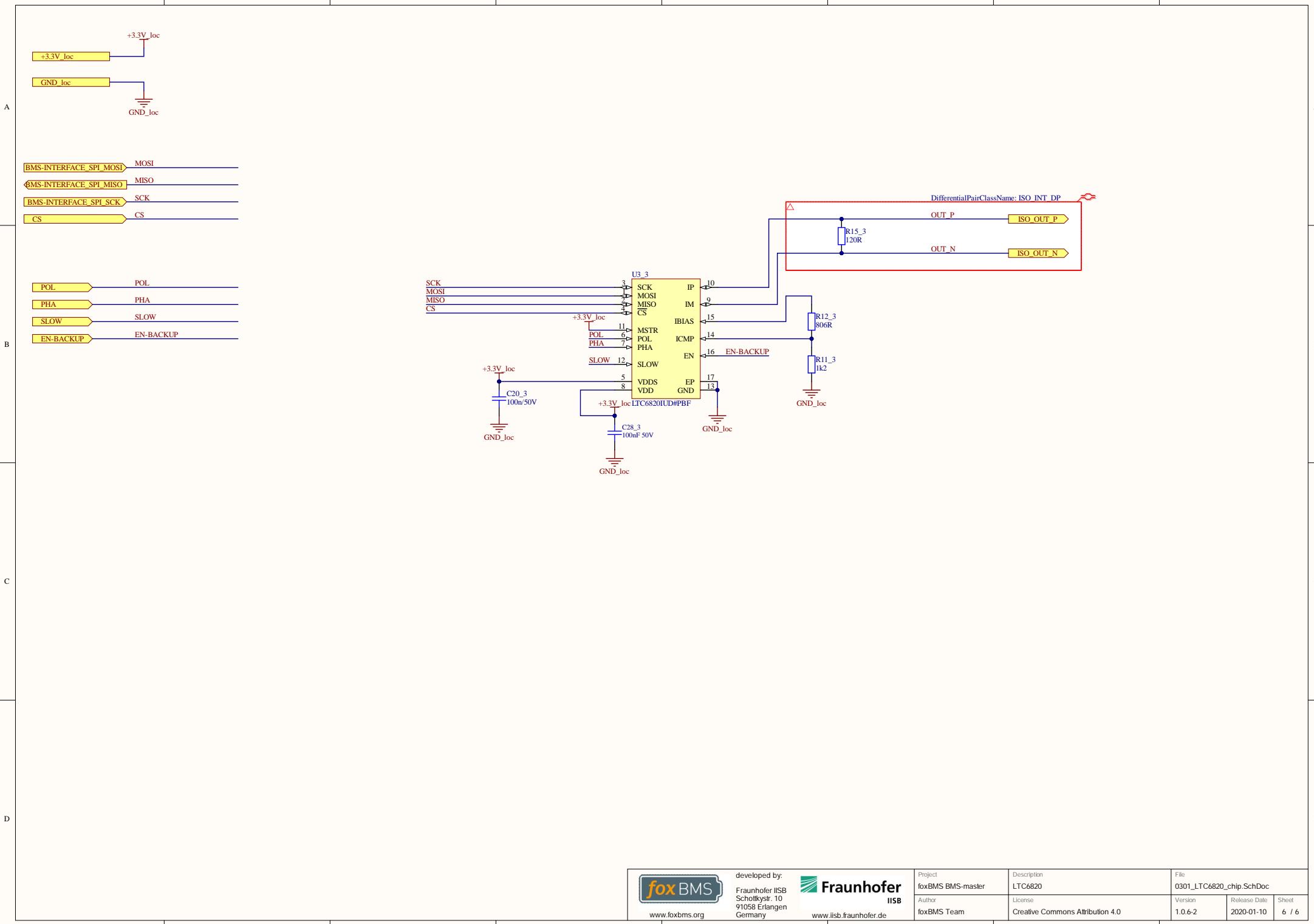
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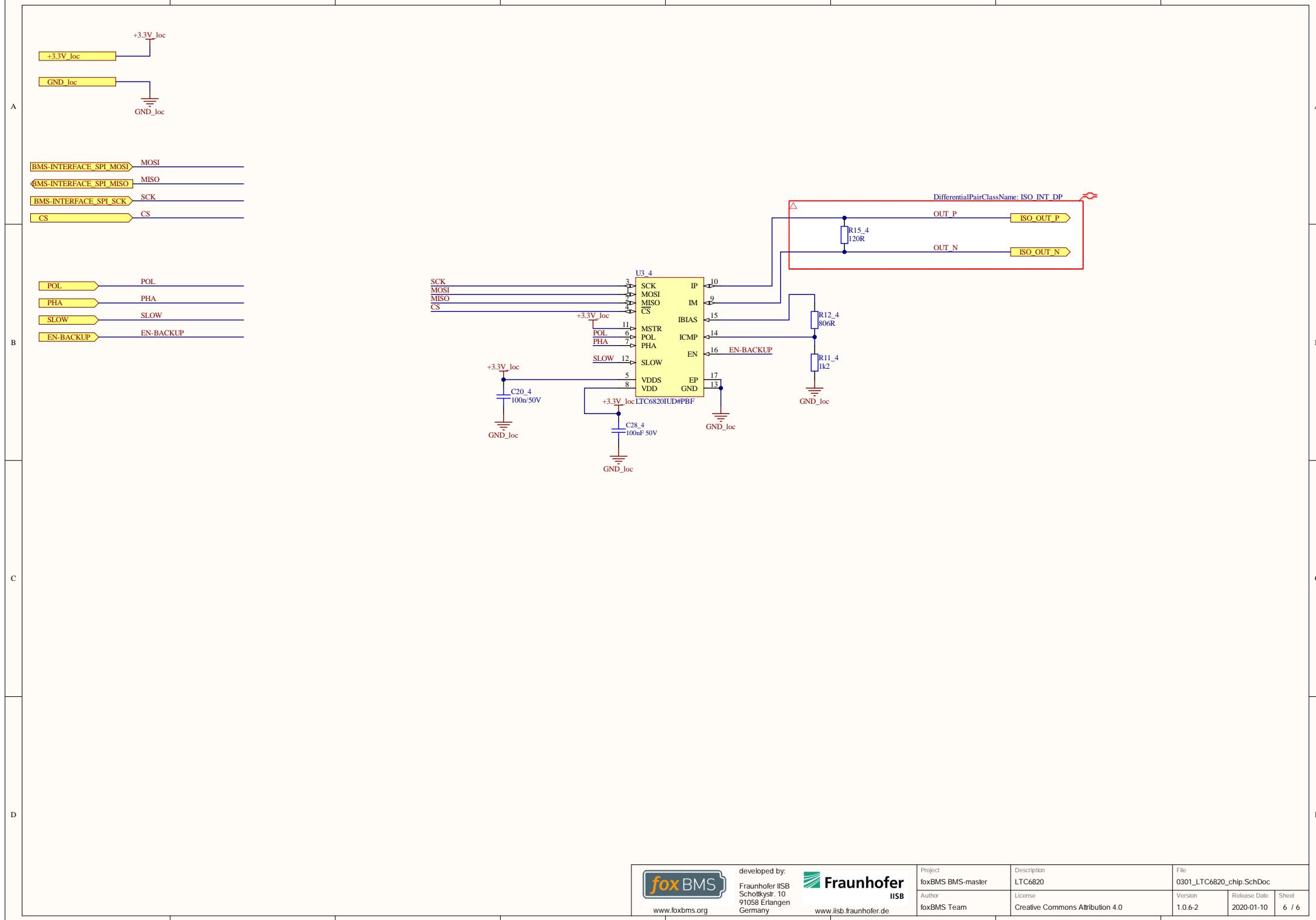


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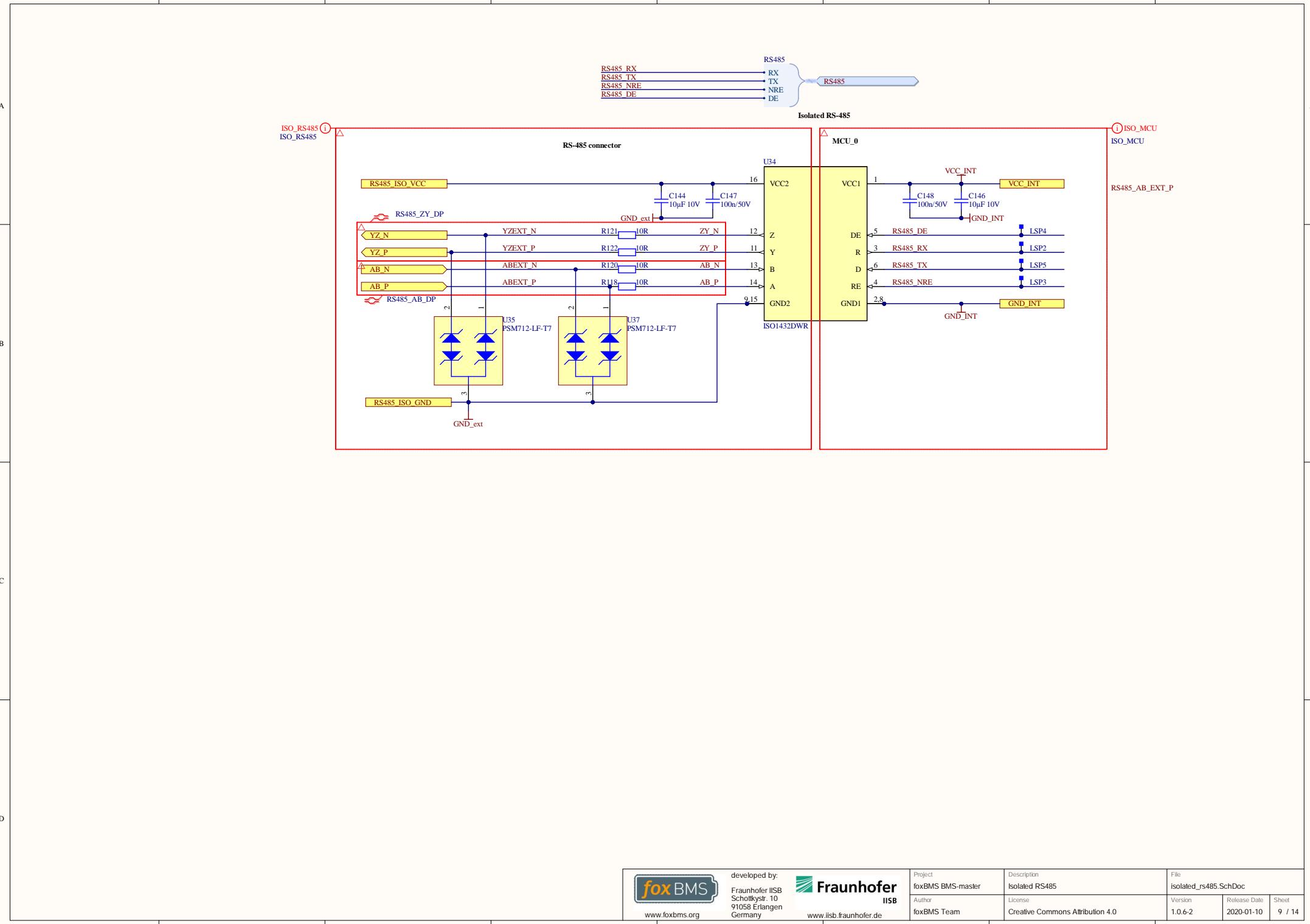
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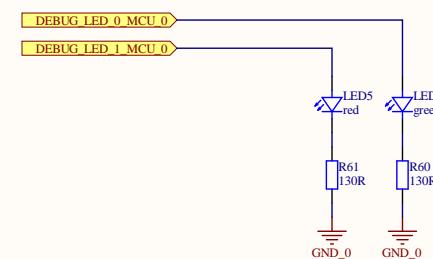
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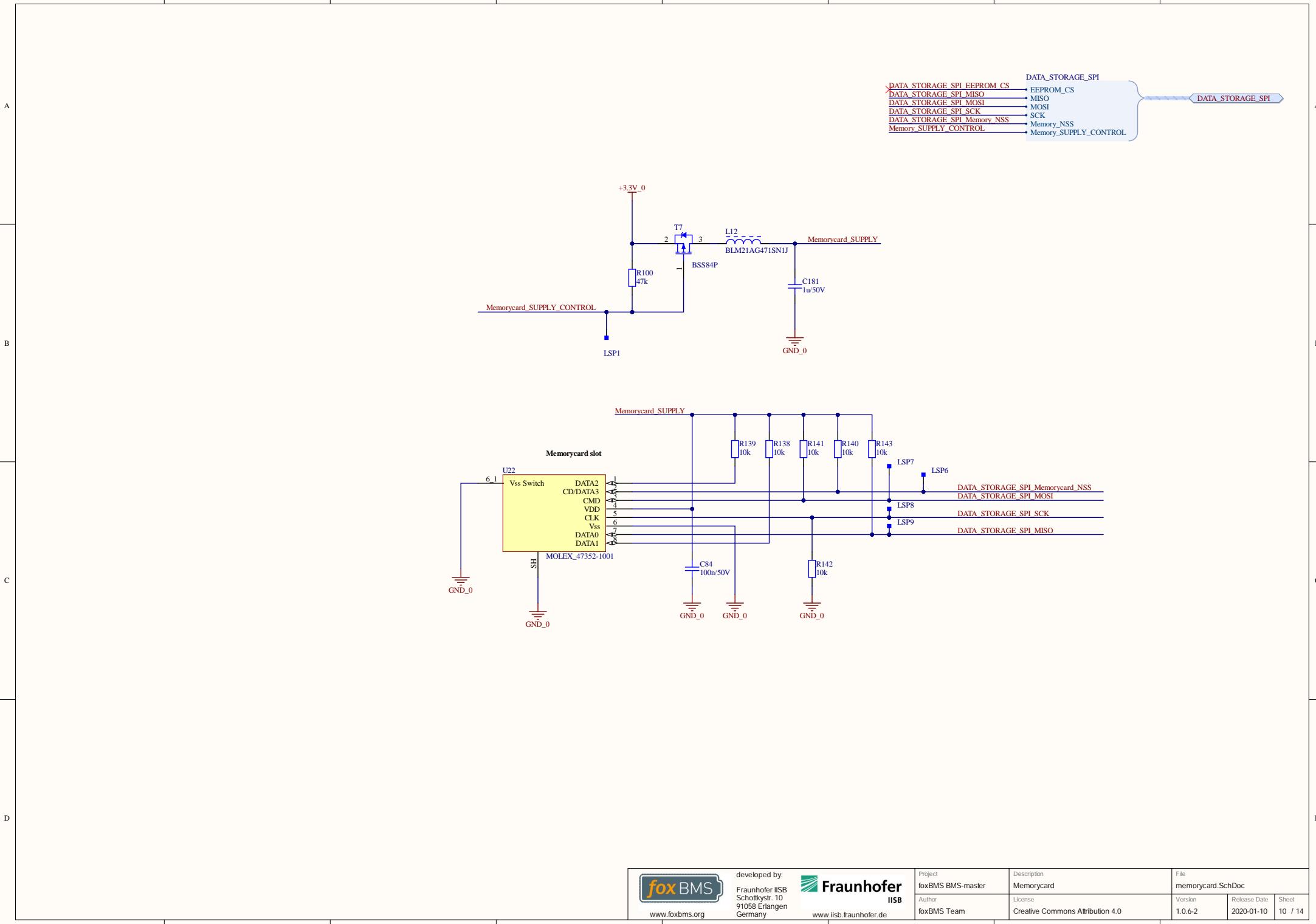
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Debug LED





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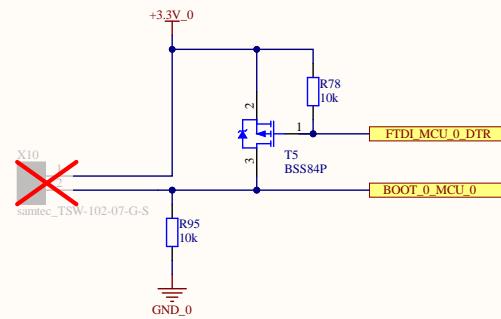
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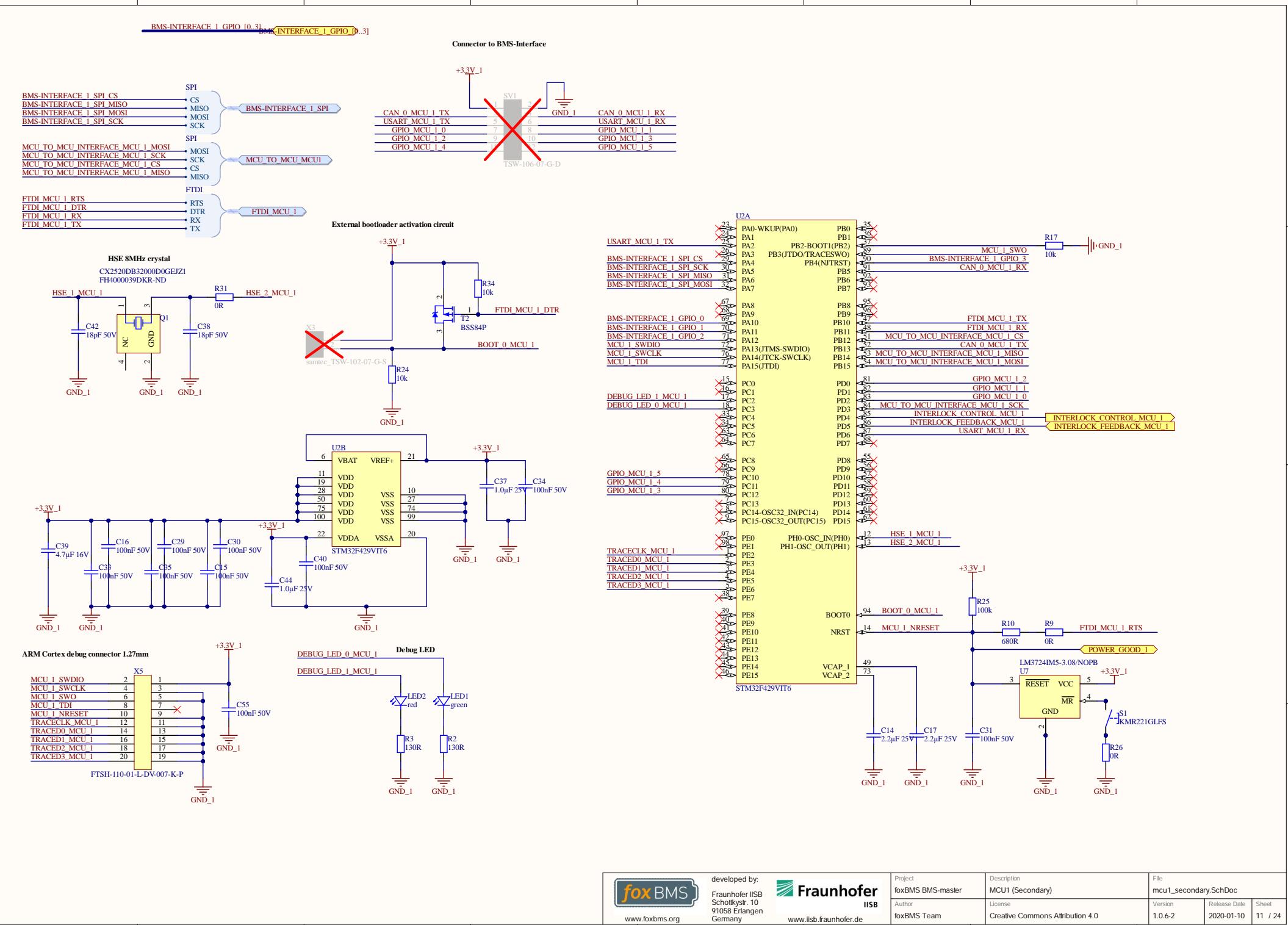
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External bootload activation circuit

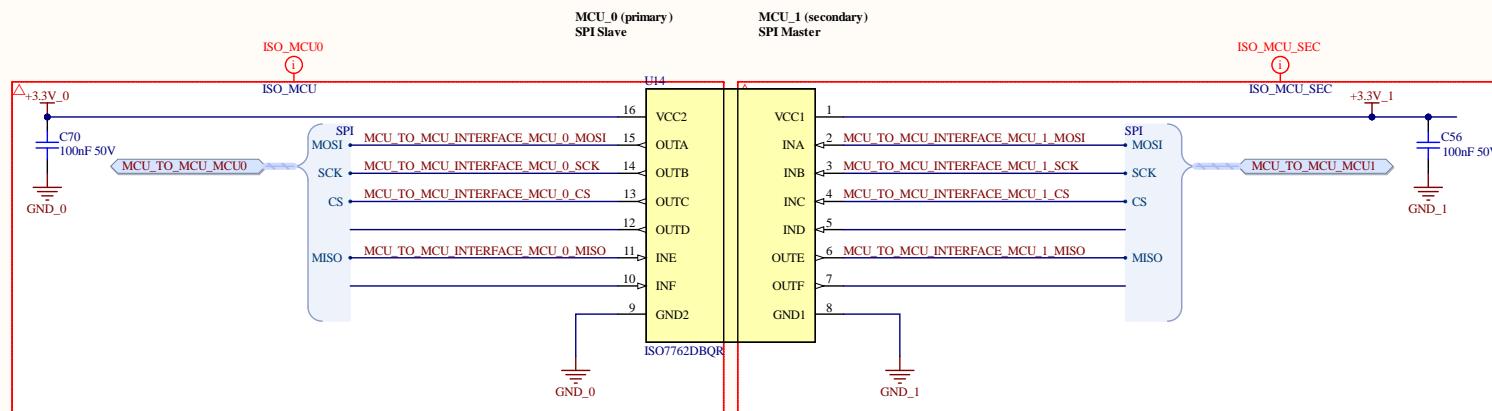




A

Isolated Bidirectional Interface
between MCU_0 (primary)
and MCU_1 (secondary)

SPI up to 45MHz



B

A

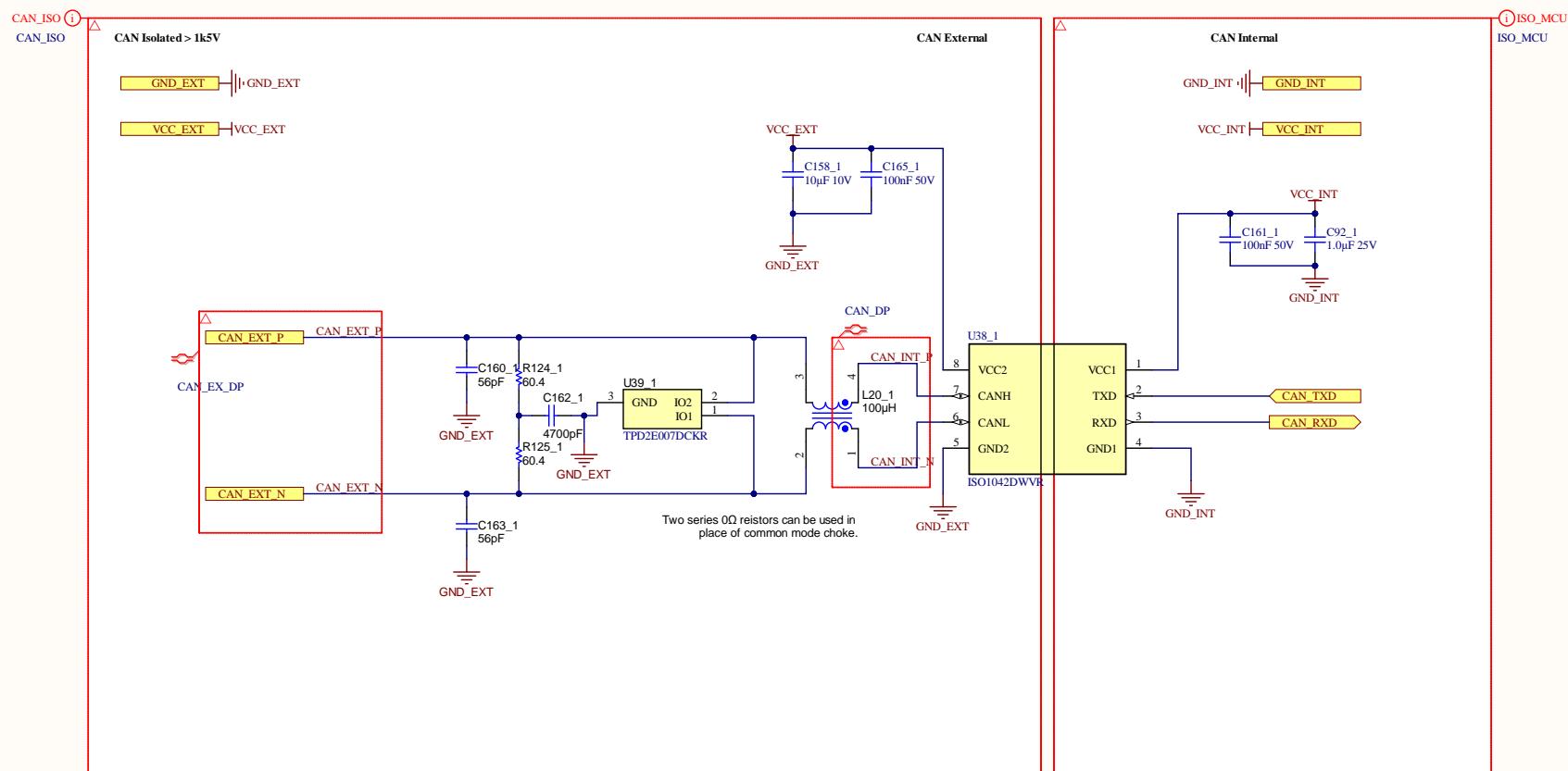
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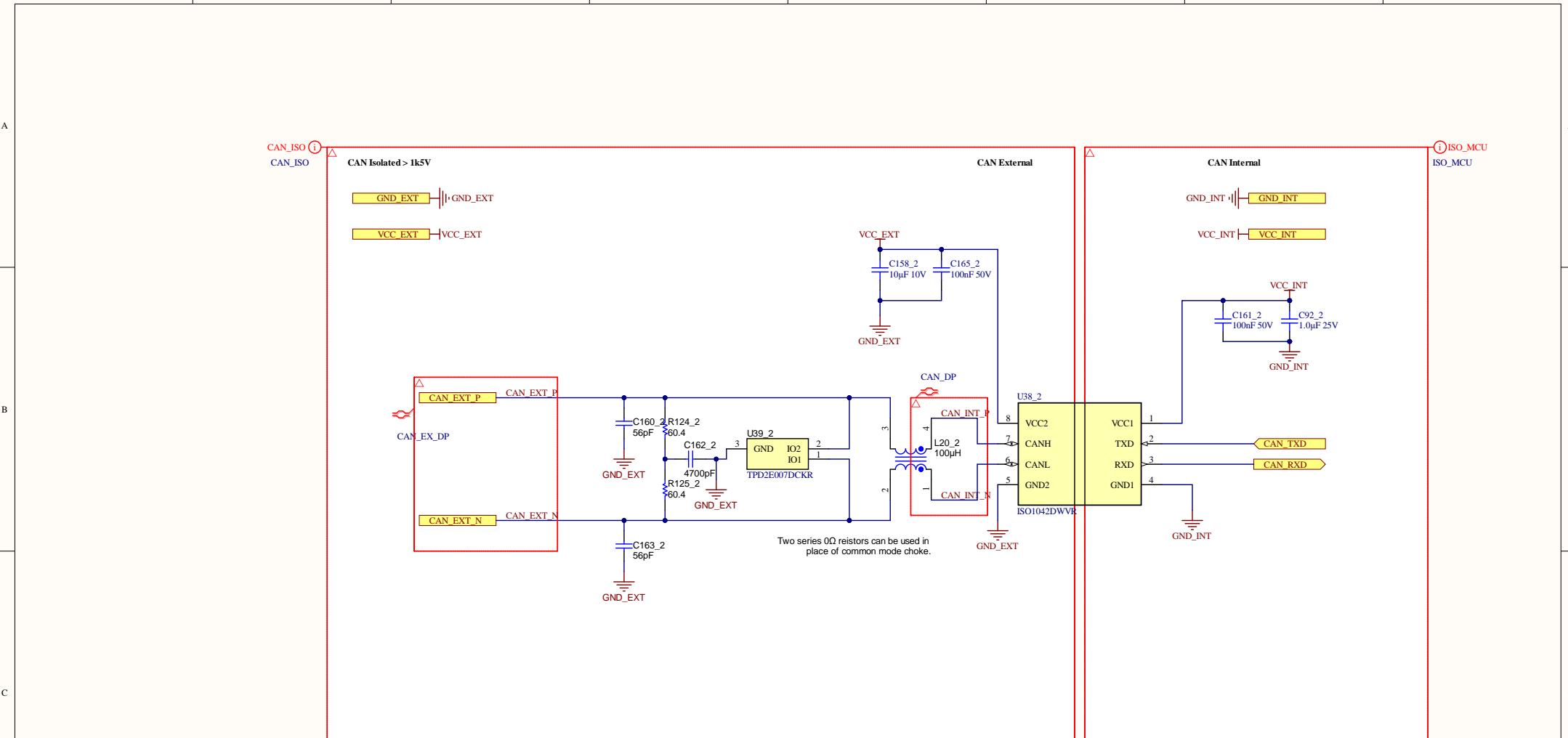
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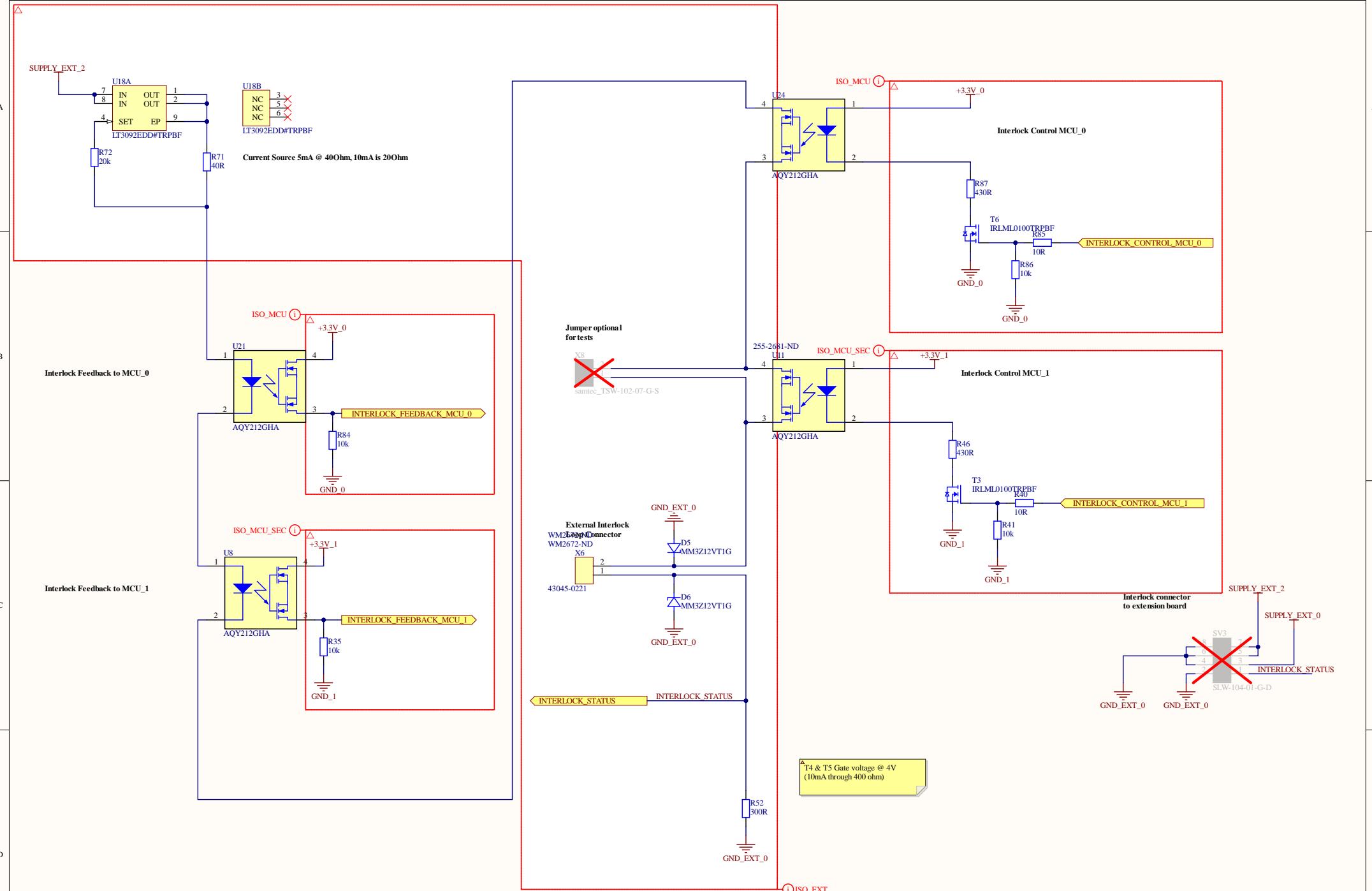
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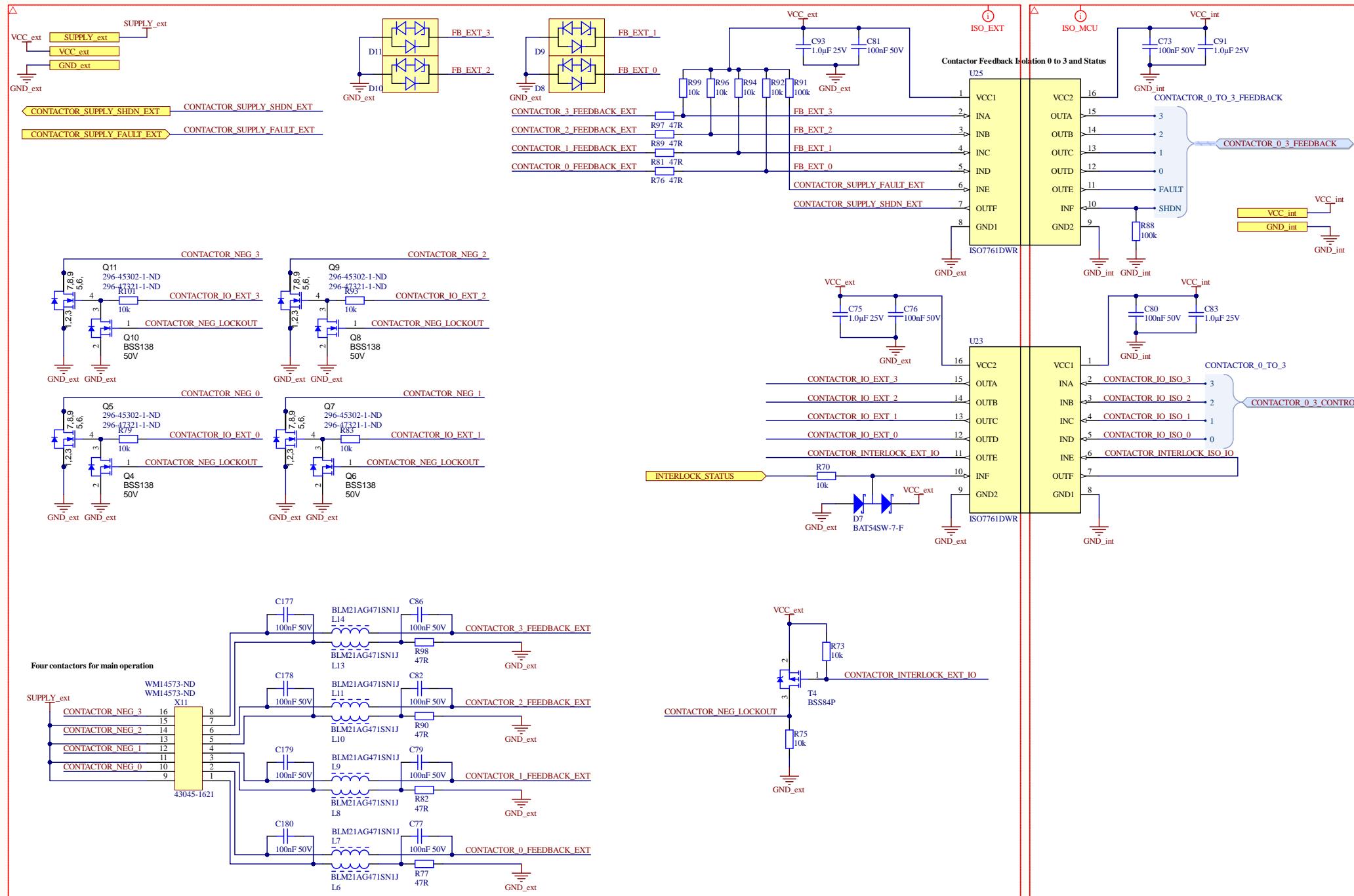
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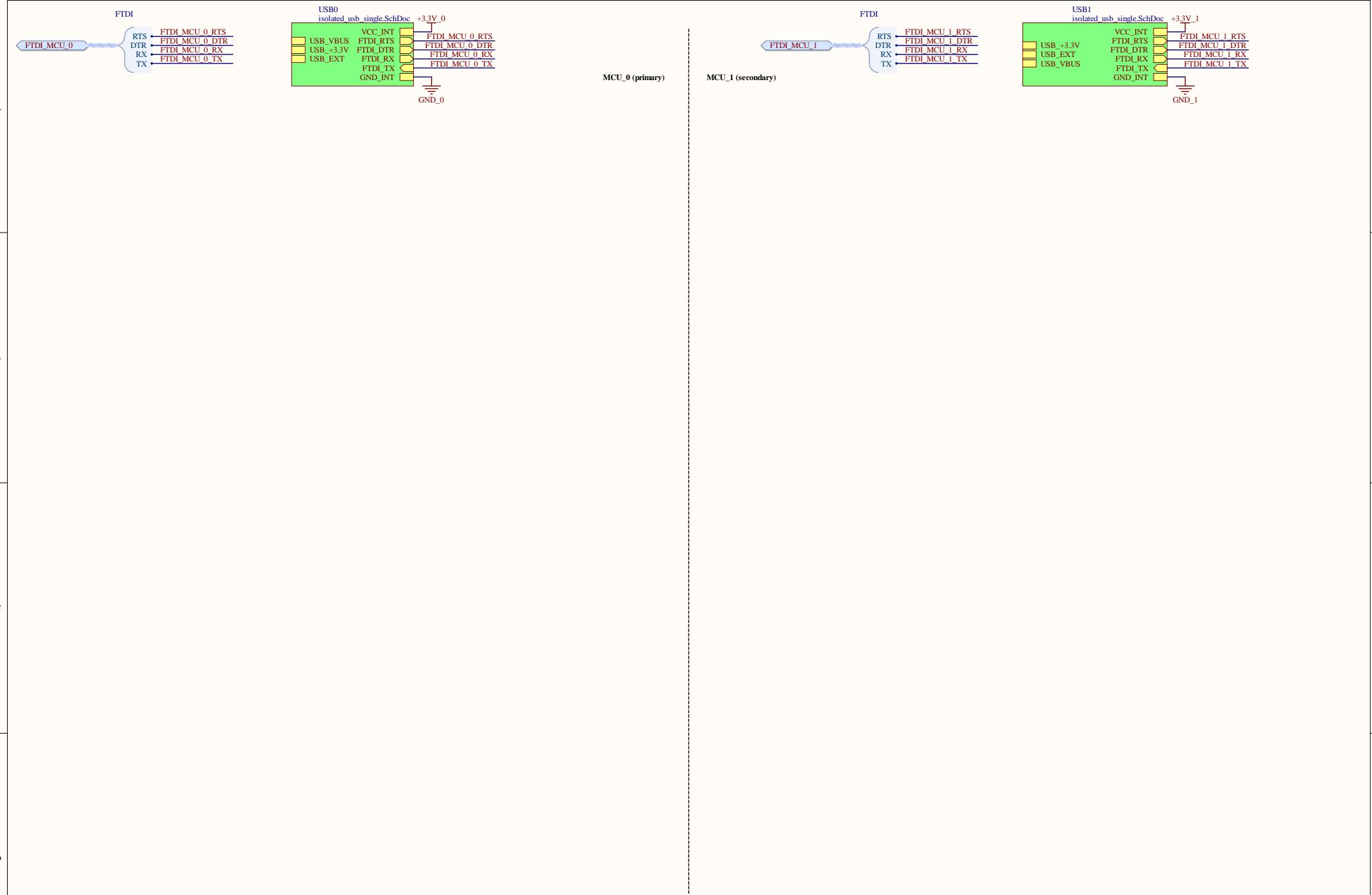
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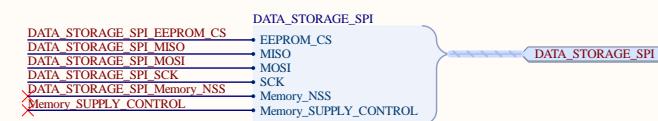






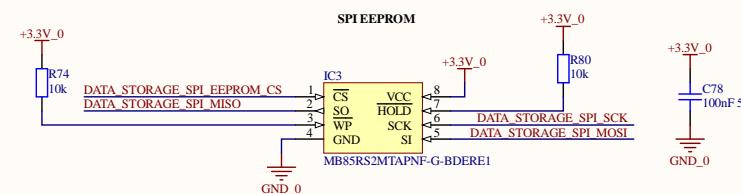


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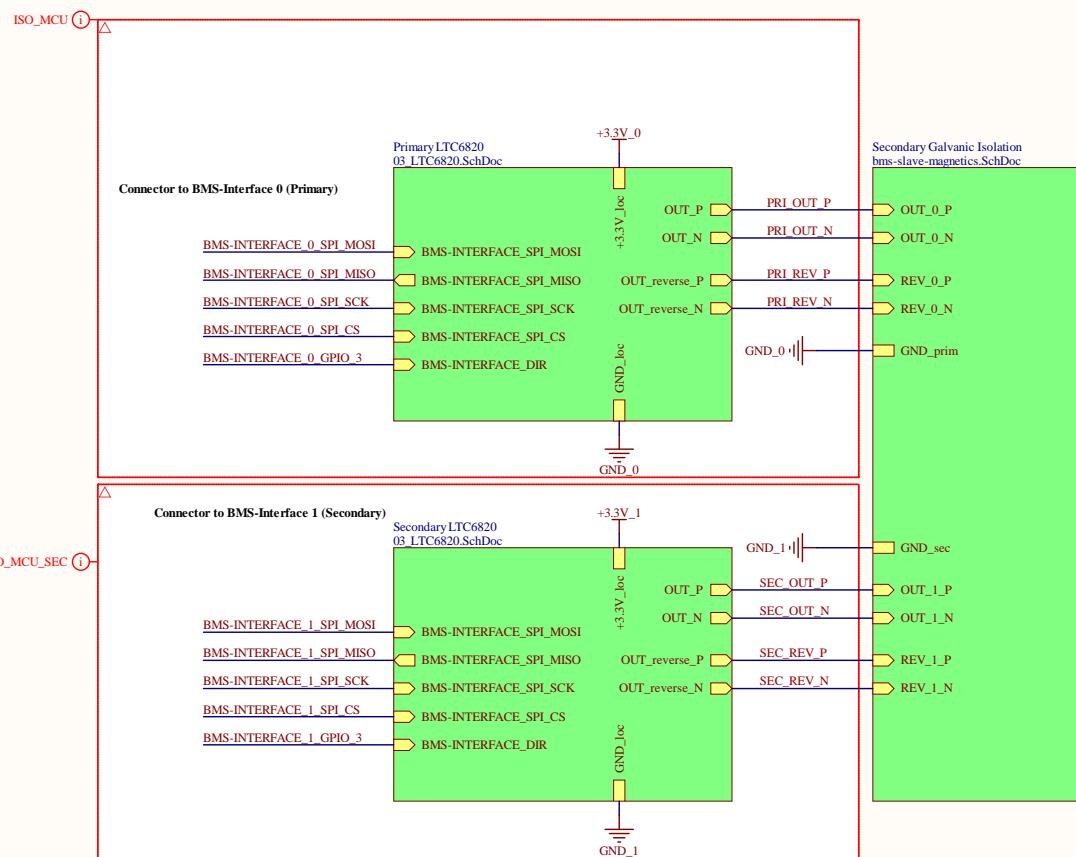
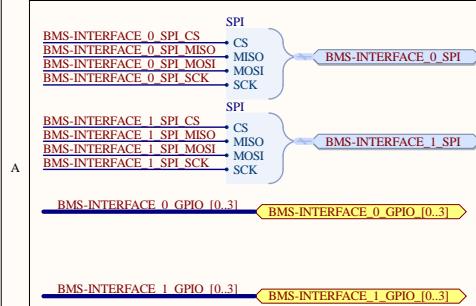
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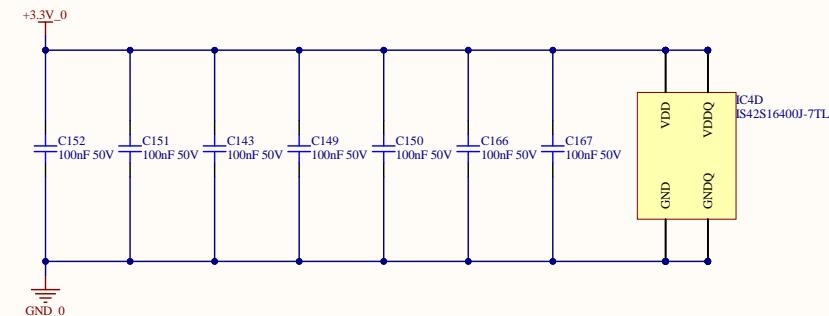
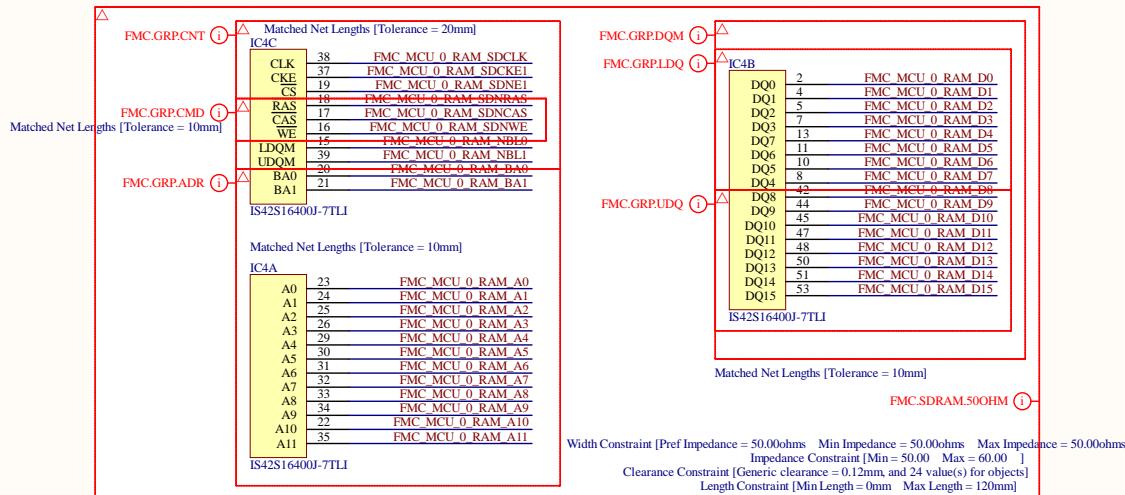
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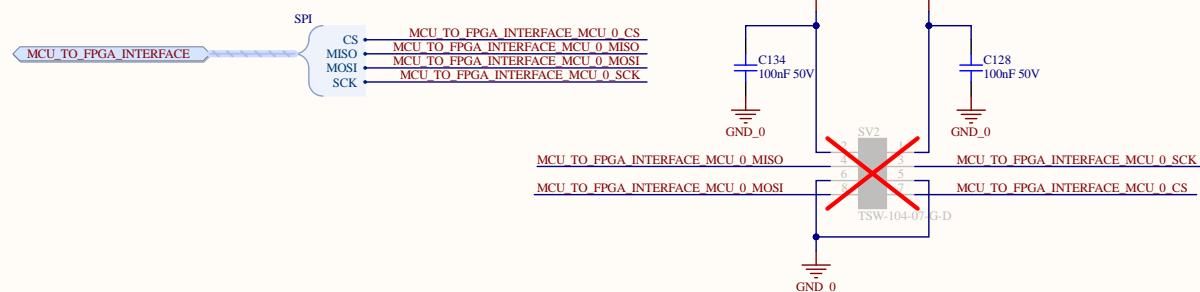
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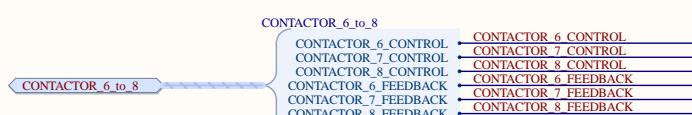
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Connector for optional FPGA extension board (SPI)

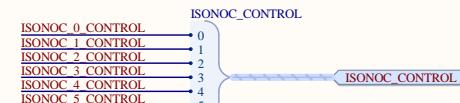


ADC MCU 0 CH [0..4] ADC MCU 0 CH [0..4]

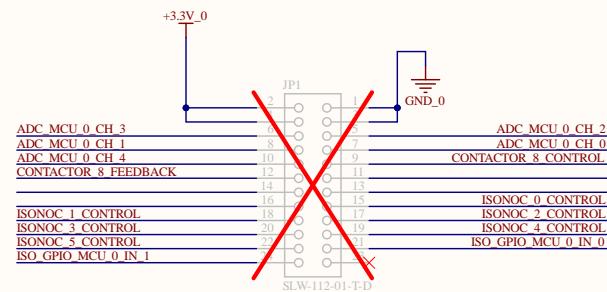
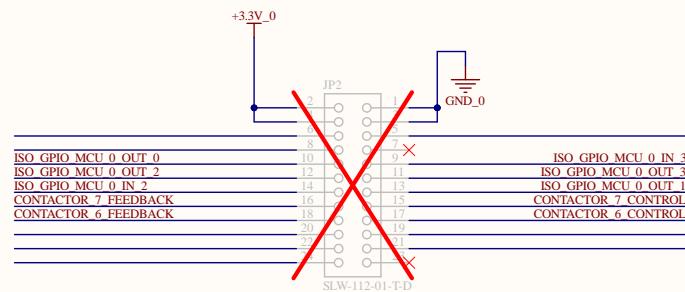
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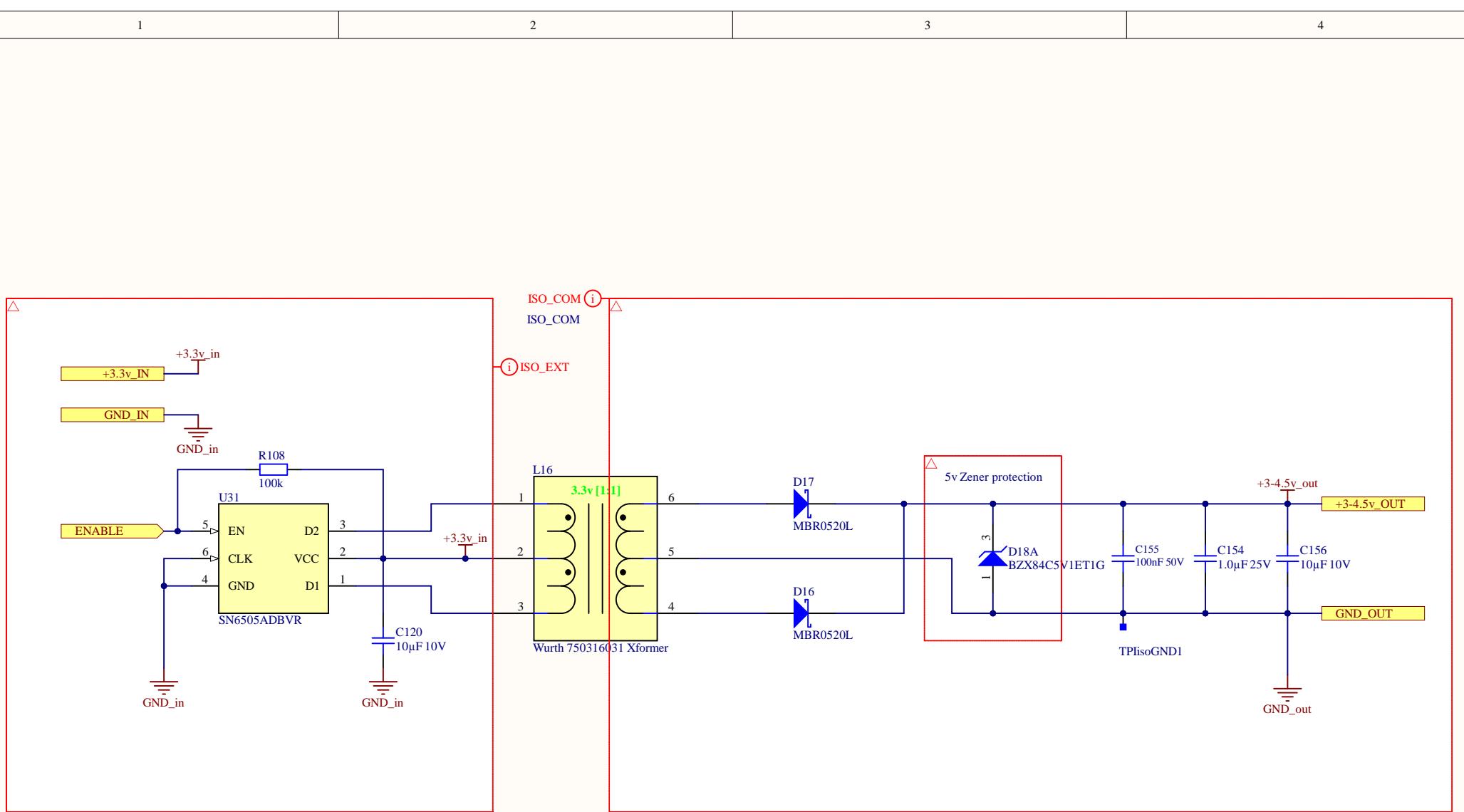
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