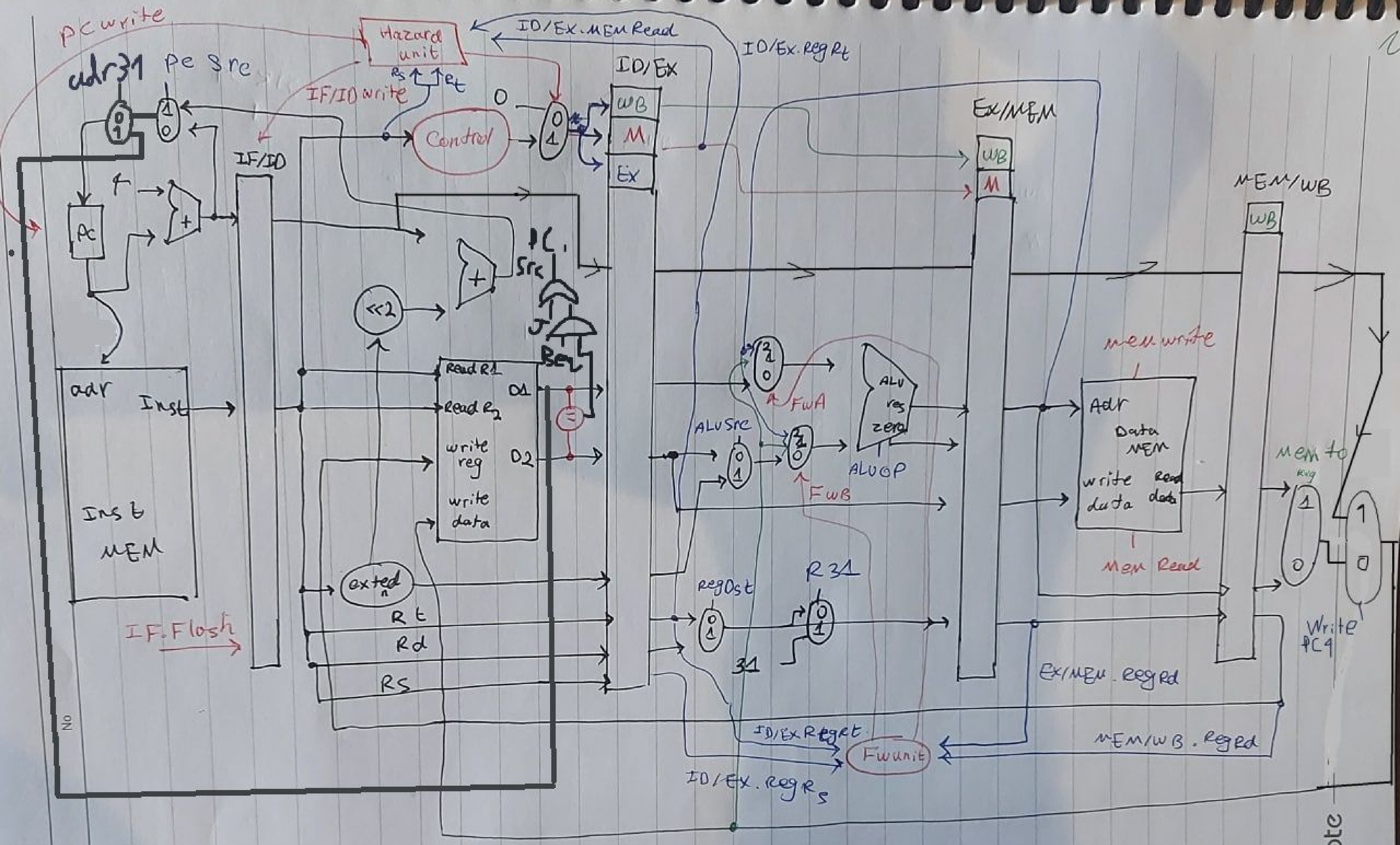

pc write
Hazard unit
Rs
Rt
ID/Ex.MEMRead
ID/Ex.RegRt
adr31
pc src
IF/ID write
Control
0
ID/Ex
WB
M
Ex
Ex/MEM
MEM/WB
IF/ID
4
pc
PC Src
J
Ben
<<2
Read R1
Read R2
write reg
write data
D1
D2
=
adr
Inst
Inst MEM
exted
Rt
Rd
RS
IF.Flosh
ALUSrc
FwA
FwB
ALU
res
zero
ALUOP
mem.write
Adr
Data MEM
write data
Read data
Mem Read
mem to reg
RegDst
R31
31
Write PC4
Ex/MEM.RegRd
MEM/WB.RegRd
ID/Ex.RegRt
Fwunit
ID/Ex.RegRs

Rt: add, sub, slt, and, or,
000000, 000001, 000010, 000011, 000100
opc = 000000

31 26	25 21	20 16	15 11	10 6	5 0
opc	rs	rt	rd	Shamt	func

Mem Reg: lw, sw
opc = 000001, 000010

31 26	25 21	20 16	15 0
opc	rs	rt	adr

Rti: addi, slti:
opc = 000011, 000100

31 26	25 21	20 16	15 0
opc	rs	rd	data bit

J, Jal:
opc = 000101, 000110

31 26	25 0
opc	adr

Jr:
opc = 000111

31 26	25 21	20 0
opc	R32	- - - - - -

don't care

beq
opc = 001000

31 26	25 21	20 16	15 0
opc	rs	rt	L

آرش شاهویی
۸۱۰۱۹۹۴۴۳
برنا ثانی
۸۱۰۱۹۹۴۳۶
معماری کامپیوتر
CA2

	RegDst	R31	Reg write	ALU Src	ALU OP	Mem Read	mem write	Mem to Reg	write PC+4	Branch	adr R31	Jump
RT	1	0	1	0	00	0	0	0	0	0	0	0
addi	0	0	1	1	01	0	0	0	0	0	0	0
sw	X	X	0	1	01	0	1	X	X	0	0	0
lw	0	0	1	1	01	1	0	1	0	0	0	0
J	X	X	0	X	X	0	0	X	X	X	X	1
Jal	X	1	1	X	X	0	0	X	1	X	X	1
Jr	X	X	0	X	X	0	0	X	X	X	1	0
beq	X	X	0	0	10	0	0	X	X	1	0	0
slti	0	0	1	1	11	0	0	1	0	0	0	0

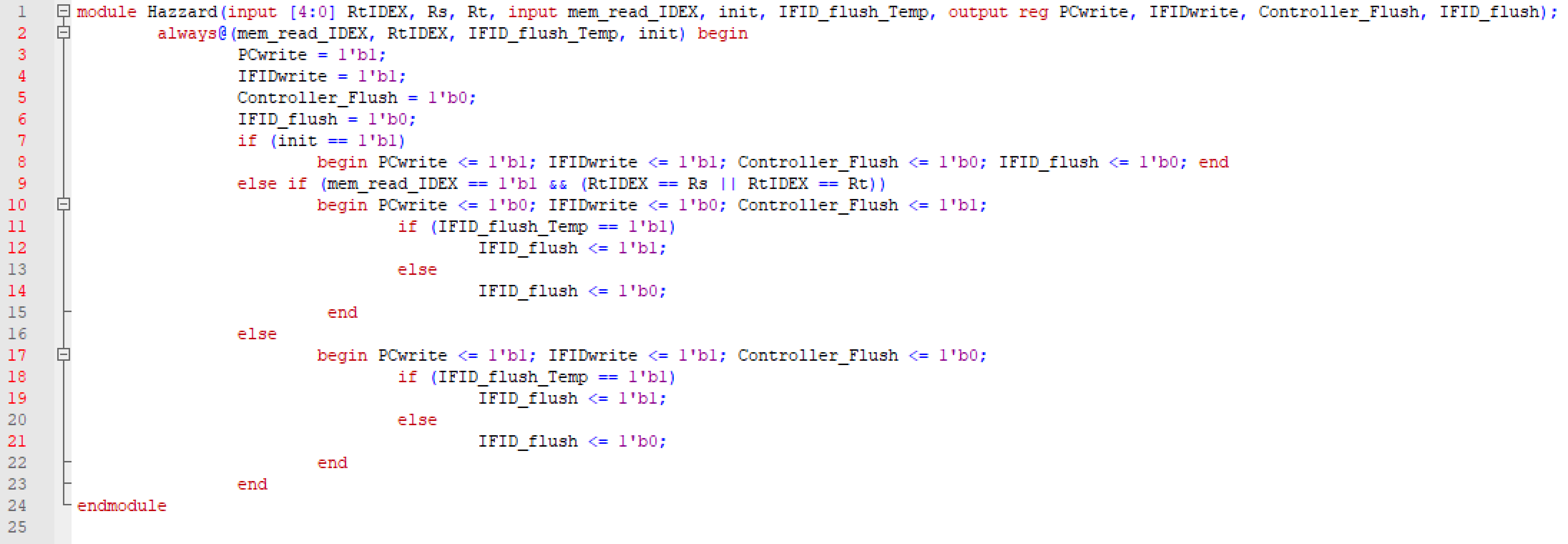
ALUop	ALU
00	RT
01	add
10	Sub
11	slt

```
if( (EX/MEM.Regwrite == 1) and
    (EX/MEM.Rd == ID/EX.Rs) and
    (EX/MEM.Rd != 0) )
        Forward A = 10;
```

بین دستور ۱ و ۲

```
if( (M/WB.Regwrite == 1) and
    (M/WB.Rd == ID/EX.Rs) and)
    (M/WB.Rd != 0) and !()
        Forward A = 01;
```

بین دستور ۱ و ۳

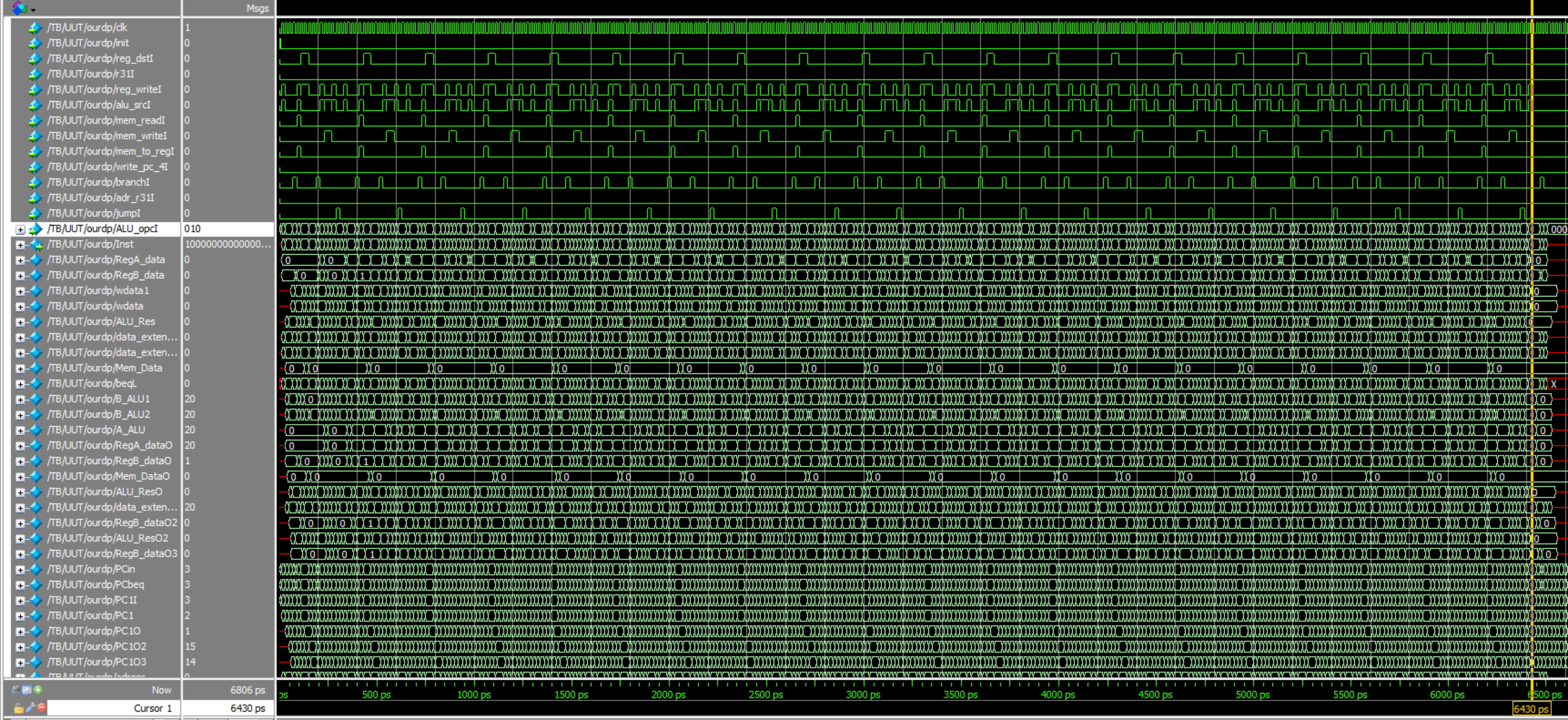


```verilog
module Hazzard(input [4:0] RtIDEX, Rs, Rt, input mem_read_IDEX, init, IFID_flush_Temp, output reg PCwrite, IFIDwrite, Controller_Flush, IFID_flush);
        always@(mem_read_IDEX, RtIDEX, IFID_flush_Temp, init) begin
                PCwrite = 1'b1;
                IFIDwrite = 1'b1;
                Controller_Flush = 1'b0;
                IFID_flush = 1'b0;
                if (init == 1'b1)
                        begin PCwrite <= 1'b1; IFIDwrite <= 1'b1; Controller_Flush <= 1'b0; IFID_flush <= 1'b0; end
                else if (mem_read_IDEX == 1'b1 && (RtIDEX == Rs || RtIDEX == Rt))
                        begin PCwrite <= 1'b0; IFIDwrite <= 1'b0; Controller_Flush <= 1'b1;
                                if (IFID_flush_Temp == 1'b1)
                                        IFID_flush <= 1'b1;
                                else
                                        IFID_flush <= 1'b0;
                         end
                else
                        begin PCwrite <= 1'b1; IFIDwrite <= 1'b1; Controller_Flush <= 1'b0;
                                if (IFID_flush_Temp == 1'b1)
                                        IFID_flush <= 1'b1;
                                else
                                        IFID_flush <= 1'b0;
                        end
                end
endmodule
```

```
R1 ← max = num[0]
R2 ← index = 0
for (i=0; i<r0; i++)
    R29
    if (max<num[i])
        max=num(i)
        index=i
```

[redacted]

```
Loop:  slt R10, R29, 20
       beq R10, R0, End_Loop
       lw R4, 1000(R29)
       slt R11, R1, R4
       beq R11, R0, Newi
       sw R4, 1000(R0)     } addi R1, R4, 0
       sw R29, 2004(R0)
Newi:  addi R29, R29, 1
       J Loop
End_Loop: ...
```



```
                              Msgs
/TB/UUT/ourdp/clk             1
/TB/UUT/ourdp/init            0
/TB/UUT/ourdp/reg_dstI        0
/TB/UUT/ourdp/r31I            0
/TB/UUT/ourdp/reg_writeI      0
/TB/UUT/ourdp/alu_srcI        0
/TB/UUT/ourdp/mem_readI       0
/TB/UUT/ourdp/mem_writeI      0
/TB/UUT/ourdp/mem_to_regI     0
/TB/UUT/ourdp/write_pc_4I     0
/TB/UUT/ourdp/branchI         0
/TB/UUT/ourdp/adr_r31I        0
/TB/UUT/ourdp/jumpI           0
/TB/UUT/ourdp/ALU_opcI        010
/TB/UUT/ourdp/Inst            10000000000000...
/TB/UUT/ourdp/RegA_data       0
/TB/UUT/ourdp/RegB_data       0
/TB/UUT/ourdp/wdata1          0
/TB/UUT/ourdp/wdata           0
/TB/UUT/ourdp/ALU_Res         0
/TB/UUT/ourdp/data_exten...   0
/TB/UUT/ourdp/data_exten...   0
/TB/UUT/ourdp/Mem_Data        0
/TB/UUT/ourdp/beqL            0
/TB/UUT/ourdp/B_ALU1          20
/TB/UUT/ourdp/B_ALU2          20
/TB/UUT/ourdp/A_ALU           20
/TB/UUT/ourdp/RegA_dataO      20
/TB/UUT/ourdp/RegB_dataO      1
/TB/UUT/ourdp/Mem_DataO       0
/TB/UUT/ourdp/ALU_ResO        0
/TB/UUT/ourdp/data_exten...   20
/TB/UUT/ourdp/RegB_dataO2     0
/TB/UUT/ourdp/ALU_ResO2       0
/TB/UUT/ourdp/RegB_dataO3     0
/TB/UUT/ourdp/PCin            3
/TB/UUT/ourdp/PCbeq           3
/TB/UUT/ourdp/PC1I            3
/TB/UUT/ourdp/PC1             2
/TB/UUT/ourdp/PC1O            1
/TB/UUT/ourdp/PC1O2           15
/TB/UUT/ourdp/PC1O3           14

Now        6806 ps
Cursor 1   6430 ps
```

1023	0	0	0	0	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4
1002	3	2	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
981	0	19	0	0	0	20	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
960	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
939	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
918	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
897	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
876	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
855	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
834	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
813	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
792	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
771	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
750	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
729	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
708	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
687	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
666	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
645	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
624	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
603	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
582	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
561	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
540	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
519	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
498	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
477	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
456	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
435	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
414	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
393	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
372	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
351	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
330	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
309	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
288	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
267	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
246	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
225	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
204	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
183	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
162	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
141	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
120	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
99	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
78	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
57	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
36	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0					
-6																					