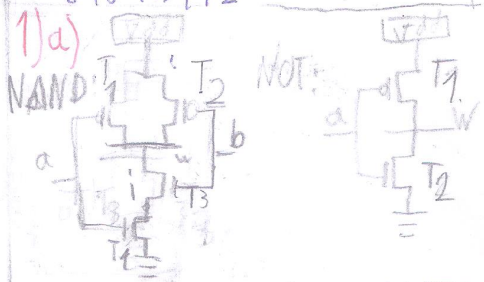
Arash Shahin
810199492

Digital Logic Design
CA1

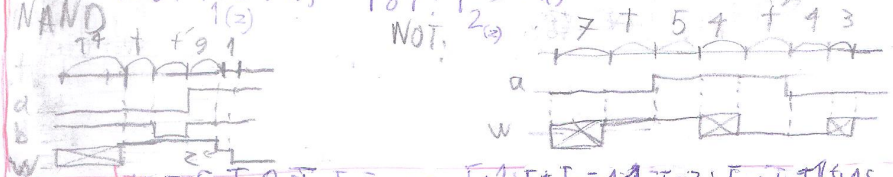
1400/7/
ECE 367

1) a)

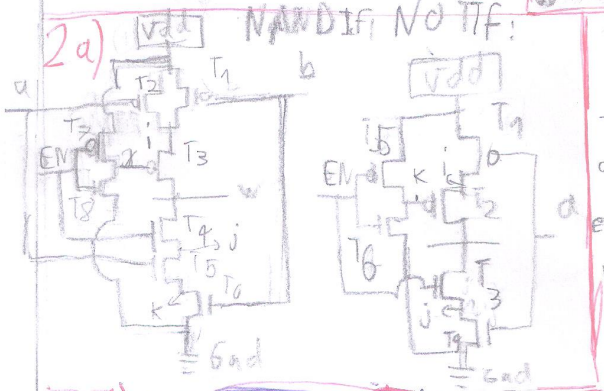


b) NAND: $T_{0,0} = T_{1(z)} + T_{4(z)} = 10ns$ $T_{0,1} = T_{3(z)} + T_{4(z)} = 14ns$

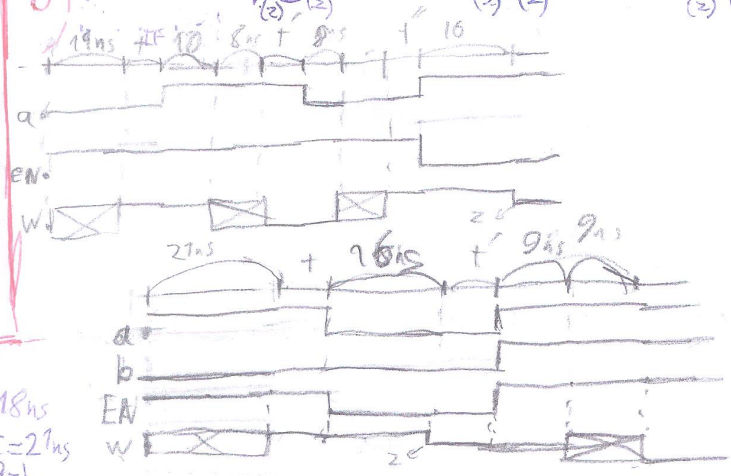
NOT: $T_{0,0} = T_{1(z)} = 9ns$ $T_{0,1} = T_{2(z)} = 7ns$



2 a)



b) NOTIF: $T_{0,0} = T_{2(z)} + T_{4(z)} = 18ns$ $T_{0,1} = T_{3(z)} + T_{4(z)} = 14ns$ $T_{0,2} = T_{5(z)} + T_{6(z)} = 16ns$



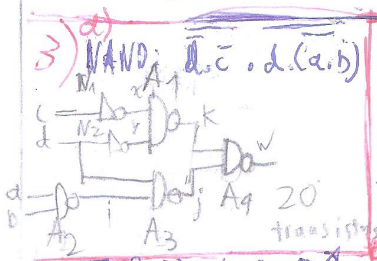
3) a) NAND: $\bar{d}.\bar{c} \cdot \bar{d}.(a.b)$

NANDIF:

$T_{0,0} = T_{1(z)} + T_{2(z)} = 18ns$

$T_{0,1} = T_{4(z)} + T_{5(z)} + T_{6(z)} = 21ns$

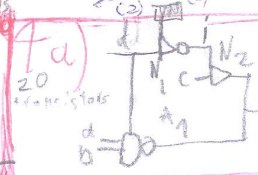
$T_{0,2} = T_{3(z)} = 16ns$



b) $T_{0,0} = A_{2(c)} + A_{3(c)} + A_{4(c)} = 34ns$

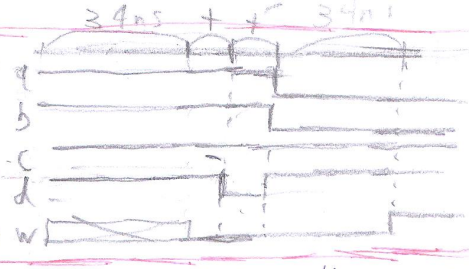
$T_{0,1} = A_{2(c)} + A_{3(c)} + A_{4(c)} = 38ns$

4 a) 20 transistors



b) $T_{0,0} = N_{1(1)} + N_{2(2)} = 39ns$

$T_{0,1} = N_{1(1)} + N_{2(2)} = 34ns$



Part 1,2,5 e: There are no differences

Part 3,4 e: The system verilog has shorter delays than our handcalculations or just using primitive version of our gates. This is because when we do hand calculations or primitive gates, we always use the worst case delays for each gate. While in reality if we also include their switch levels as well, that is not the case and so we will have shorter delays.

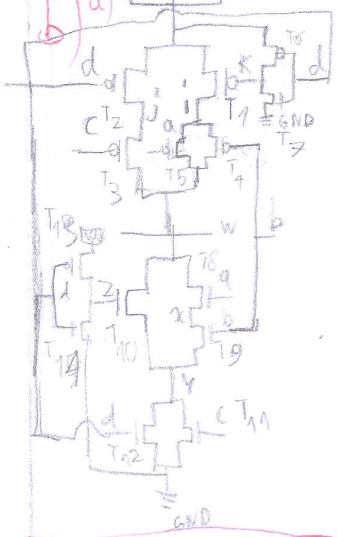
6) c) timing: part3: $T_{0,1}=38$ $T_{0,0}=34$ / part4: $T_{0,1}=39$ $T_{0,0}=34$ / part5: $T_{0,1}=21$ $T_{0,0}=18$

transistors: part3 = part4 = 20 / part5 = 14

Power consumption: part3 > part4 > part5

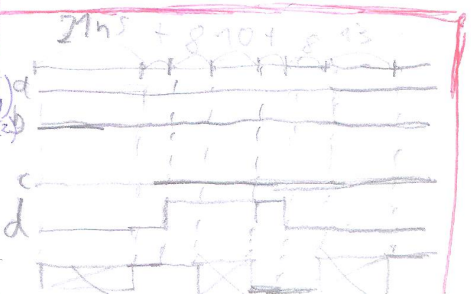
as the number of transistors and delays increases so does our power consumption

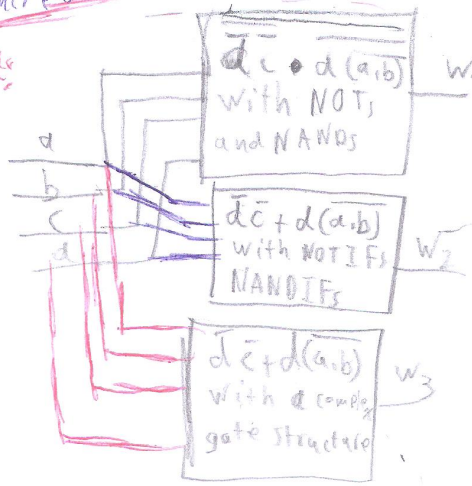
5) a)



b) $T_{0,1}$: 21ns $(T_{11(c)} + T_{8(c)} + T_{9(c)})$

$T_{0,0}$: $T_{2(c)} + T_{3(c)} = 18ns$





```
`timescale 1ns/1ns
module mynot (input a, output w);
        supply1 Vdd;
        supply0 Gnd;
        pmos #(4,7,9) T1(w,Vdd,a);
        nmos #(3,5,7) T2(w,Gnd,a);

endmodule
```

```
`timescale 1ns/1ns
module mynand (input a,b, output w);
        wire i;
        supply1 Vdd;
        supply0 Gnd;
        pmos #(4,7,9) T1(w,Vdd,a);
        pmos #(4,7,9) T2(w,Vdd,b);
        nmos #(3,5,7) T3(w,i,b);
        nmos #(3,5,7) T4(i,Gnd,a);

endmodule
```

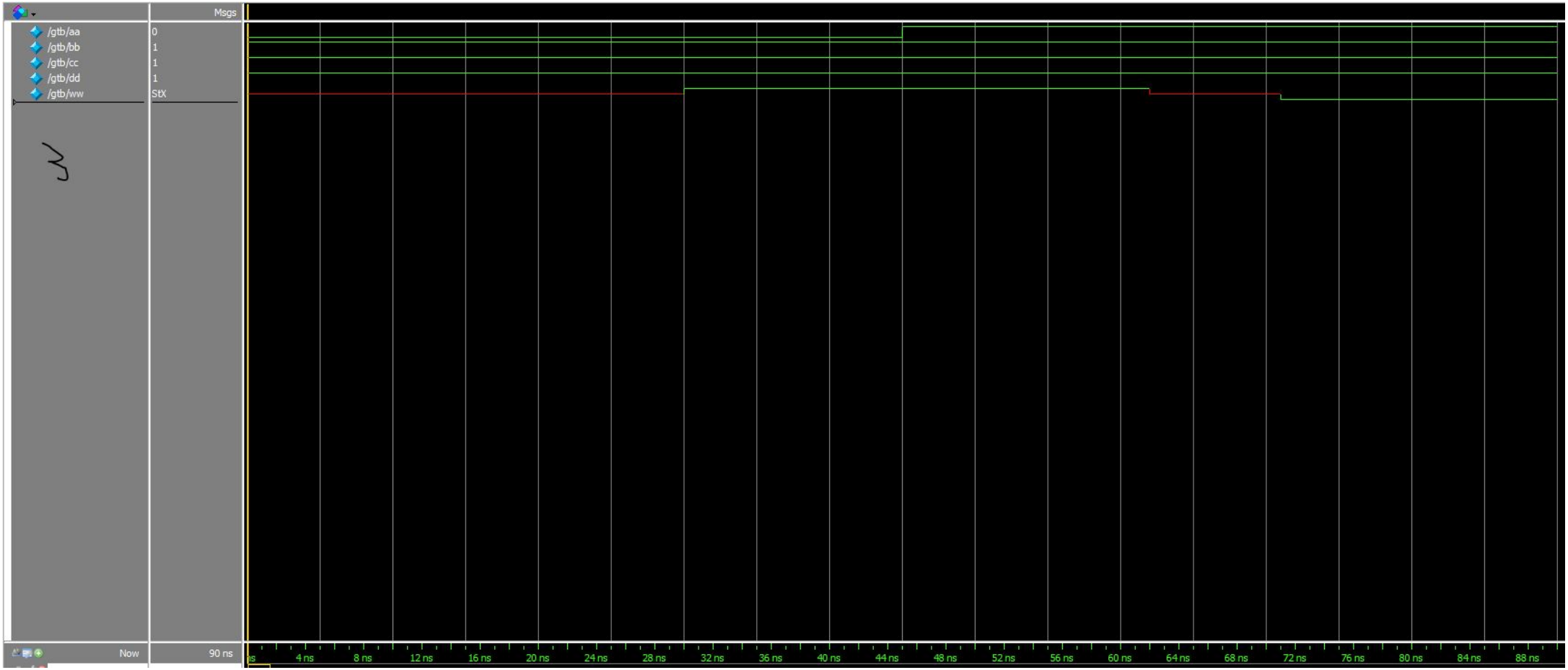
1.2

```
`timescale 1ns/1ns
module mynotif (input a,EN, output w);
        wire i,j,k;
        supply1 Vdd;
        supply0 Gnd;
        pmos #(4,7,9) T1(i,Vdd,a);
        pmos #(4,7,9) T2(w,i,k);
        nmos #(3,5,7) T3(w,j,EN);
        nmos #(3,5,7) T4(j,Gnd,a);
        pmos #(4,7,9) T5(k,Vdd,EN);
        nmos #(3,5,7) T6(k,Gnd,EN);

endmodule
```

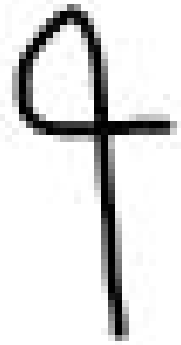
```
`timescale 1ns/1ns
module mynandif (input a,b,EN, output w);
        wire i,j,k,x;
        supply1 Vdd;
        supply0 Gnd;
        pmos #(4,7,9) T1(i,Vdd,b);
        pmos #(4,7,9) T2(i,Vdd,a);
        pmos #(4,7,9) T3(w,i,x);
        nmos #(3,5,7) T4(w,j,EN);
        nmos #(3,5,7) T5(j,k,a);
        nmos #(3,5,7) T6(k,Gnd,b);
        pmos #(4,7,9) T7(x,Vdd,EN);
        nmos #(3,5,7) T8(x,Gnd,EN);

endmodule
```

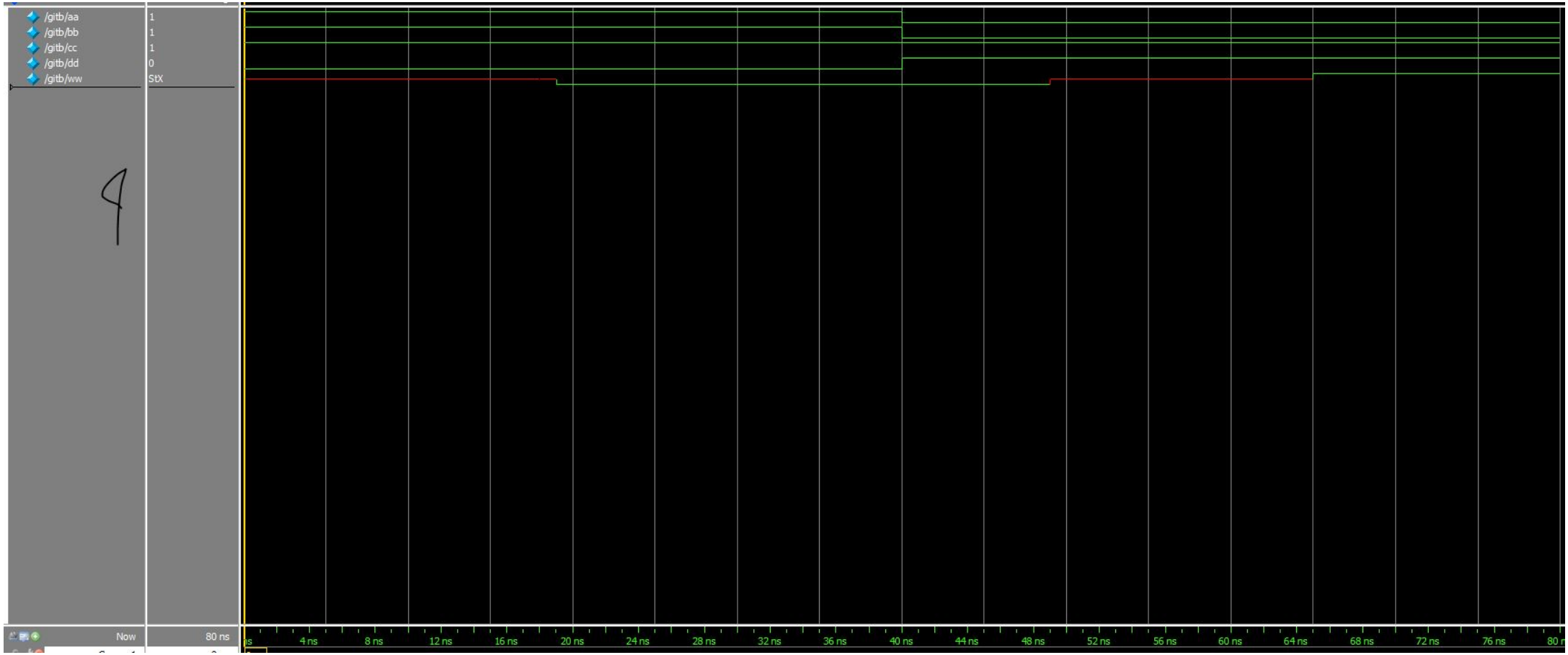
22

```
`timescale 1ns/1ns
module gates (input a,b,c,d, output w);
        wire i,j,k,x,y;
        mynot N1(c,x);
        mynot N2(d,y);
        mynand A1(x,y,k);
        mynand A2(a,b,i);
        mynand A3(d,i,j);
        mynand A4(k,j,w);

endmodule
```


Msgs
/gtb/aa
/gtb/bb
/gtb/cc
/gtb/dd
/gtb/ww
0
1
1
1
StX
Now
90 ns
4 ns
8 ns
12 ns
16 ns
20 ns
24 ns
28 ns
32 ns
36 ns
40 ns
44 ns
48 ns
52 ns
56 ns
60 ns
64 ns
68 ns
72 ns
76 ns
80 ns
84 ns
88 ns

```
`timescale 1ns/1ns
module gatesif (input a,b,c,d, output w);
        wire i;
        supply1 Vdd;
        mynotif N1(d,Vdd,i);
        mynotif N2(c,i,w);
        mynandif A1(a,b,d,w);

endmodule
```

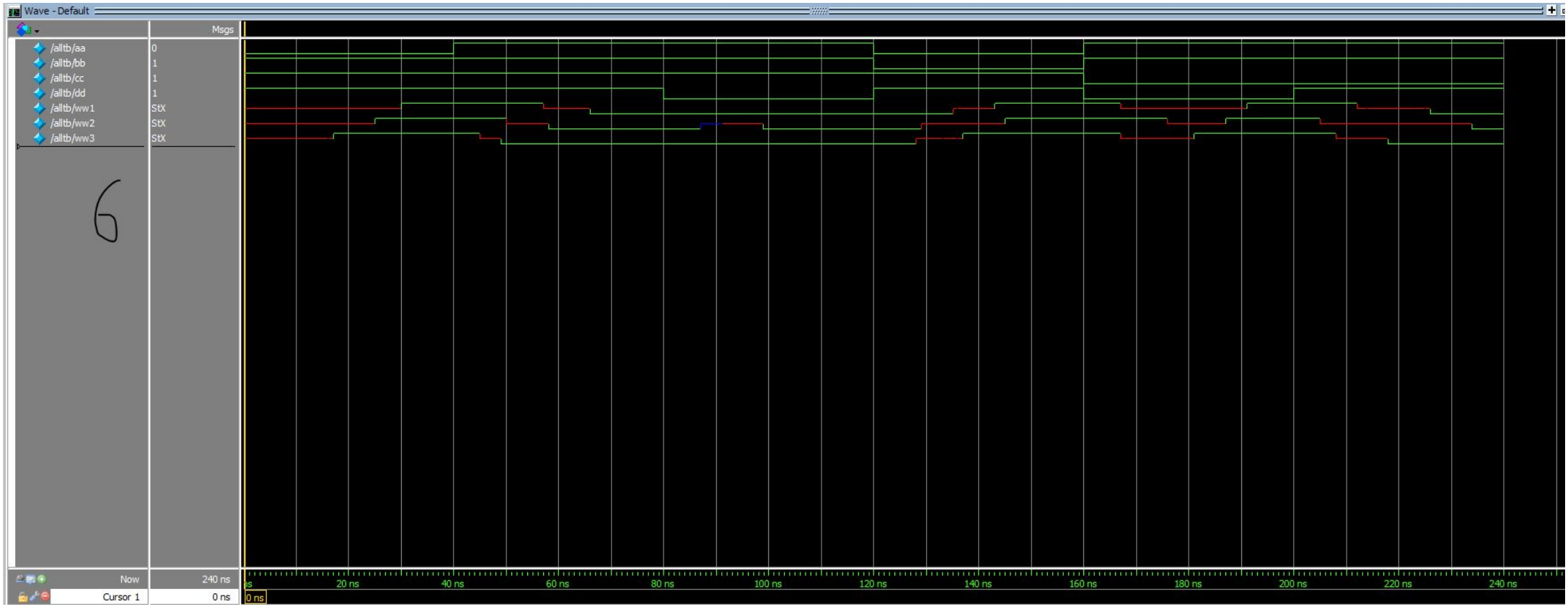



/gitb/aa
/gitb/bb
/gitb/cc
/gitb/dd
/gitb/ww
1
1
1
0
StX
9
Now
80 ns
4 ns
8 ns
12 ns
16 ns
20 ns
24 ns
28 ns
32 ns
36 ns
40 ns
44 ns
48 ns
52 ns
56 ns
60 ns
64 ns
68 ns
72 ns
76 ns

```
`timescale 1ns/1ns
module mycmoss (input a,b,c,d, output w);
        wire i,j,k,x,y,z;
        supply1 Vdd;
        supply0 Gnd;
        pmos #(4,7,9) T1(i,Vdd,k);
        pmos #(4,7,9) T2(j,Vdd,d);
        pmos #(4,7,9) T3(w,j,c);
        pmos #(4,7,9) T4(w,i,b);
        pmos #(4,7,9) T5(w,i,a);
        pmos #(4,7,9) T6(k,Vdd,d);
        nmos #(3,5,7) T7(k,Gnd,d);
        nmos #(3,5,7) T8(w,x,a);
        nmos #(3,5,7) T9(x,y,b);
        nmos #(3,5,7) T10(w,y,z);
        nmos #(3,5,7) T11(y,Gnd,c);
        nmos #(3,5,7) T12(y,Gnd,d);
        pmos #(4,7,9) T13(z,Vdd,d);
        nmos #(3,5,7) T14(z,Gnd,d);

endmodule
```

5

```
`timescale 1ns/1ns
module alltb ();
        logic aa=0,bb=1,cc=1,dd=1;
        wire ww1,ww2,ww3;
        gates AGT(.a(aa),.b(bb),.c(cc),.d(dd),.w(ww1));
        gatesif AGIT(.a(aa),.b(bb),.c(cc),.d(dd),.w(ww2));
        mycmoss MCT(.a(aa),.b(bb),.c(cc),.d(dd),.w(ww3));
        initial begin
        #40 aa=1;
        #40 dd=0;
        #40 aa=0;bb=0;dd=1;
        #40 aa=1;bb=1;cc=0;dd=0;
        #40 dd=1;
        #40 $stop;
        end
endmodule
```


Wave - Default
Msgs
/alltb/aa
/alltb/bb
/alltb/cc
/alltb/dd
/alltb/ww1
/alltb/ww2
/alltb/ww3
0
1
1
1
StX
StX
StX
6
Now
240 ns
Cursor 1
0 ns
20 ns
40 ns
60 ns
80 ns
100 ns
120 ns
140 ns
160 ns
180 ns
200 ns
220 ns
240 ns
0 ns