



LAN9512/LAN9513/LAN9514 Layout Guidelines

1 Introduction

The LAN9512/LAN9513/LAN9514 is a high performance Hi-Speed USB 2.0 hub with a 10/100 Ethernet Controller. With applications ranging from embedded systems, desktop PCs, notebook PCs, printers, game consoles, and docking stations, the LAN9512/LAN9513/LAN9514 is targeted as a high performance, low cost USB/Ethernet and USB/USB connectivity solution.

The LAN9512/LAN9513/LAN9514 contains an integrated USB 2.0 hub, USB 2.0 PHYs, a 10/100 Ethernet PHY, a 10/100 Ethernet controller, a TAP controller, a EEPROM controller, and a FIFO controller. The internal USB 2.0 hub and USB PHYs are compliant with the USB 2.0 High-Speed standard.

The Ethernet controller supports auto-negotiation, auto-polarity correction, HP Auto-MDIX, and is compliant with the IEEE 802.3 and IEEE 802.3u standards. An external MII interface provides support for an external Fast Ethernet PHY, HomePNA, and HomePlug functionality.

Multiple power management features are provided, including various low power modes and "Magic Packet", "Wake On LAN", and "Link Status Change" wake events. These wake events can be programmed to initiate a USB remote wakeup.

An internal EEPROM controller exists to load various USB configuration information and the device MAC address. The integrated IEEE 1149.1 compliant TAP controller provides boundary scan via JTAG.

This layout guide provides important information about the PCB layout requirements for the LAN9512/LAN9513/LAN9514.

1.1 References

LAN9512 Data Brief

LAN9512 Datasheet

LAN9512 Reference Design

LAN9513 Data Brief

LAN9513 Datasheet

LAN9513 Reference Design

LAN9514 Data Brief

LAN9514 Datasheet

LAN9514 Reference Design

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2 General PCB Layout Guidelines

2.1 Power Supply Considerations

1. Ensure adequate power supply ratings. Verify that all power supplies and voltage regulators can supply the amount of current required.
2. Power supply output ripple should be limited to less than 50 mV.
3. Noise levels on all power planes and ground planes should be limited to less than 50 mV.
4. Ferrite beads should be rated for 4 – 6 times the amount of current they are expected to supply. Any de-rating over temperature should also be accounted for.

2.2 PCB Decoupling

1. Every high-speed semiconductor device on the PCB assembly requires decoupling capacitors. One decoupling cap for every power pin is necessary.
2. Decoupling capacitor value is application dependent. Typical decoupling capacitor values may range from 0.1 μF to 0.001 μF .
3. The total decoupling capacitance should be greater than the load capacitance presented to the digital output buffers.
4. Typically, Class II dielectric capacitors are chosen for decoupling purposes. The first choice would be an X7R dielectric ceramic capacitor for its excellent stability and good package size vs. capacitance characteristics. The designer's second choice might be the X5R dielectric for its excellent stability but it may be somewhat limiting in the package size vs. capacitance characteristics. For a third choice, one might look to the Y5V dielectric, but this Class III dielectric is less stable and the package size vs. capacitance characteristics may be a problem for most applications. Low inductance is of the utmost importance when considering decoupling capacitor characteristics.
5. Each decoupling capacitor should be located as close as possible to the power pin that it is decoupling.
6. All decoupling capacitor leads should be as short as possible. The best solutions are plane connection vias inside the surface mount pads. When using vias outside the surface mount pads, pad-to-via connections should be less than 5 – 10 mils in length. Trace connections should be as wide as possible to lower inductance.

Figure 2.1 illustrates PCB decoupling techniques.

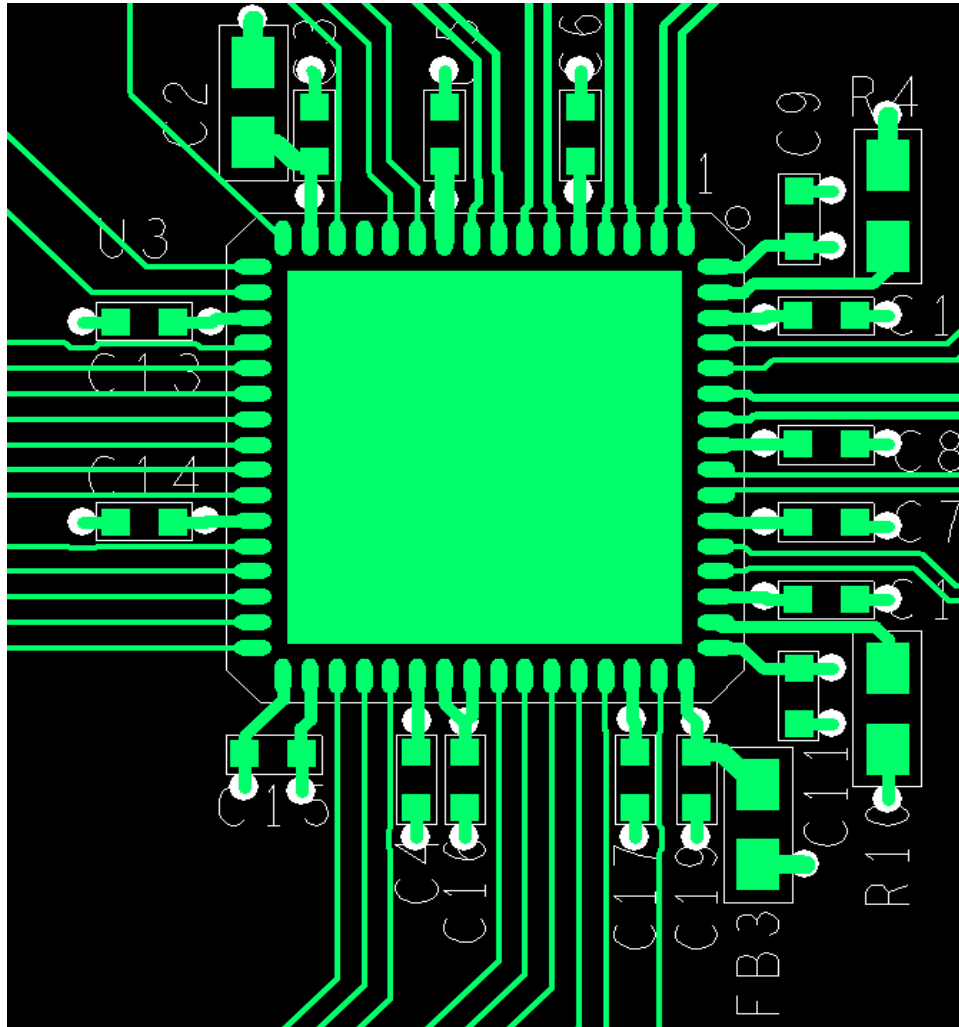


Figure 2.1 PCB Decoupling

2.3 PCB Bypassing

1. Bypass capacitors should be placed near all power entry points on the PCB. These caps will allow unwanted high-frequency noise from entering the design; the noise will simply be shunted to ground.
2. Bypass capacitors should be utilized on all power supply connections and all voltage regulators in the design.
3. Bypass capacitor values are application dependent and will be dictated by the frequencies present in the power supplies.
4. All bypass capacitor leads should be as short as possible. The best solutions are plane connection vias inside the surface mount pads. When using vias outside the surface mount pads, pad-to-via connections should be less than 5 – 10 mils in length. Trace connections should be as wide as possible to lower inductance.

2.4 PCB Bulk Capacitors

1. Bulk capacitors must be properly utilized in order to minimize switching noise. Bulk capacitance helps maintain constant DC voltage and current levels.
2. Bulk capacitors should be utilized on all power planes and all voltage regulators in the design.
3. All bulk capacitor leads should be as short as possible. The best solutions are plane connection vias inside the surface mount pads. When using vias outside the surface mount pads, pad-to-via connections should be less than 5 – 10 mils in length. Trace connections should be as wide as possible to lower inductance.
4. In the case where a ferrite bead is used on the USB connector to filter the VCC, the use of bulk capacitance on the USB connector side is not recommended. This is an attempt to limit the in-rush current of the USB circuitry. SMSC does recommend the use of a 4.7 uF bulk capacitor on the in-board side of the ferrite bead. Refer to the latest LAN9512/LAN9513/LAN9514 reference schematic for details.

2.5 Crystal Circuitry

1. Locate all crystal circuit components on the top layer. This will reference all these components and their traces to the same digital ground plane reference.
2. Isolate all the crystal components and traces from other signals as best as possible.
3. Verify that the crystal circuit operates within specification (+/-50 PPM) over the entire operating range of the application. This includes temperature, time and application tolerance.

2.6 PCB Layer Strategy

1. SMSC strongly recommends using at least a four layer PCB for all high-speed Ethernet LAN designs.
2. The typical PCB stack-up uses a signal layer on the top (component side) layer, a solid, contiguous ground plane layer on Layer 2, a solid power plane layer on Layer 3 and another signal layer on Layer 4. Layer 1 is considered the prime layer for critical routes and components because of the solid digital ground plane directly beneath it and Layer 1 also requires no vias to connect components located on Layer 1.
3. All PCB traces (especially high-speed and critical signal traces) should be routed on Layer 1 next to the solid, contiguous ground plane layer. These traces must have a continuous reference plane for their entire length of travel. This will improve EMC performance and signal integrity issues.
4. The implementation of an Ethernet chassis ground plane separate from the digital ground plane is required.
5. Avoid creating ground loops in the PCB design and the system design.
6. In order to facilitate routing and minimize signal cross talk issues, adjacent layers in a multi-layer design should be routed orthogonal.

2.7 Signal Integrity Concerns

1. Provide AC terminations for all high-speed switching signals and clock lines when required. Locate these terminations at the load end of the trace. This design issue becomes more critical with longer length traces on the PCB.
2. Provide impedance matching series terminations to minimize ringing, overshoot and undershoot on critical signals (address, data & control lines). These series terminations should be located at the driver end of the trace as apposed to the load end of the trace. This design issue becomes more critical with longer length traces on the PCB.
3. Minimize the use of vias throughout the design. Vias add capacitance to signal traces.
4. Be certain to review the entire PCB design for any traces crossing over any reference plane cuts. This will more than likely create an EMC occurrence. Refer to LANCheck reference document number ER226303, "EMI Reduction Document, PCB Design Guidelines, Reference Plane Cuts" for further information.
5. In general, review all signal cross talk design rules to avoid cross talk problems. Use the 3-W rule to provide enough trace separation to avoid cross talk problems.
6. Guard traces may also be utilized to minimize cross talk problems.

2.8 Component Guidelines

1. Verify that all components in the design meet application requirements. For instance, if the application requires operation in the Industrial Temperature range, be certain that all the other devices in the design (besides the LAN device) meet this requirement. This should include crystals, magnetics, ferrite beads, etc.
2. Verify that all components in the design meet application requirements. For instance, if the application requires operation to a specific high ESD level, be certain that all the other devices in the design (besides the LAN device) meet this requirement. This should include bypass caps (usually 2KV for Ethernet applications), magnetics, etc.
3. Review all surface mount components for proper sizing with respect to power dissipation.
4. Locate any bias resistor on the component side of the PCB.
5. In general, locate any bias resistor as close as possible to the device bias pin. Route the bias resistor with short, wide traces and connect immediately to the ground plane.
6. Do not run any traces under bias resistors. In general, it's a good PCB design rule practice to not run any traces in between any surface mount pads (resistors, capacitors, ferrite beads, etc.).

2.9 PCB Trace Considerations

1. PCB traces should be routed using 45 degree corners when changing directions. 90 degree corners should never be used.
2. PCB traces should be designed with the proper width for the amount of current they are expected to supply. The use of mini-planes in a local area on either the top or bottom layers will ensure proper current supply.
3. All component leads to any power plane or ground plane should be as short as possible. The best solutions are plane connection vias inside the surface mount pads. When using vias outside the surface mount pads, pad-to-via connections should be less than 5 – 10 mils in length. Trace connections should be as wide as possible to lower inductance. This will include any power ferrite beads feeding power planes, fuses feeding power planes, etc.

2.10 Crystal Oscillator

The crystal oscillator is sensitive to stray capacitances and noise from other signals. It can also disturb other signals and cause EMI noise. The load capacitors, crystal and parallel resistors should be placed close to each other. The ground connection for the load capacitors should be short and out of the way from return currents from USB and VBUS power lines. The load capacitors return path should be to the digital logic power supply ground plane.

Figure 2.2 illustrates a suggested PCB layout of the crystal circuit. All components are far removed from USB lines.

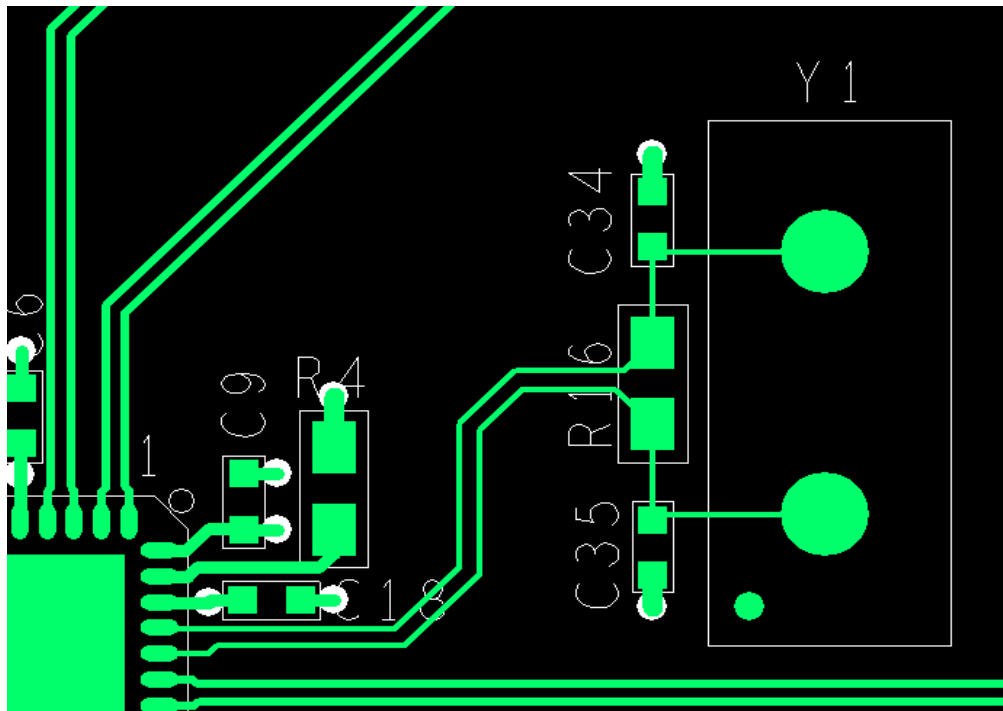


Figure 2.2 Crystal Oscillator Component Layout

2.11 VIAS in Ground Flag (Exposed Pad)

There are 36 thermal vias connecting the pad to the ground plane. Each via has a 12 mil plated hole with a 24 mil annular ring. Tolerances are +/- 2 mils. Vias are completely connected to ground plane, not cross-hatched. Via spacing is 50 mils center to center. Vias are tented with solder mask.

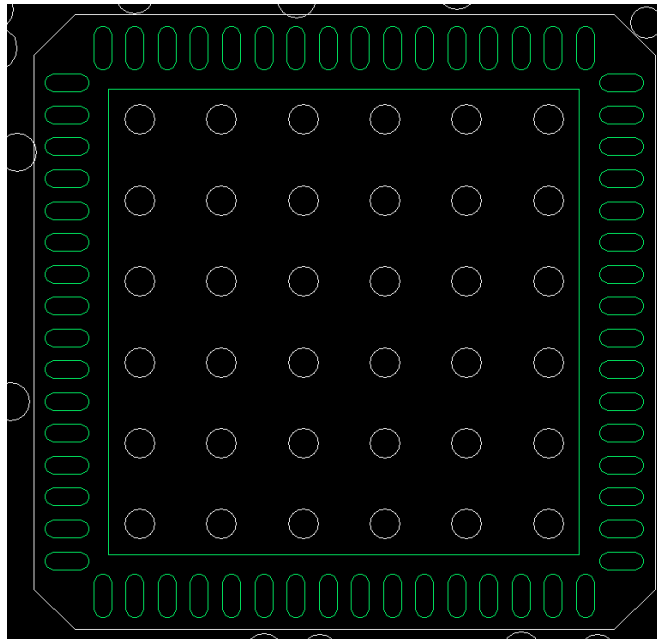


Figure 2.3 VIAS In Ground Flag (Exposed Pad)

2.12 Miscellaneous

1. Review all PCB connector interfaces for proper shielding and grounding to ensure good EMC performance. An improperly designed connector circuit may allow EMC energy to radiate from the system.

3 Recommended PCB Stack-up

3.1 PCB Recommended Stack-up

The following section outlines the recommended PCB stack-up for good EMC performance. Depending upon the specific application and EMC testing required, many stack-ups and configurations may work for the designer. However, for the highest EMC level of testing, certain PCB stack-ups perform better than others. Incorrect stack-ups may increase EMC emissions. If the product being designed must pass higher EMC test levels, the designer should consider all design points that will give his product the best chance of passing those EMC levels.

3.2 4-Layer Stack-ups

Figure 3.1 represents a 4-layer stack-up that should perform very well for the PCB designer. Each signal layer has an adjacent reference plane.

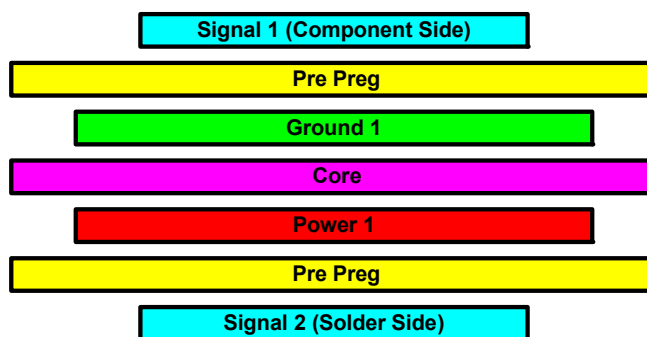


Figure 3.1 4 Layer Stack-Up

One last recommendation to our customers who have EMC testing as a requirement for their product; determine what EMC test levels you need to pass early on, design your PCB accordingly and begin EMC testing as soon as possible in your design cycle. Test early and test often; too many of our customers wait until the end of their design cycle to begin EMC testing only to find that they are not achieving passing levels with their current design. With the added pressure of impending release schedules, this is not the time to be analyzing and correcting EMC problems. The correct time in the design cycle to combat EMC problems is in the very beginning, during schematic design and PCB design.

4 USB Layout Guideline

4.1 Controlled Impedance for USB Traces

The USB 2.0 specification requires the USB DP/DM traces maintain nominally 90 Ohms differential impedance (see USB specification Rev 2.0, paragraph 7.1.1.3 for more details). A continuous ground plane is required directly beneath the DP/DM traces and extending at least 3 times the spacing width to either side of DP/DM lines. Maintain close to 90 Ohms differential impedance. For different dielectric thickness, copper weight or board stack-up, trace width and spacing will need to be calculated. Maintain symmetry between DP/DM lines in regards to shape and length.

Single ended impedance is not as critical as the differential impedance, a range of 42 to 78 Ohms is acceptable (equivalently, common mode impedance must be between 21 Ohms and 39 Ohms).

Figure 4.1 and Figure 4.2 show DP/DM traces with approximately equal trace length and symmetry. It is important to maintain a conductor width and spacing that provides differential and common mode impedances compliant with the USB specification. Use 45 degree turns to minimize impedance discontinuities.

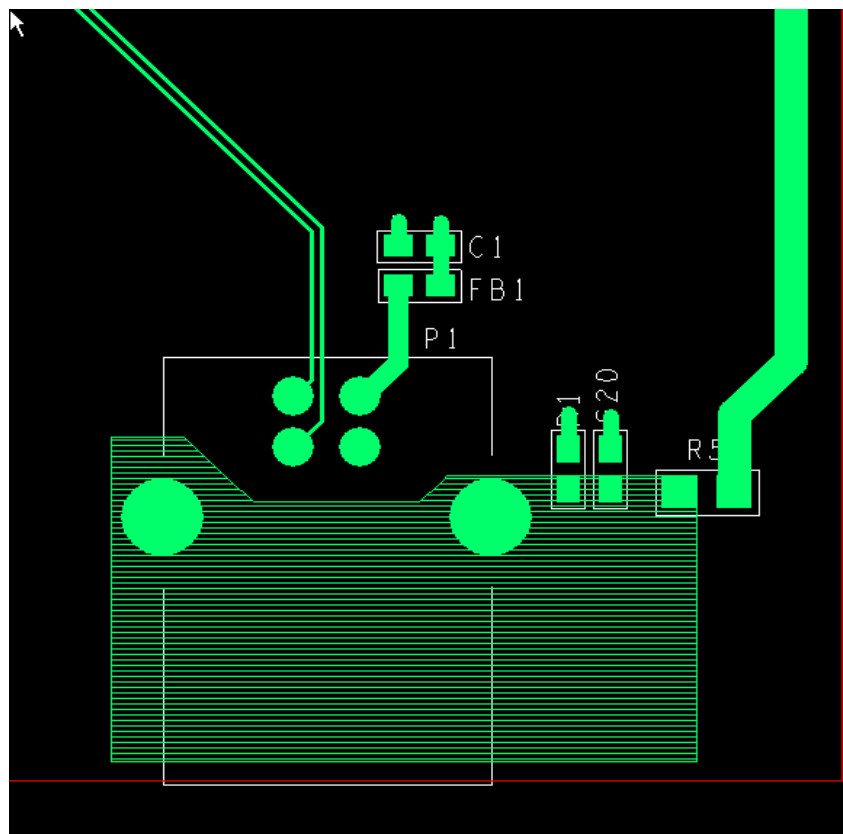


Figure 4.1 Example of Routing DP/DM to Type B Upstream Connector

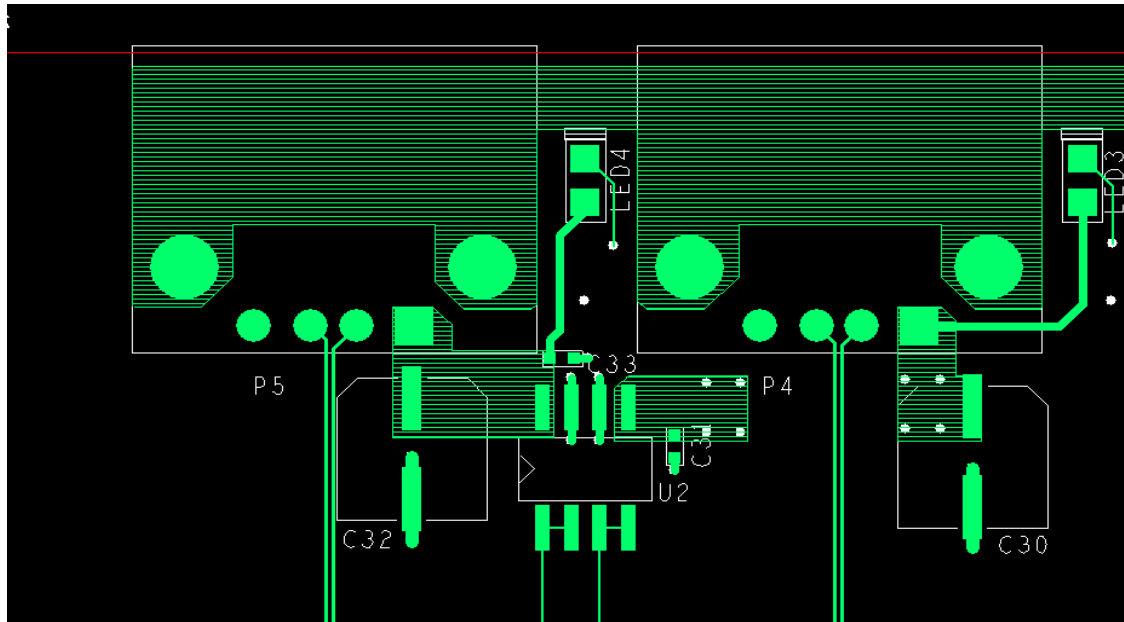


Figure 4.2 Example of Routing DP/DM to Type A Downstream Connector

4.2 Isolation of DP/DM Traces

The DP/DM traces must be isolated from nearby circuitry and signals. Maintain a distance of parts to lines that is greater than or equal to 3 times the distance of the spacing between the traces. Do not route differential pairs under parts. Do not cross DP/DM lines with other PCB traces unless the traces are on the opposite side of the ground plane from DP/DM. Route DP/DM traces over solid plane, not over power planes.

4.3 Isolated Shielding on the USB Connector

LAN9512/LAN9513/LAN9514 incorporates a USB peripheral device PHY. [Figure 4.3](#) and [Figure 4.4](#) show the Type B Upstream and Type A Downstream chassis grounds DC isolated but AC coupled to the device ground. Industry convention is to ground only the host side of the cable shield. This is done to provide cable shielding while preventing possible ground currents from flowing in the USB cable if there happens to be a potential difference between the host and device grounds.

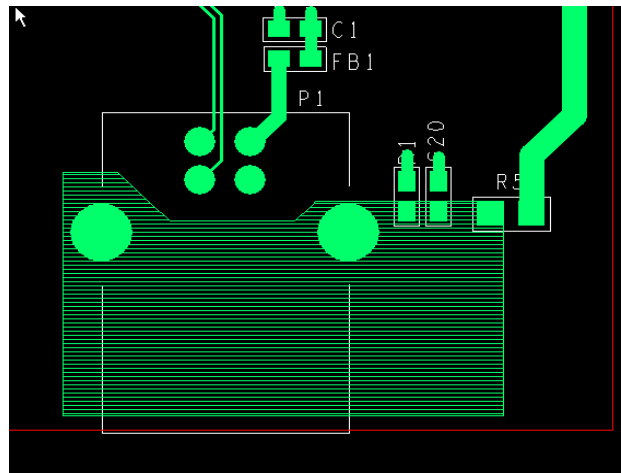


Figure 4.3 Connections to Shield of Type B Upstream USB Connector

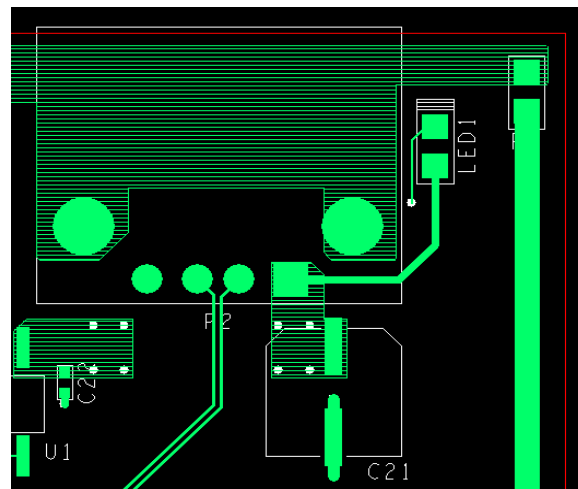


Figure 4.4 Connections to Shield of Type A Downstream USB Connector

4.4 USBRBIAS

The USBRBIAS resistor sets an internal current source reference. Thus, the USBRBIAS pin is a high impedance node and so any noise induced on the USBRBIAS traces will directly impact internal current references and negatively degrade eye-diagram quality. The USBRBIAS resistor should be placed close to the USBRBIAS pin and the ground return should be short and direct to the ground plane. Traces for resistor should be very short and isolated from nearby traces if possible.

4.5 VBUS Power Delivery from DC Supply to Downstream Ports

4.5.1 Introduction

USB2.0 specifications require that VBUS power delivered to downstream ports be between 4.75 V and 5.25 V at all times. Furthermore, on self powered hubs, current to individual downstream ports must be limited to 500 mA after 100 usec settling time after hot plug. Solely bus powered hubs are allowed (but rarely designed) and current to individual downstream ports must be limited to 100 mA.

The following sections will be targeted towards the more demanding component selection and layout requirements of self-powered hubs. They are not intended for use as a complete design guide to downstream power delivery, but rather as a PCB layout guide. They also enumerate some common mistakes in component selection and layout that can result in a non-compliant design.

4.5.2 Voltage Drop and Voltage Droop Explanation

4.5.2.1 What is Voltage Drop?

According to the USB Specification Revision 2.0, the operating voltage of the USB ports must remain in the range of 4.75 V to 5.25 V while supplying anywhere from 0 A to 500 mA per port. To ensure all downstream ports meet this requirement, a voltage drop test verifies the voltage between V_{BUS} and GND is within the 4.75 V to 5.25 V range, when all USB ports in the system are fully (with 500 mA load per port) loaded, and also when all USB ports in the system are not loaded. ¹

4.5.2.2 What is Voltage Droop?

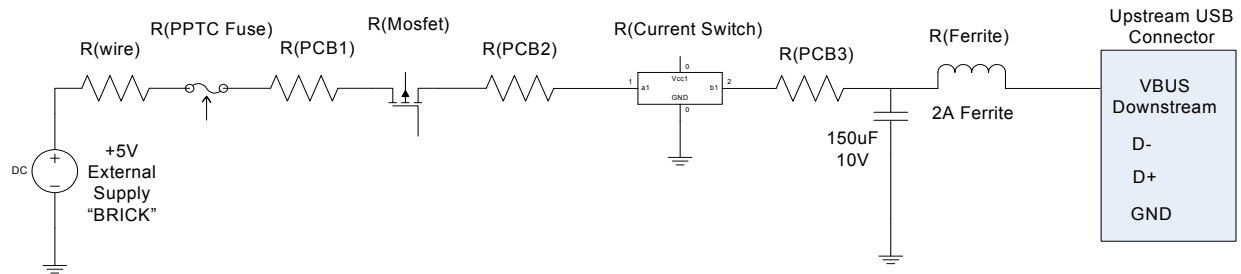
USB allows users to plug and unplug USB devices while the PC is still in operation. When a USB device is plugged into a port, inrush current occurs as the newly plugged device's internal bypass capacitor charges to its full potential. This current is drawn from the USB VBUS power plane of the motherboard and causes the VBUS to sag momentarily. This sag is referred to as droop. Voltage droop testing evaluates the port under test's ability to withstand a maximum device equivalent load of 100 mA load in parallel with a 10 μ F capacitor being hot-plugged into an adjacent port. The simulated hot-plug, generated by the droop test fixture, occurs at approximately a 1 second interval. The test is conducted with the victim port (port under test) and all other USB ports loaded with 5-unit load (500 mA) except the aggressor port (port with the simulated hot-plugging). ²

4.5.2.3 Sources of Voltage Drop and Droop

As stated before, VBUS must be between 4.75 V and 5.25 V. It is usually the lower boundary violation that causes failures. Refer to [Figure 4.5](#) for sources of resistance that cause voltage drop and droop non-compliance and an equation to determine VBUS at the downstream port when a 4 port hub LAN9514 is fully loaded. A lot of choices have to be made in component selection and routing. Budget your resistance values carefully so that you can comfortably pass the 4.75 V limit over the operating temperature of your design. A variety of PCB resistance calculators are available for calculating PCB resistance.

1. Intel Power Delivery Design Issues for Hi-Speed USB on Motherboards

2. Ibid.



$$5.25\text{Volts} \geq V_{DC_SUPPLY} - [(2.0\text{Amps} * R_{WIRE+FUSE+PCB1+MOSFET+PCB2}) + (500\text{mA} * R_{CURRENT_SWITCH+PCB3+FERRITE})] \geq 4.75\text{Volts}$$

Figure 4.5 VDROOP and VDROOP Sources of Resistance/Equation for Determining VBUS (LAN9514)

4.5.3 Elements That Contribute to VDROOP and VDROOP Failure

4.5.3.1 Improper +5V External DC Power Supply (“Brick”) Selection

The external DC supply will be referred to as a brick in the remainder of this section. Although a total of 2.5 Amps maximum is needed to power a self powered 4 downstream port hub, 2.5-3 Amp rated Bricks often have small enough guage wires to cause enough voltage drop to create VBUS voltage failures of less than 4.75 volts.

Choose a Brick that is rated at 4 A. Although further testing is required, if the 4 Amp specification is met, one will most likely not encounter of failure because of Brick selection. SMSC recommends, and ships with Customer Evaluation Boards, the Brick manufactured by Cincon Electronics Co., Ltd – model number TR25050-A-11A03.

4.5.3.2 Improper sizing of Circuit Protection Element

The use of an underrated fuse element can cause voltage drop failure. An underrated fuse element is likely to have a higher than desired resistance, thus adding excessive voltage drop across the component. Polymeric Positive Temperature Coefficient devices, commonly referred to as polyfuses, will be abbreviated PPTC in the rest of this section. The commonly used PPTC in USB Hubs exhibits exponential increase in resistance with increase over ambient temperature, thus resulting in increased voltage drop. Improper sizing here can result in USB compliance failure.¹

PPTC fuses are really only suitable on Brick input power, not power switching to downstream ports. Choose a PTC fuse that has a Rmax of less than 150 mOhms after exposure to reflow and/or tripping. Be wary of the Rmax specification for the device before it has been exposed to heat.

Downstream Circuit Protection should be handled with a Port Power Management Device (PPMD). When downstream current exceeds 500 mA in a USB2.0 compliant design, power should be switched off to downstream port and the hub controller must be informed. Choice and design of Port Power Protection Devices is beyond the scope of this document. Refer to LAN9512/LAN9513/LAN9514 reference designs for one particular choice of PPMD – keeping in mind that there are myriad of devices available.

1.Intel Power Delivery Design Issues for Hi-Speed USB on Motherboards.

4.5.3.3 Improper Sizing of Ferrite Bead

Ferrite Beads or chokes are often used in series with VBUS Downstream Port Power routing to limit EMI. The LAN9512/LAN9513/LAN9514 devices do not require these parts to meet EMI testing, but some designers use them to achieve additional guard band or when in EMI constrained environments.

When used, the maximum current capability should be 4 times the maximum expected value of current. In the case of series ferrite beads in VBUS Downstream Port Power routing, the maximum current specification should be at least 2 Amps.

4.5.3.4 Inadequately Chosen Downstream Port Bulk/Bypass Capacitor

It is important to provide sufficient bulk/bypass close to each downstream port to prevent VBUS downstream port power to dip below 4.75 V on hot plug insertion. One common mistake is to choose too low a value capacitor to supply sufficient short term energy. SMSC recommends a 150 μ F 10V capacitor or greater. ESR of the capacitor should be less than 100 mOhms over spectrum from DC to 100 MHz.

Multiple capacitors may be used if the total value of capacitance reaches 150 μ F, although a single capacitor is generally preferred because the total distance from the output of the Port Power Management Device to the capacitor to the downstream USB Type A connector should be as short as possible to limit IR drop in the PCB traces.

4.5.3.5 Inadequate PCB Trace Width

The most common cause of voltage drop and droop failures is the resistance of the PCB trace from the Brick voltage to the Port Power Management Device to a Power MOSFET to the Port Bulk/Bypass capacitor to the downstream Type A connector. Refer back to [Figure 4.5](#) to see the three PCB interconnects involved.

Power should be routed over an at least 50 mil wide trace with at least 1.5 oz. copper after plating. Power routed in internal layers should be routed over shapes/planes rather than trace. Use multiple vias of at least 1.2mm when transitioning from layer to layer. Ideally power should be routed entirely over shapes and planes. Refer to the following figures to see how power was routed to and from the Port Power Management Device and bulk bypass capacitor. Following these practices on all your USB VBUS power routing and PCB layout will contribute to a USB 2.0 compliant design.

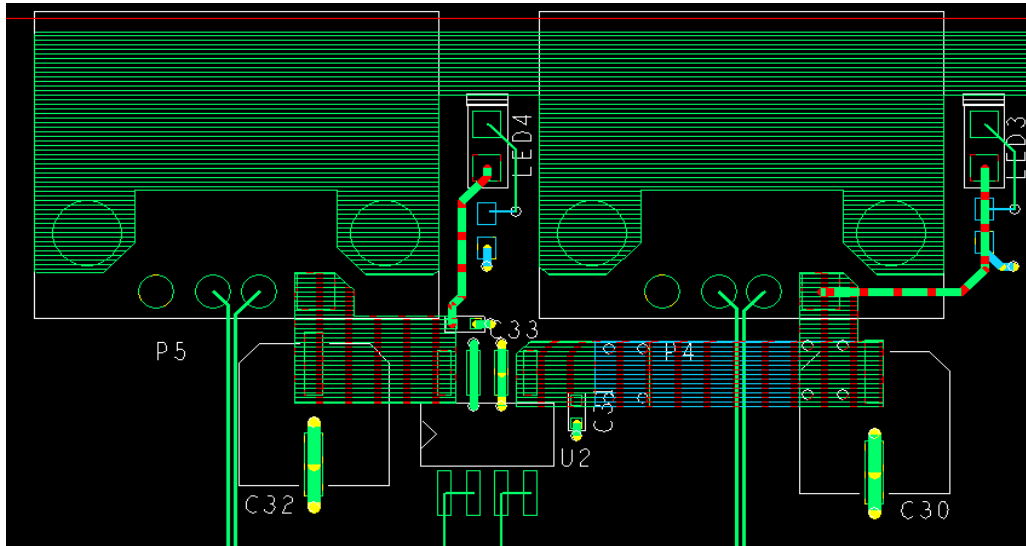


Figure 4.6 Output of Port Power Management Device

Note: The routing of the output of the Port Power Management Device (U2) to the bulk/bypass capacitors (C30 and C32) to the downstream Type A USB connectors (P4 and P5) in on layer 1 (green with red striping).

Also note that the GND (green with yellow striping) is double viaed on the Port Power Management Device (U2) and on the bulk/bypass capacitors (C30 and C32).

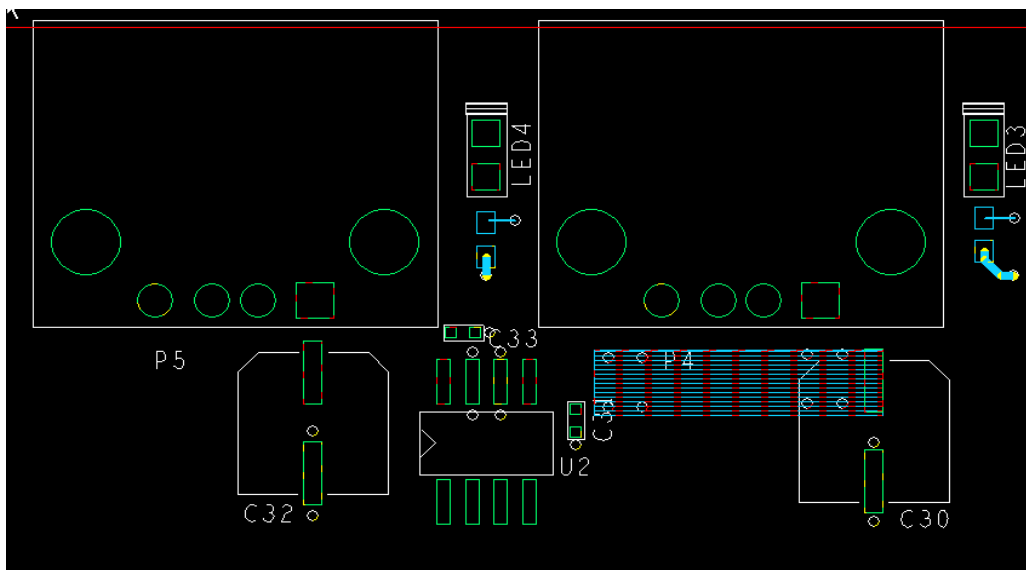


Figure 4.7 Transitioning Between Layers

Refer between [Figure 4.6](#) and [Figure 4.7](#) and notice how the output of the Port Power Management Device (U2-pin5) has four vias when making a transition from layer 1 to layer 4 that was needed to allow proper routing of the DP/DM pair to P4 on layer 1. Notice that the PCB connection on layer 4 in [Figure 4.7](#) (blue striped with red) is also a shape and not a trace.

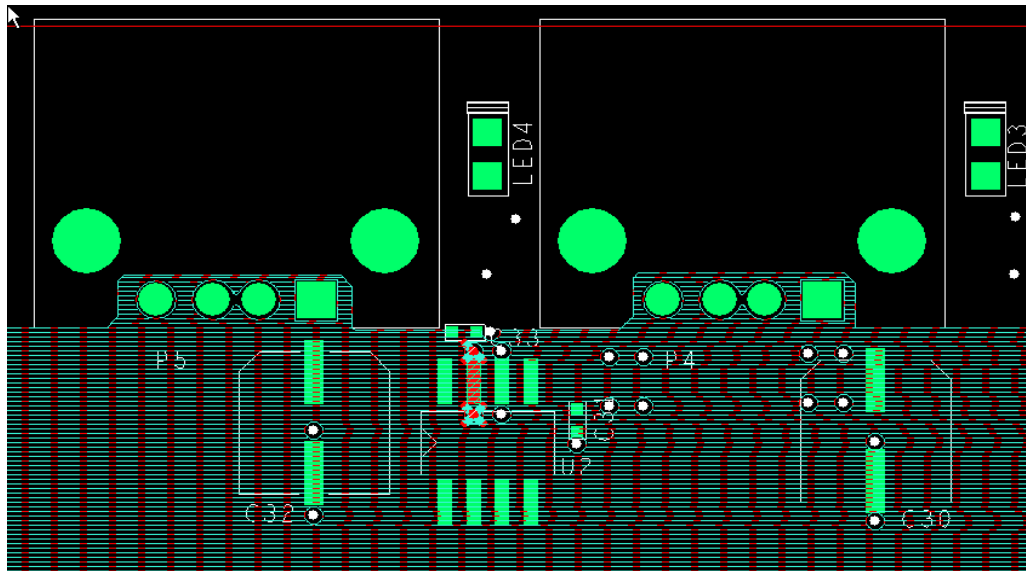


Figure 4.8 5 Volt Plane to Port Power Management Device

Note in [Figure 4.8](#) that a solid plane on layer 3 (teal striped with red) supplies power through two vias to the Port Power Management Device (U2).

5 Ethernet Layout Guideline

5.1 TX+/- & RX+/- Differential Pairs

1. Both RX+/- and TX+/- pairs should be routed as differential pairs. This includes the entire length of travel of the traces from the RJ45 connector to the LAN device.
2. RX+/- and TX+/- differential pairs should be routed as close together as possible. Typically, when beginning the impedance calculation, the smallest trace space (4 – 5 mils) is selected. The trace width is then adjusted to achieve the necessary impedance.
3. Differential pairs should be constructed as 100 Ohm, controlled impedance pairs.
4. Differential pairs should be routed away from all other traces. Try to keep all other high-speed traces at least .300" away from the Ethernet front end.
5. Each trace of the differential pair should be matched in length.
6. The differential pairs should be as short in length as possible.
7. The use of vias is not recommended. If vias are used, keep to a minimum and always match vias so the differential pairs are balanced.
8. Layer changes are also not recommended. Keep the differential pairs referenced to the same power/ground plane whenever possible.
9. For optimum immunity, route Transmit pairs and Receive pairs as far away from each other as possible.
10. Always reference any Transmit terminations to the same reference plane that the Transmit routes are referenced to. Likewise, always reference any Receive terminations to the same reference plane that the Receive routes are referenced to.
11. Precedence should be given to the differential pair routing. Terminations should be added after the routing is determined. The terminations should simply be "dropped" onto the differential routing.
12. All resistive terminations in the Ethernet front end should have values with 1.0% tolerances.
13. All capacitive terminations in the Ethernet front end should have tight tolerances and high quality dielectrics (NPO).
14. For optimum separation, experimentation can be explored with inserting a ground plane island between the Transmit pair and the Receive pair. A separation from this ground plane from any of the traces of 3 – 5 times the dielectric distance should be maintained.
15. This same technique can be used to separate different Ethernet ports if port cross talk is an issue. A ground plane can be inserted between Ethernet channels. The separation space between the two channels should be as wide as possible. Again, a separation from this ground plane from any of the traces of 3 – 5 times the dielectric distance should be maintained.

Figure 5.1 illustrates TX/RX differential pair routing. In this example, routing is not ideal because a tab up RJ45 jack was used and the RX lines wrap around the connector.

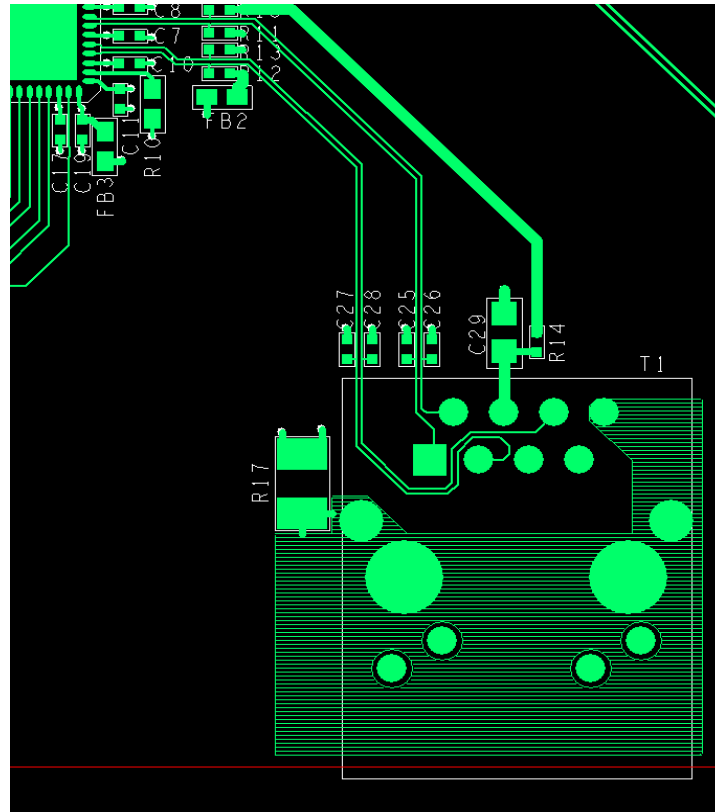


Figure 5.1 TX/RX Differential Pair Routing

5.2 Unused Cable Pairs

1. The unused cable pairs (pins 4, 5, 7 & 8 on the RJ45 connector) should be properly terminated for common mode considerations.
2. These terminations should be routed with heavy, short traces.
3. Place these terminations as close as possible to the RJ45 connector.
4. Terminate these resistors to a proper chassis ground plane through a high voltage (2KV) capacitor.

5.3 RJ45 Connector

1. A shielded, metal enclosed RJ45 connector is recommended.
2. The metal shield should be connected directly to a proper chassis ground plane.
3. To maximize ESD performance, the designer should consider selecting an RJ45 module without LEDs. This will simplify routing and allow greater separation in the Ethernet front end to enhance ESD/susceptibility performance.
4. Another ESD enhancement may be to use of an RJ45 connector with surface mount contacts. This may simplify routing and allow greater separation in the Ethernet front end to enhance ESD/susceptibility performance.

5.4 Magnetics

1. There are many different types and configurations of magnetics available for use with any particular LAN device. Different packages, orientations, sizes are all factors that need to be considered when selecting magnetics. For all our SMSC LAN devices, it is our recommendation is to use a qualified, recommended magnetic from our “Suggested Magnetics” application note. This application note is available from our website.
2. If the design engineer chooses to select an alternate magnetic for his application, he should take certain steps to ensure a proper match to our LAN devices. Again, referring to our “Suggested Magnetics” application note, the designer should use a tested and qualified magnetic from that application note as his reference. By obtaining the data sheet for that preferred magnetic and using it for comparison, the alternate magnetic can be evaluated. By comparing the specifications from the two data sheets, the design engineer can make an informed decision on how the alternate magnetic compares to the recommended and if it is suitable for use with the particular SMSC LAN device.
3. Generally speaking, the magnetics should be placed as close as possible to the RJ45 connector. In the case of the LAN9512/LAN9513/LAN9514, SMSC recommends 0.50” at a minimum and 0.75” at a maximum.
4. Depending upon which style of magnetic selected (North/South or East/West) will determine the orientation of the magnetics as related to the RJ45 connector. Be certain the network side of the magnetics faces the RJ45 connector and the device side of the magnetics faces the LAN device. This will ensure that the high voltage barrier through the middle of the magnetics can be correctly routed and designed on the PCB.
5. Ideally, the LAN device should then be placed as close as possible to the magnetics. If this is not possible, the RJ45 connector and magnetics must remain in close proximity. The LAN device then can be located somewhat remotely from the RJ45/magnetics area. In the case of the LAN9512/LAN9513/LAN9514, SMSC recommends a distance between the device and the magnetics of 1.0” at a minimum and 3.0” at a maximum.
6. To maximize ESD performance, the designer should consider selecting a discrete transformer as opposed to an integrated magnetic/RJ45 module. This may simplify routing and allow greater separation in the Ethernet front end to enhance ESD/susceptibility performance.

5.5 PCB Layer Strategy

1. In typical applications, power planes and digital ground planes are run from the LAN device to halfway through the magnetics module.
2. Typically, all planes are cleared out on the PCB in the area from halfway through the magnetics to the RJ45 connector. The TX+/- and RX+/- pairs should be the only traces in this cleared out region of the PCB. This creates one part of the high voltage barrier required for LAN applications.
3. Then, a chassis ground plane is designed up around the RJ45 connector. Once the plane shape is determined, this same shape should then be mirrored on all layers of the PCB.
4. Keep the chassis ground plane dimensions in a 6:1 ratio. Any sizing smaller than this results in the plane looking and acting more like a trace than a plane.
5. Do not allow any other plane or trace overlap the chassis ground plane. This will reduce the isolation/protection performance of the chassis ground plane.
6. Review basic Chassis Ground Plane Design Guidelines for PCBs before committing to a PCB assembly.

5.6 TX/RX Channel Crossover

1. Depending upon RJ45 orientation (Tab-up or Tab-down), the magnetics selected and the LAN device pin-out, a TX/RX channel crossover may be required at the PCB level. This practice is not recommended but when it is unavoidable, it can be accomplished.
2. When designing a crossover at the PCB board level, care should be taken. Typically, the recommendation is to leave the transmit channel intact on the top signal layer referenced to a solid digital ground plane. Since the Receive channel, in general, is more forgiving, the crossover can be performed on the Receive channel.
3. The crossover begins by taking the RX+/- pins from the LAN device immediately to the bottom layer through matched vias. The pairs can then be run completely on the bottom layer, if necessary, to complete the crossover function.
4. The crossover should have matched vias in each of the RX traces. This will balance the pairs as best as possible. The use of vias should be kept to a minimum for this crossover function.
5. The RX traces should also be matched in length as best as possible.
6. Keep all the routes as short as possible.

5.7 EXRES

The EXRES resistor sets an internal current source reference. Thus, the EXRES pin is a high impedance node and so any noise induced on the EXRES traces will directly impact internal current references and negatively degrade eye-diagram quality. The EXRES resistor should be placed close to the EXRES pin and the ground return should be short and direct to the ground plane. Traces for resistor should be very short and isolated from nearby traces if possible.

5.8 EMI Caps

For added EMC flexibility, SMSC recommends the addition of four small common mode caps to the differential pairs. Add a 15 pF cap to digital ground to each of the TXP, TXN, RXP & RXN lines of the LAN9512/LAN9513/LAN9514. Add them into your design as Do Not Populates (DNP). Then, if you run into any EMC trouble down the line, you can simply add these caps to your PCB in order to experiment with EMI reduction.

6 EMI Considerations

6.1 PCB EMI Design Guidelines

Designing for EMC success must be considered during the schematic design and the PCB design cycles within the overall product design cycle. EMC design violations are especially critical to any Ethernet product simply due to the relationship between an Ethernet enabled device and EMC testing. Any circuit, anywhere inside the system enclosure, can generate EMC energy. The EMC energy will attempt to exit the system through any opening in the metal enclosure or at any cable making a system connection.

This leads to the following situation; first order evaluations identify the Ethernet portion of the design as the source for the radiated energy. More times than not, upon further investigation, we find that the Ethernet portion of the design is designed and implemented correctly. Upon closer examination, we find offending designs have an “EMC generator” residing elsewhere in the design on the system PCB. The radiated energy is simply exiting the system at the Ethernet port. Upon correcting the source of the problem, the offending system usually passes testing with a much lower EMC signature.

Another phenomenon that we see in these situations is the incorrect first reaction by our customers to these EMC problems. SMSC has noticed a trend where PCB designers will react by introducing a band-aid for these EMC violations rather than to identify and correct the source of the EMC energy. Designers will try to include series resistors; series ferrite beads and additional common mode chokes on the Ethernet differential transmit pairs to reduce EMC levels. For obvious reasons, this is not the correct course of action. The EMC problem must be investigated and the “EMC generator” in the system must be identified and corrected. The problem is best corrected at the source.

6.2 Identify Critical Circuits

- Emissions – Clocks, buses and other repetitive circuits
- Immunity – Resets, interrupts and critical control lines

6.3 Choose Devices with EMI in Mind

- Slower is better – rise times and clocks
- Watch out for high-speed CMOS – both signal and power

6.4 Choose a Board Design

- Multilayer boards are 10 to 100 times better for both emissions and immunity
- Five-Five Rule – use multilayer boards for clocks >5 MHz or rise time <5 nSec
- Do not embed traces in power or ground planes

6.5 Do The Initial Layout

- Separate high- and low-speed sections
- Keep critical circuits away from I/O circuits
- Hand route critical lines
- Terminate traces based on 2-in./nSec rule. Unterminated PCB traces should be less than 2 * (rise time of signal in nSec) inches in length.

6.6 Pay Attention to Power Decoupling

- Decouple every power pin with a high-frequency capacitor
- Bypass every power input to board with a high-frequency capacitor
- Keep capacitor leads short

6.7 Pay Attention to Connectors

- Keep critical circuits away from connectors
- Use adequate ground returns (5:1 minimum for high-frequency circuits)
- Watch out for internal-cable sneak paths

6.8 Special Concerns for Clocks

- Keep the hot leads short
- Add small damping resistors or ferrites to clock outputs
- Control clock routing
- Watch out for noisy oscillator modules

6.9 Special Concerns for Resets, Interrupts & Control Lines

- Add high-frequency filtering at circuit inputs
- Control trace routing
- Do not cross any plane splits with high-speed signal traces

6.10 Special Concerns for I/O Circuits

- Three EMI paths through I/O – signal, power & ground
- Add high-frequency filtering to all I/O lines – even slow I/O
- Isolated I/O planes can help but must be done correctly

6.11 Test Early and Often

- Don't wait until the end to do EMI testing
- Develop and implement your own engineering-level EMI testing
- Objective is to improve probability for success in compliance tests

7 ESD Considerations

7.1 Ethernet Specific Considerations

1. The RJ45 connector must have a metal shield to ensure the highest ESD performance.
2. The metal shield of the RJ45 connector must be connected directly into the system's chassis ground plane at two points.
3. For increased ESD protection, the design engineer should consider using an RJ45 connector that does not have integrated LEDs. Selecting an RJ45 connector without LEDs will simplify the design of the high-voltage barrier and simplify any troubleshooting of the ESD hardness of the product.
4. Another ESD enhancement to consider is the choice of integrated magnetics vs. discrete magnetics. Since the basic concept of good ESD performance is separation, the discrete magnetic choice may be the wiser selection. The belief is that it is simply easier to get the proper spacing for all the components in the Ethernet front end with discrete magnetics. Using discrete magnetics will also greatly simplify any troubleshooting of the ESD hardness of the product.
5. All power planes and non-Ethernet traces must be cleared out from halfway under the magnetics to the RJ45 connector. Separation should be maintained for at least .250".
6. The choice and placement of the magnetics is also very important for high ESD performance. Depending on space and location on the PCB, magnetic modules must be selected and placed according to their construction. North/South magnetics are pinned out differently than East/West magnetics and must be placed accordingly on the PCB. The size of the magnetic module may prove to be important. All these factors have an affect on the design and outcome of the high-voltage barrier required by the Ethernet interface.
7. The PCB on which the Ethernet circuitry resides should rest on metal stand-offs that are at least .250" high (or higher if solder nibs are not trimmed) off the metal case of the product.
8. The choice and placement of the specific RJ45 connector may also have a very high impact on the ESD performance of the product. RJ45 connectors with the chassis ground tabs as far away from the 8 pin connections may prove to be the best configuration for ESD. Placement of the RJ45 connector with respect to other connectors and overall PCB location may also be very important in overall ESD performance.
9. Be certain to check that all circuitry related to and residing in the high-voltage barrier region is referenced to chassis ground only. LEDs, capacitors, transorbs, anti-parallel diodes referenced to digital ground in the high-voltage barrier area will compromise the high-voltage barrier.

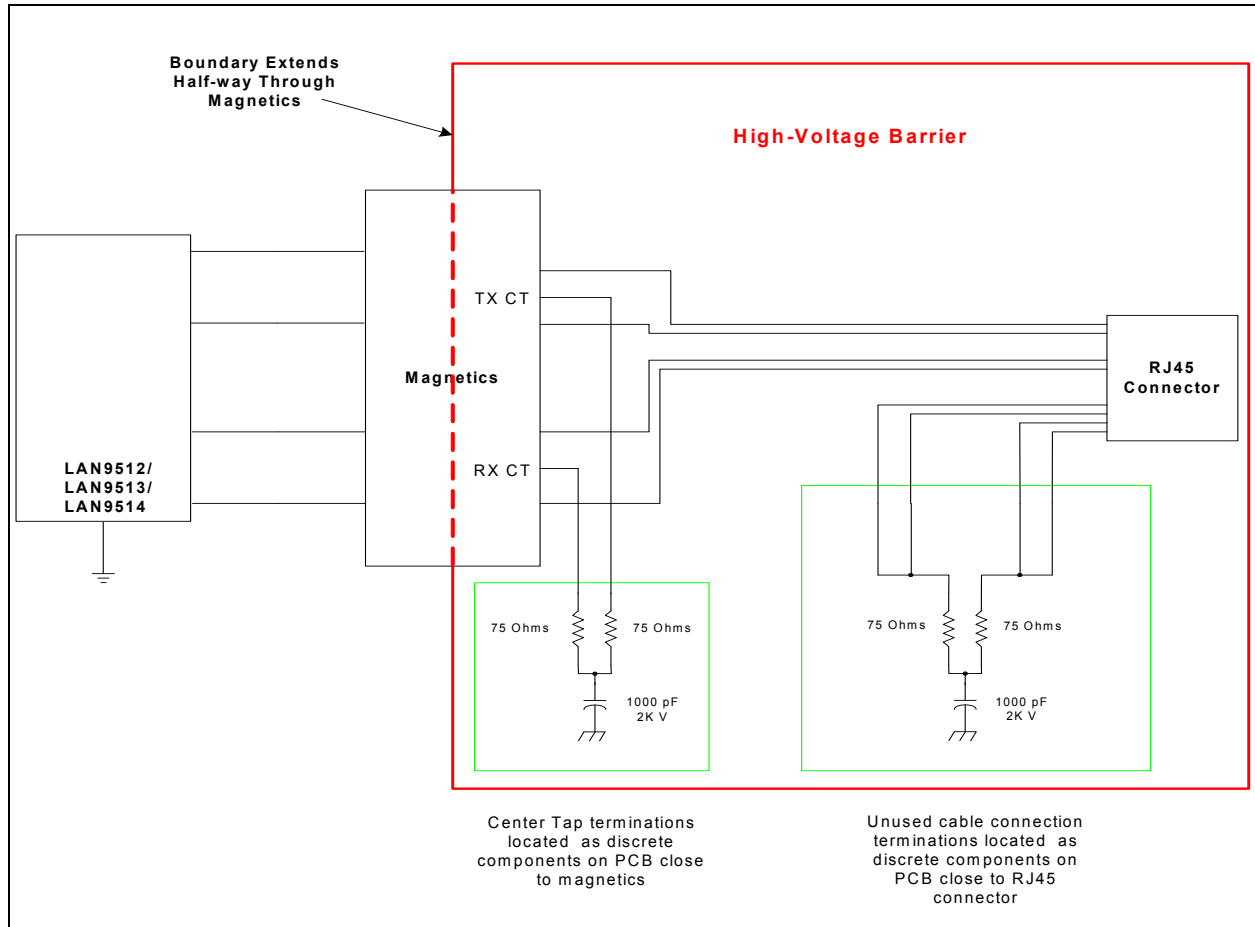


Figure 7.1 Schematic of Ethernet and USB Front End

7.2 Power Supply Considerations

1. Power supply voltage wires should be twisted tightly together with their return wires.
2. All power entries to the PCB must be bypassed properly as close as possible to the power connector on the PCB.

7.3 PCB Layer Strategy

1. SMSC strongly recommends using at least a four layer PCB for all high-speed Ethernet LAN designs. Multi-layer PCBs are very important in order to control ESD problems.
2. The implementation of an Ethernet chassis ground plane completely separate from the digital ground plane is required.
3. The chassis ground plane should be mirrored on every layer of the PCB. Each chassis ground plane on each layer should then be stitched together with multiple vias placed 0.500" apart.
4. Use a large plated hole to connect the chassis ground planes to the metal enclosure (Earth ground). This mounting hole should have large, conductive pads on both the component side and solder side of the PCB. These two large, conductive pads should also be stitched together with multiple, plated through vias. The pads should also be free from solder to ensure a good, flat surface to mate with the metal standoff.
5. All chassis ground plane connections must have low impedance connections. Short traces and multiple via connections will attain this.
6. This Earth ground connection mounting hole should be located within 1.0" of the RJ45 connector.
7. Locate the Earth ground connection(s) away from sensitive circuitry. This strategy will force the flow of an ESD occurrence away from the sensitive circuitry and direct it to Earth ground.
8. All other connectors in the system should also incorporate a chassis ground beneath them. Any connector going to the outside world is a candidate for a chassis ground plane.
9. Any other PCB mounting hole can be designed with optional digital ground plane connections through a wide SMD footprint. In this case, each of the other mounting holes in the design can be configured as a soft ground (500 – 1K Ohm jumper), hard ground (zero Ohm jumper), separate from ground (no connection) or an AC-coupled connection to ground (high voltage capacitor). This will give the designer the flexibility required to shape the ESD profile of his product to his exact test needs.

7.4 Signal Integrity Concerns

1. All signal traces throughout the design should be kept to a minimum. Consider adding a digital ground "guard trace" to signal traces over 8" long.
2. Place I/O circuits close to their respective connectors. This will minimize trace length and susceptibility.
3. ESD occurrences can cause digital ground plane "ground bounce" if allowed to enter the digital ground plane. This can cause erratic system behavior and/or system failure. Every effort should be taken to make sure that any ESD source is not allowed to enter any digital ground or power plane on the PCB.

7.5 Component Guidelines

1. Verify that all components in the design meet application requirements. For instance, if the application requires operation to a specific high ESD level, be certain that all the other devices in the design (besides the LAN device) meet this requirement. This should include bypass caps (usually 2KV for Ethernet applications), magnetics, etc.
2. Review all component placing guidelines for proper clearance (.250") from outside metal cases, board edges and chassis ground plane contacts.

7.6 PCB Trace Considerations

1. All component leads to any power plane or ground plane should be as short as possible. The best solutions are plane connection vias inside the surface mount pads. When using vias outside the surface mount pads, pad-to-via connections should be less than 5 – 10 mils in length. Trace connections should be as wide as possible to lower inductance. This will include any power ferrite beads feeding power planes, fuses feeding power planes, etc.
2. Review all signal traces for proper clearance (.250") from outside metal cases, board edges and chassis ground plane contacts.

7.7 Miscellaneous

1. Review all PCB connector interfaces for proper shielding and grounding to ensure good ESD performance. One improperly designed connector circuit may allow ESD energy to enter the system and cause system failure.
2. As with EMI testing, the same can be said of ESD testing. The design engineer must design in ESD safeguards at the onset of his design. The design should then be tested as soon as possible in the prototype stages of the design. In order to ensure compliance at the production release time of the schedule, the product must be ESD tested early and as often as possible. To wait until the end of the design cycle to find out about the system's ESD hardness would be a huge mistake.

8 Application Note Revision History

Table 8.1 Customer Revision History

| REVISION LEVEL & DATE | SECTION/FIGURE/ENTRY | CORRECTION |
|------------------------|----------------------|---------------------------------------|
| Rev. 1.1 (02-04-10) | All | LAN9513 added throughout the document |
| Rev. 1.0 (05-15-09) | Initial Release | |



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