Signal Integrity and Power Integrity Analysis around the SDRAM Bus Activity Using an AT91SAM9260 Microcontroller

AT91 ARM Thumb-based Microcontrollers

Application Note

1. Introduction

In the past, the primary concern for digital designers was to ensure timing compatibility between on-board devices. Device specifications pertaining to setup and hold timing were the critical parts of the interconnection between two devices. As soon as this stage was completed, the designer had only to lay out the trace without other considerations.

Now, with the evolution in technology, another aspect must be taken into account before laying out any trace between two devices on a printed circuit board. The trace has to be considered as a component with recognition that “a perfect world” does not exist during the transient event of a digital signal.

This explains why the IBIS model file is becoming important for applications having high frequency bus accesses. The electronic engineer can predict the trace behavior after a transient event using such a model file.

A Synchronous Dynamic Random Access Memory (SDRAM) Controller is embedded in the latest generation of Atmel’s AT91SAM microcontrollers with more constrained timing requirements. With shorter timings, transient time and steady delay are implicitly reduced to be consistent with this evolution. This timing reduction race has various impacts. The span of rising and falling edge times becomes too short versus the non-evolution of board material (physical characteristics of the PCB); subsequently, the risks of parasitic noise and lost signal, as well as the risks to power supply integrity are increased.

In Section 1. “Introduction” and Section 2. “Extracting Data from the IBIS File”, this document gives required electrical characteristics derived from the IBIS Model file of the device. Extraction methods are presented regarding the buffer impedance and edge shape, in order to derive electrical values.

Section 3. “PCB Electrical Characteristics” and Section 4. “Power Supply Bypass”, using data from the first two sections, provide explanations and data concerning the requested trace characteristics and bypass circuitry.

The last section, Section 5. “From Theory to Practice: QFP and BGA Routing Examples”, is an exhaustive presentation of designs using the AT91SAM920 device in QFP and BGA packages, provided by Atmel.

Note: Although this Application Note nominally pertains to the AT91SAM9260 microcontroller, the theoretical and practical aspects described can be applied generally with specific variances across the entire range of Atmel’s AT91 ARM® Thumb®-based Microcontroller products.

6386A–ATARM–06-Jul-09

1.1 Associated Documents and Software

- AT91-AN02: Signal Integrity and AT91 Products (Basic Relationships between IBIS Data and your PCB)":
  This Application Note gives the rule of thumb to calculate trace length limitation according to digital signal shape. It contains useful information that is not repeated in this document.
- AT91SAM9260_bsdl_ibis.zip software file:
  Associated with the AT91SAM9260 Device, this file contains all buffer specifications, boundary scan chain information (BSDL) and IBIS.
- AT91SAM9260 PCB layout file:
  Contains both PCB projects under Cadstar V9 PCB design tool by Zuken.

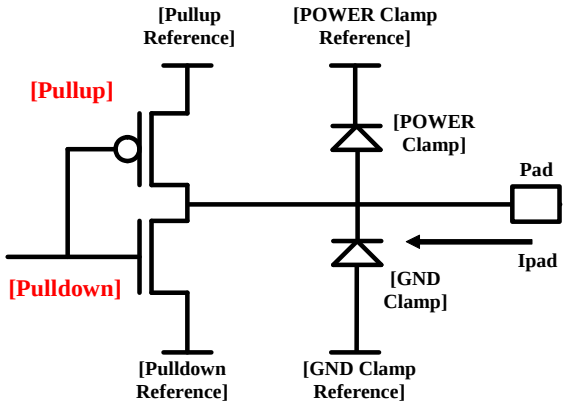
See Atmel website: http://atmel.com/AT91SAM 32-bit ARM-based Microcontrollers

1.2 Terminology and Definitions

Some of the terminology and technical definitions used in this document are given below.

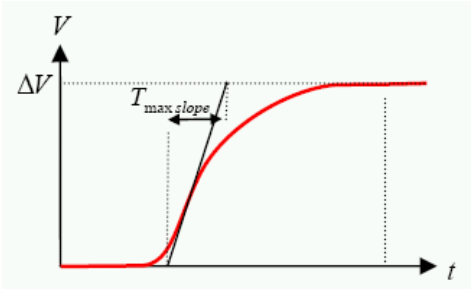
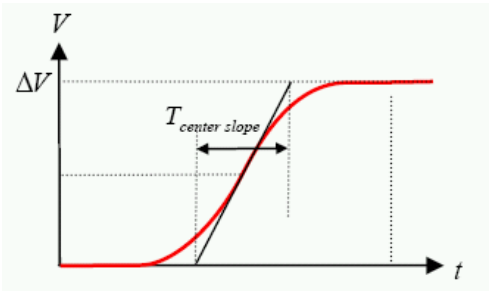
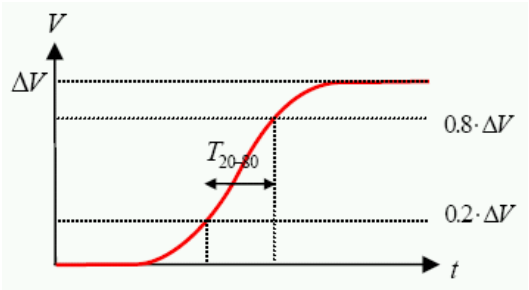
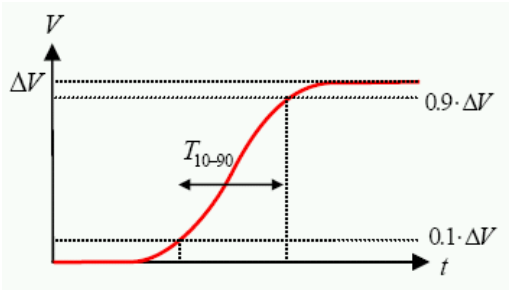
PCB	**P**rinted **C**ircuit **B**oard
ESD	**E**lectro**S**tatic **D**ischarge
ESL	**E**quivalent **S**eries of "**L**" Inductance used to describe the inductive parts of the impedance of certain electrical components or physical material: trace, capacitor, resistor, chip bounding, etc.
ESR	**E**quivalent **S**eries **R**esistance is an effective resistance that is used to describe the resistive parts of the impedance of certain electrical components or physical material: trace, capacitor, chip bounding
SSN/SSO	**S**imultaneous **S**witching **N**oise and **S**imultaneous **S**witching **O**utput expressions. Simultaneous output switching is often a main cause of application noise at several levels. It is the first thing to consider apropos the IO power rail bypass method.
IBIS	**I**nput/Output **B**uffer **I**nformation **S**pecification. IBIS is a template (standard, data-exchange format, etc.) for exchanging model information between semiconductor device suppliers, simulation software suppliers and end users of this information.
Clamp Diode	ESD oriented protection. It is used for clamping abnormal voltage levels. (refer to Figure 1-1)
Pullup Pulldown	IBIS designation of circuits used to switch the output, respectively, to high or low voltage level. (refer to Figure 1-1)
Rising & Falling Time	Four methods of Rising and Falling time extraction are shown in Table 1-1 on page 4

Figure 1-1. Conceptual Diagram of Model Keyword Structure



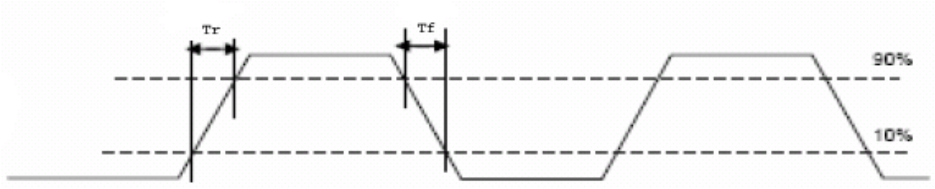
Four methods are used to extract rising or falling time from experimental oscilloscope measurements or display curves from a simulation. These methods are described below:

Table 1-1. Rising or Falling Extraction Methods

Maximum Slope	
Center Slope	
20% to 80% Slope	
10% to 90% Slope	

The example below uses the "10% to 90% Slope" method. The necessary delay for a signal transition increases from 10% up to 90% (T_R), or decreases from 90% to 10% (T_F) of the final level.

Figure 1-2. Rising and Falling Time on a Digital Signal



Die Capacitance (C_comp) designation in IBIS Model:
Defines the capacitance of each pad (the "C_comp" [1]parameter). This is the capacitance seen when looking from the pad into the buffer for a fully placed and routed buffer design, exclusive of package effects.

***F_{KNEE}* Frequency** Common frequency parameter used in signal integrity and electromagnetic domains. In digital electronics, the F_{KNEE} frequency value is deducted from the rising or falling time. This value defines the frequency below which most energy in digital pulses is concentrated. A means to facilitate the transition from time to frequency domain. (refer to Figure 3-3. "Clock Frequency, FKNEE and Slope Spectral Spreading")

Note: 1. "Cdie" or "die capacitance" may be used in other industry contexts to refer to the capacitance of the entire component as measured between the power and ground supply rails.

2. Extracting Data from the IBIS File

Data given in the IBIS file provides a fast and accurate way of extracting a buffer's overall process conditions. This study focuses on output buffer impedances and edge slopes.

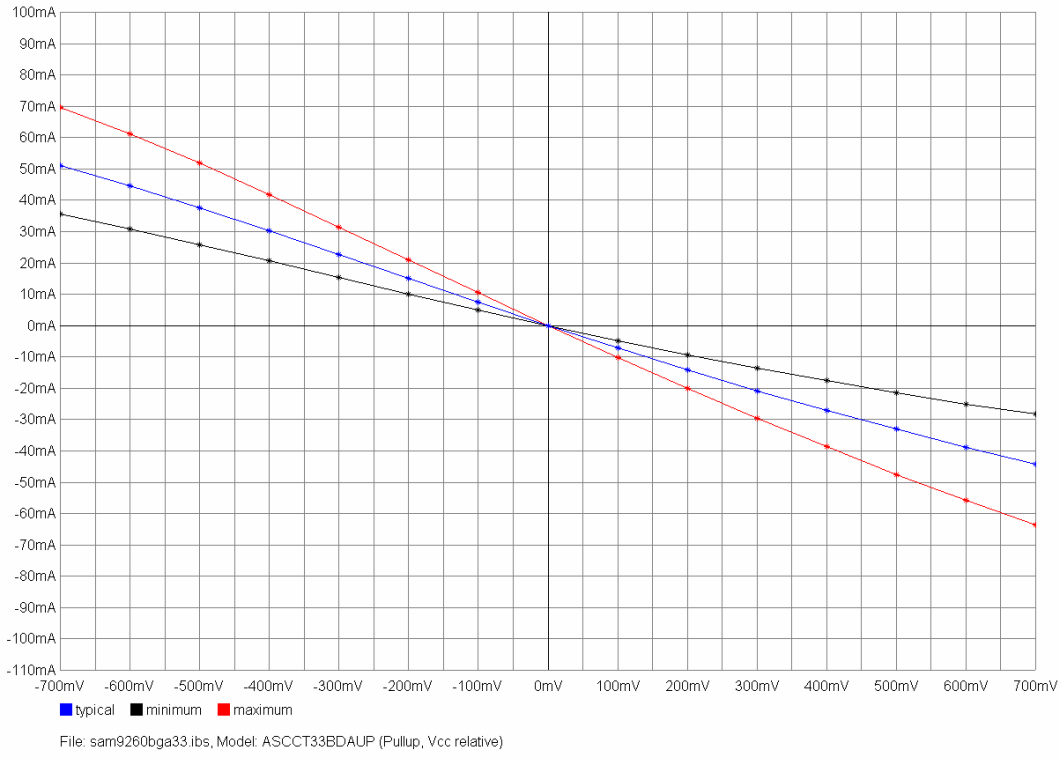
2.1 Output Buffer Impedance for Address, Data and Control Busses

This paragraph describes the method to extract the output buffer impedances of the AT91SAM9260. This method is based on "Pullup" and "Pulldown" IBIS curves. These are usually called I-V Curves because they are the result of current drive vs. voltage. These curves can be non-linear. But, in the unclamped midrange, they can usually be approximated by a straight line calculation of:

$$Z_{OUT} = \frac{|V_2 - V_1|}{|I_2 - I_1|} \quad (1)$$

By using an IBIS editor **(**freeware available on the Internet–refer to Atmel Application Note: "AT91-AN02: Signal Integrity and AT91 Products (Basic Relationships between IBIS Data and your PCB)"**)**, it is possible to differentiate an output buffer by its signal name, such as "A0" for address 0, or according to the library where it stems from. Address [A0 to A22], Control and Data [D0 to D31] busses use the same buffer library, ASCCT33BDAUP. The following graph has been extracted from the AT91SAM9260 IBIS file regarding "Pullup" circuitry. Figure 2-1. "Current vs. Voltage on Pull-up Transistor of the ASCCT33BDAUP Pad" shows only the most linear section of the "Pullup" data and not the whole range of the Pull-up IBIS data.

Figure 2-1. Current vs. Voltage on Pull-up Transistor of the ASCCT33BDAUP Pad



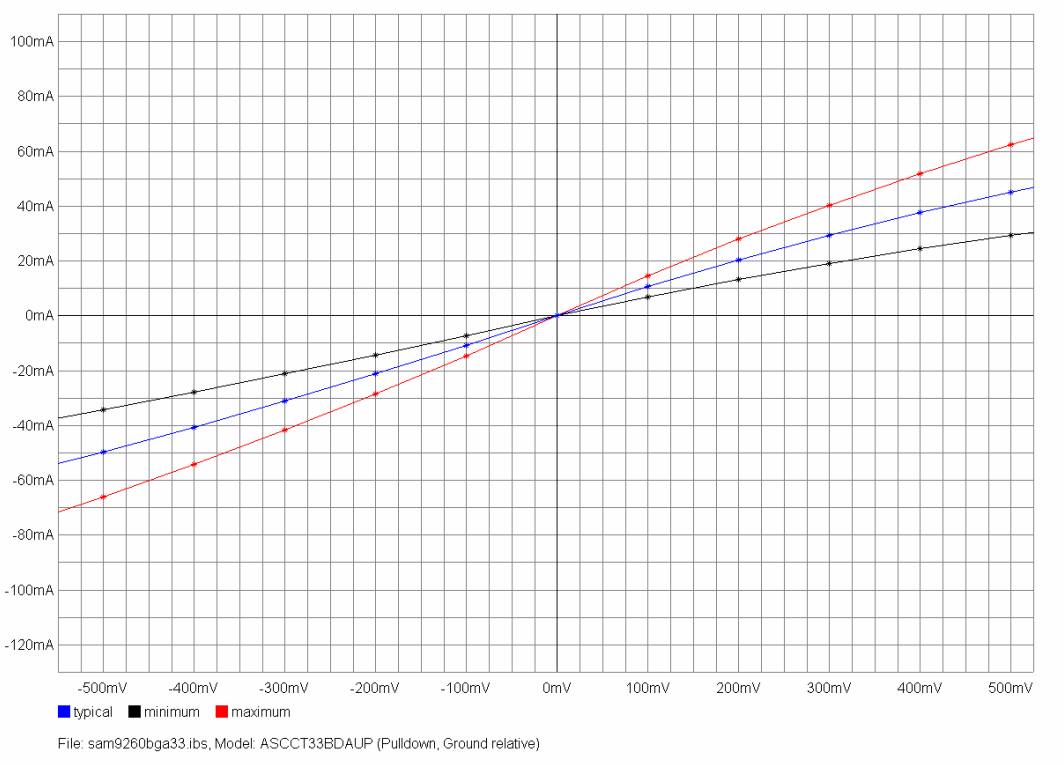
From the curve in Figure 2-1 and by using Equation "(1)", we can compute the three output impedances with three different processes: minimum, nominal and maximum.

Table 2-1. Intrinsic Impedance of the ASCCT33BDAUP Pull-up Circuitry

	Minimal	Nominal	Maximum
Pull-up transistor Z_{OH}	10 Ohms	14 Ohms	21 Ohms

Figure 2-2 shows pull-down behavior between the current and the output voltage.

Figure 2-2. Current vs. Voltage on Pull-down Transistor of the ASCCT33BDAUP Pad



From the curves in Figure 2-2 and by using Equation "(1)", we can compute the three output impedances with three different processes: minimum, nominal and maximum cases.

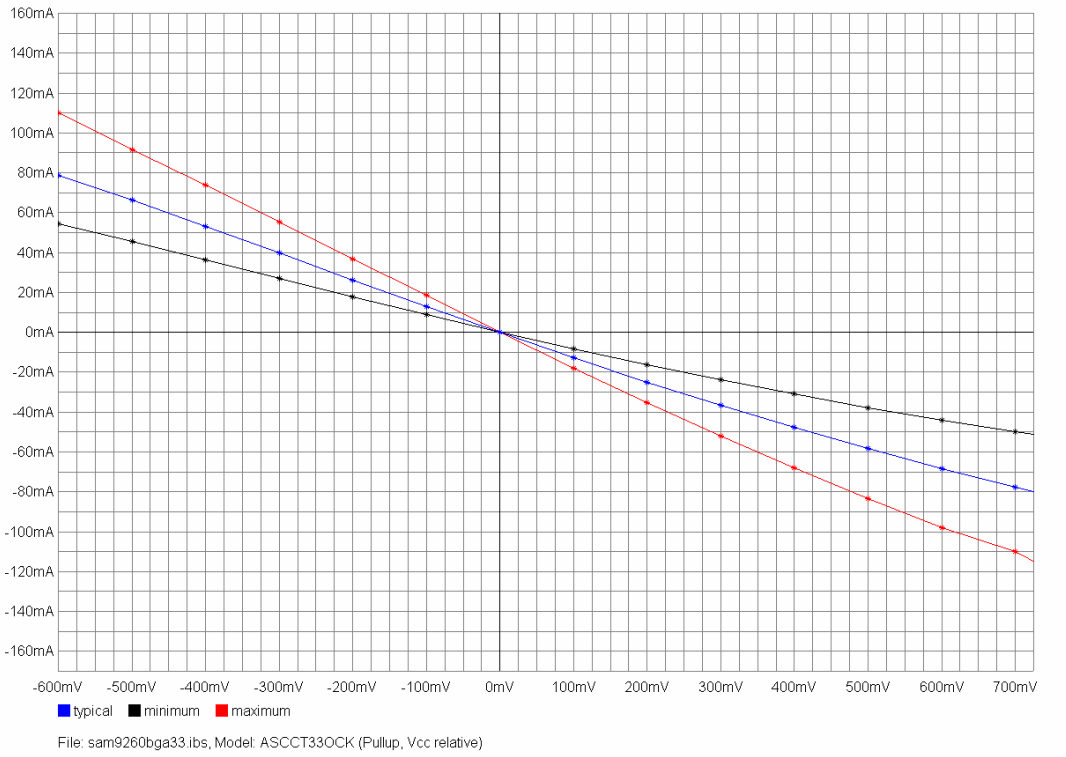
Table 2-2. Intrinsic Impedance of the ASCCT33BDAUP Pull-up Circuitry

	Minimal	Nominal	Maximum
Pull-up transistor Z_{OL}	7.5 Ohms	10 Ohms	15 Ohms

2.2 Output Buffer Impedance for the AT91 Clock Signal Output

Atmel uses the library to drive the SDRAM Clock signal only (called “sdck”). The following graph has been extracted from the AT91SAM9260_bsdl_ibis.zip software file, concerning “Pull-up” circuity. Figure 2-3 represents only the most linear section of the “Pull-up” data and not the whole range of the Pull-up IBIS data.

Figure 2-3. Current vs. Voltage on Pull-up Transistor of the ASCCT33OCK Pad



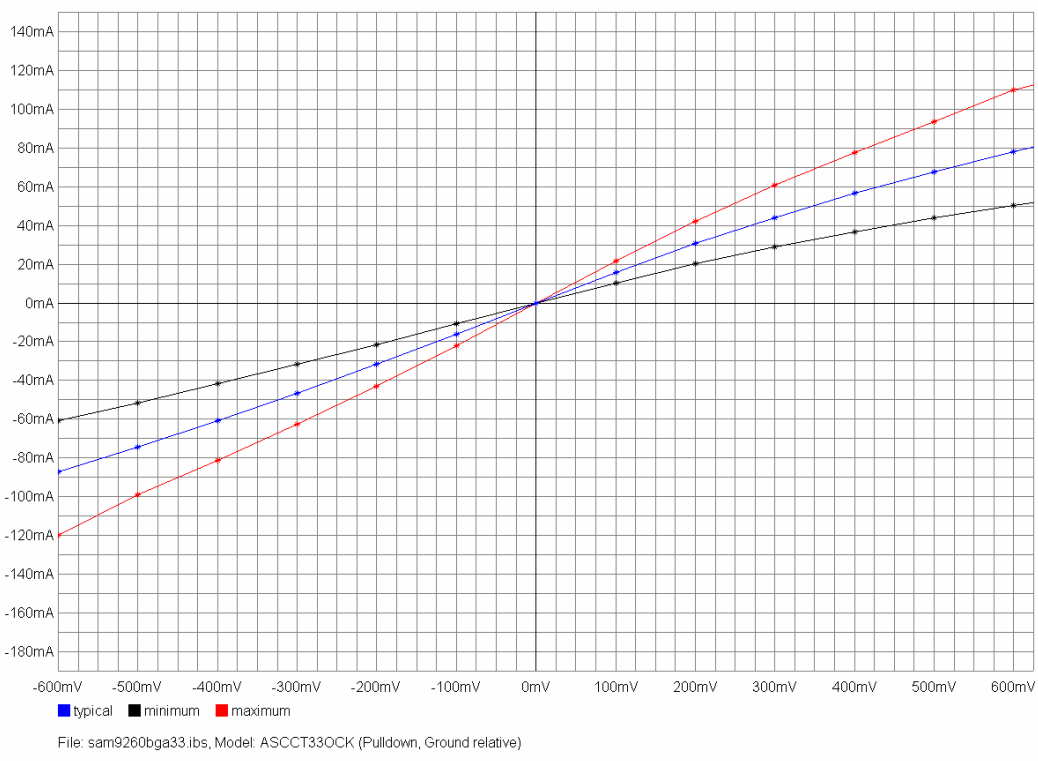
From the curves in Figure 2-3 and by using Equation “(1)”, we can compute the three output impedances with three different processes: minimum, nominal and maximum cases.

Table 2-3. Intrinsic Impedance of the ASCCT33OCK Pull-up Circuitry

	Minimal	Nominal	Maximum
Pull-up transistor Z_{OH}	5.8 Ohms	8.3 Ohms	12.5 Ohms

Figure 2-4 shows the “Pull-down” circuitry behavior between the current and the output voltage.

Figure 2-4. Current Curves vs. Voltage on Pull-down Transistor of the ASCCT33OCK Pad



From the curves in Figure 2-4 and by using Equation"(1)", we can compute the three output impedances with three different processes: minimum, nominal and maximum cases.

Table 2-4. Intrinsic Impedance of the ASCCT33OCK Pull-up Circuitry

	Minimal	**Nominal**	**Maximum**
Pull-up transistor Z_{OL}	5.2 Ohms	7 Ohms	10.5 Ohms

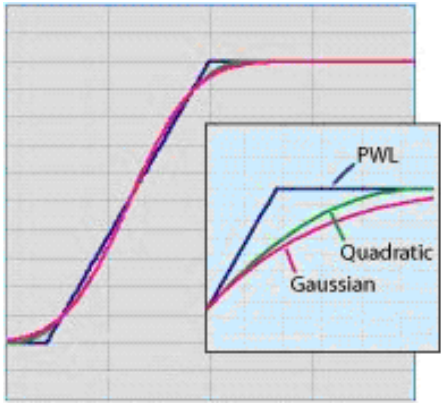
2.3 Extracting Data for Rising and Falling Time

As driver output impedances have been computed from the "Pullup" and "Pulldown" curves, using the same process, rise and fall times will be extracted by using the "Rising Waveform" and "Falling Waveform" IBIS curves. These graphs give the relationship between the output voltage vs. time. Three curves are used to describe the three possible process cases: **weak**, **nominal** and **fast**. It is important to remember that the effect of C_comp on dV/dt is already included.

The first task is to determine a shape as close as that of the end of the rising edge, or of the beginning of the falling edge, and theoretical linear, quadratic or Gaussian curve. According to this observation and edge slope delay, the second task is to deduce the F_{KNEE} frequency value. The edge spectral spreading being strongly dependent upon the edge shape, we are going to differentiate the output voltage behavior from among three theoretical shapes:

- Linear edge (represented as PWL in Figure 2-5)
- Double pole
- Gaussian edge

Figure 2-5. Linear, Double Pole and Gaussian Edge Superposition



By observing a voltage response vs. time, at driver output level (refer to Figure 2-6. "Rising Edge of the ASCCT33BDAUP Pad"), it appears that the signal shape resembles that of a Double Pole voltage response, rather than that of a PWL. It is not easy to determine the difference between a Gaussian and a Quadratic shape. To have a safety margin, we assume having a Quadratic behavior. In this condition, the rule of thumb is to approximate the cut-off frequency (F_{KNEE} frequency) for a digital signal by the following formula:

$$F_{KNEE} = \frac{K}{T_{RorF}} \quad (2)$$

Table 2-5 gives a quick look at the *K* factor value relative to the signal shape.

Table 2-5. K Factor vs. Edge Shape

Edge Shape	K Factor
Linear	0.5
Simple Pole	0.35
Double Pole	0.344
Gaussian	0.339

Then, in accordance with the curve shape given by the IBIS Model, Equation "(2)" becomes:

$$F_{KNEE} = \frac{0.344}{T_{RorF}} \quad (3)$$

2.4 Rising and Falling Time for Address, Data and Control Busses

The waveforms as shown in Figure 2-6. “Rising Edge of the ASCCT33BDAUP Pad” and Figure 2-7. “Falling Edge of the ASCCT33BDAUP Pad” give respectively, the rising and falling output shape of ASCCT33BDAUP Pad.

As recommended in the IBIS standard, buffer output simulations have been completed on an external 50 Ohms load resistor (“R_fixture” condition).

Figure 2-6. Rising Edge of the ASCCT33BDAUP Pad

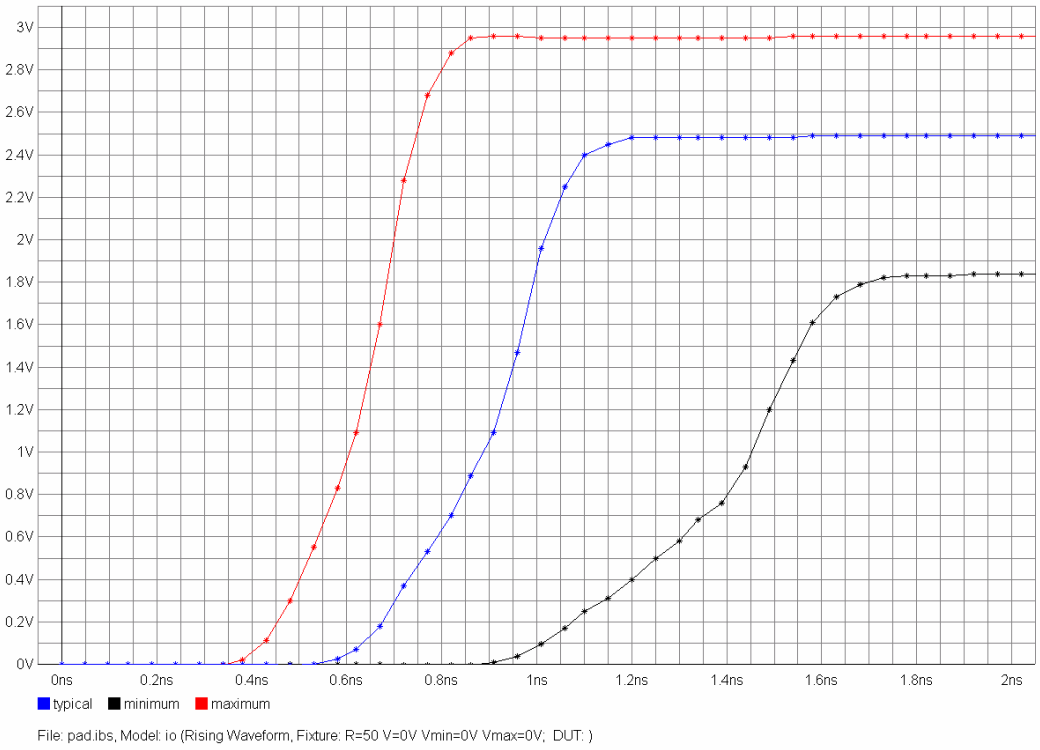
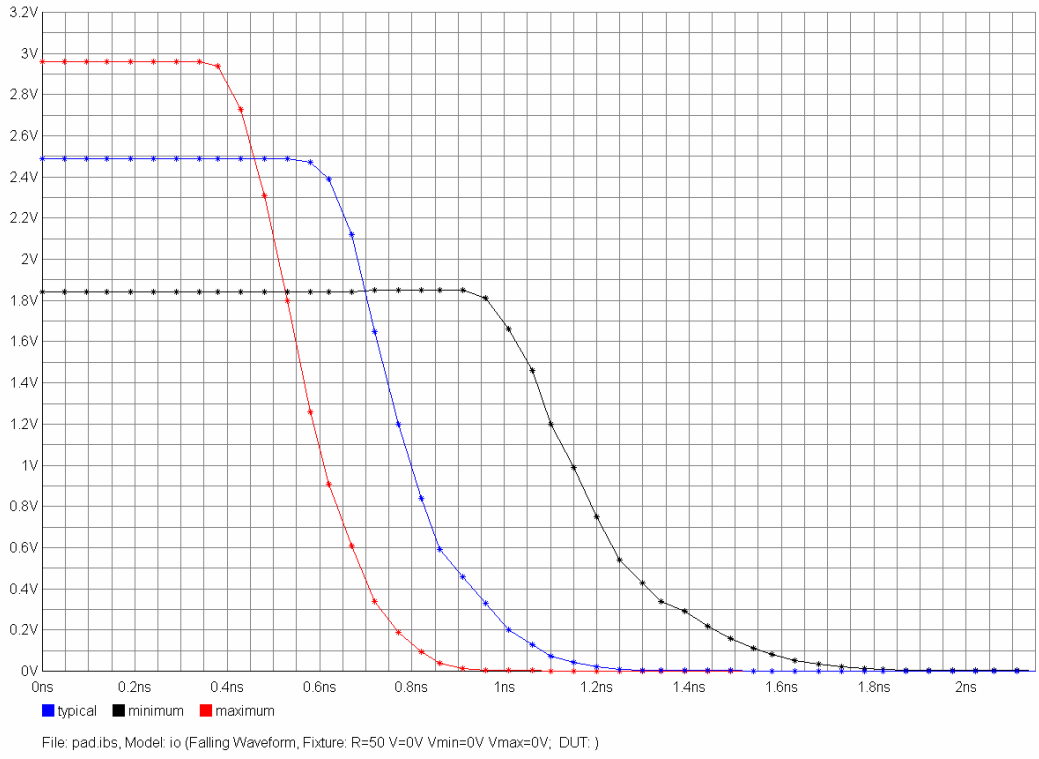


Figure 2-7. Falling Edge of the ASCCT33BDAUP Pad



- **Weak Process**

	Time Value at 10% (in ps)	Time Value at 90% (in ps)	$\lvert T_{90\%} - T_{10\%} \rvert$ Time (in ps)	F_{KNEE} (in MHz)
Rising Edge	1084	1592	508	677
Falling Edge	1522	1030	492	700

- **Nominal Process**

	Time Value at 10% (in ps)	Time Value at 90% (in ps)	$\lvert T_{90\%} - T_{10\%} \rvert$ Time (in ps)	F_{KNEE} (in MHz)
Rising Edge	686	1050	364	945
Falling Edge	1026	652	374	920

- **Fast Process**

	Time Value at 10% (in ps)	Time Value at 90% (in ps)	$\lvert T_{90\%} - T_{10\%} \rvert$ Time (in ps)	F_{KNEE} (in MHz)
Rising Edge	478	759	282	1200
Falling Edge	752	448	304	1130

2.5 Rising and Falling Time for the Clock Signal output to the SDRAM device

Below are simulation results which show the voltage curve vs. time on external 50 ohms load resistor but about the SDCK clock signal from the SDRAM Bus.

Figure 2-8. Rising edge of the ASCCT33OCK Pad

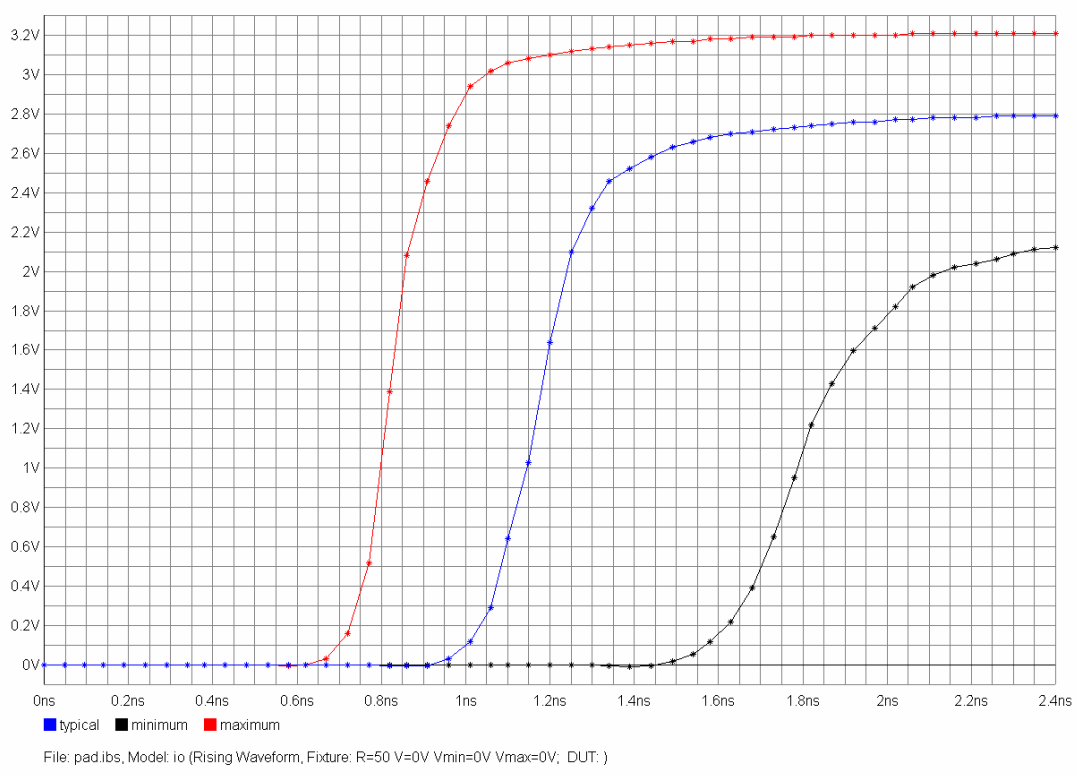
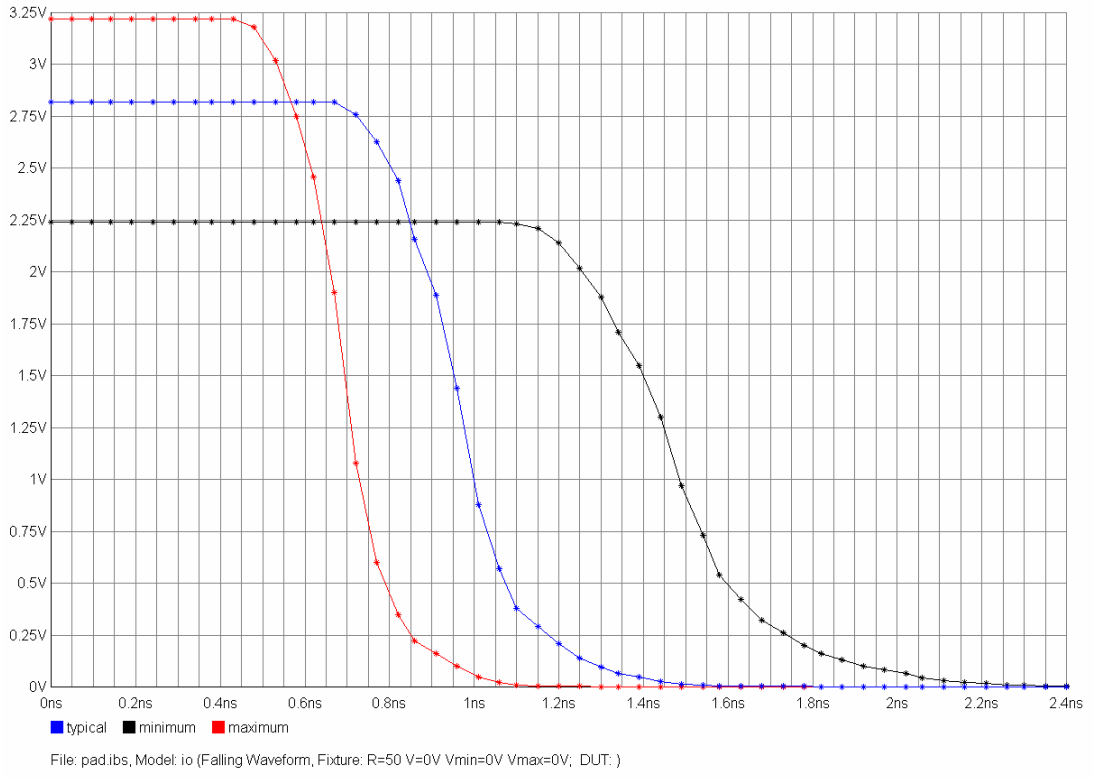


Figure 2-9. Falling edge of the ASCCT33OCK Pad



- **Weak Process**

	Time Value at 10% (in ps)	Time Value at 90% (in ps)	$\lvert T_{90\%} - T_{10\%} \rvert$ Time (in ps)	F_{KNEE} (in MHz)
Rising Edge	1629	2110	481	715
Falling Edge	1760	1250	510	674

- **Nominal Process**

	Time Value at 10% (in ps)	Time Value at 90% (in ps)	$\lvert T_{90\%} - T_{10\%} \rvert$ Time (in ps)	F_{KNEE} (in MHz)
Rising Edge	1056	1382	326	1050
Falling Edge	1154	793	361	952

- **Fast Process**

	Time Value at 10% (in ps)	Time Value at 90% (in ps)	$\lvert T_{90\%} - T_{10\%} \rvert$ Time (in ps)	F_{KNEE} (in MHz)
Rising Edge	741	997	256	1340
Falling Edge	829	552	277	1240

3. PCB Electrical Characteristics

Without getting deep into theory, with the evolution in AT91SAM process technology (to increase working frequency and to lower power consumption), aberrant effects, such as stray capacitance, inductance and resistance, have more and more impact on electrical integrity. It follows that a trace, considered in the past as a simple means of connection, now becomes a “filter”.

At this level, with the calculated buffer impedance and F_{KNEE} frequency data from the IBIS file, it is possible to set some rules to complete PCB in accordance with the required signal integrity of the application, especially when the timing constraints are severe, as around an SDRAM Controller.

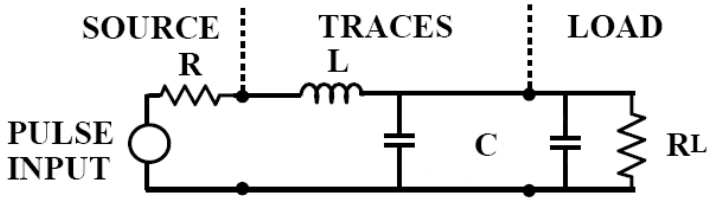
In the following paragraph, we deal with a point-to-point connection (from the driver to the load) without addressing the effect of the via or the change of layer.

3.1 Short Trace Length: a Localized System

The first subject to address is “localized circuitry”, i.e., when the trace length is short enough. We say “localized” when we are able to consider, at any time, that all trace points have the same voltage. Of course, in static mode it is always localized. But, during a rising or falling edge, with very short edge time, we can often observe some issues at signal level. Due to the trace length (reflection issue with long traces) or the stray inductance of the trace (second order response resulting from LC equivalent circuitry with short traces), the signal transmission on a “passive” element (as a trace should be) may become a problem source.

This first paragraph will treat short traces. In this condition, a trace can be considered as a second order system as shown in Figure 3-1:

Figure 3-1. Equivalent Circuitry of a Localized System



Notes:

Typical application loads being CMOS circuitry inputs, therefore $R_L >> 1/C$, both capacitances, the trace and the load circuitry, will be replaced by a called “*C* equivalent” punctual capacitance.

The *R* electrical parameter can be replaced by the previously extracted output impedance from IBIS Model file called: Z_{OL} or Z_{OH}.

The response of the RLC system is perfectly known. The ringing condition depends on a quality factor of the circuitry, i.e.:

$$Q = \frac{Z_0}{R} \quad (4)$$

Z_0 is called the characteristic impedance of the trace and it is defined by the following formula:

$$Z_0 = \sqrt{\frac{L}{C}} \quad (5)$$

In general, the value of Z_0 is from around 50 Ohms up to 100 Ohms. These are optimal conditions (a high Q factor with LC circuitry) to find ringing on a trace.

As seen previously, the R impedance has a value from 5 Ohms up to 15 Ohms in this case.

For example, by replacing Z_0 by 50 Ohms (with, for example, a Z_0 = 50 Ohms characteristic impedance and an output impedance equal to 10 Ohms), in Equation " (4)", the quality factor will be around 5. It is too high and we have to expect ringing after each transient event.

- A reminder on damped second order system:

  The quality factor of a damped second ordering system as defined in this Application Note, i.e., on approximated RLC second order system, is given in the formula below:

$$Q = \frac{Z_0}{R} \text{ or } = \frac{1}{R}\sqrt{\frac{L}{C}}$$

  Two parameters are usually used to classify the damping of a second order system, the Q quality factor stated above and the damping ζ factor as seen below.

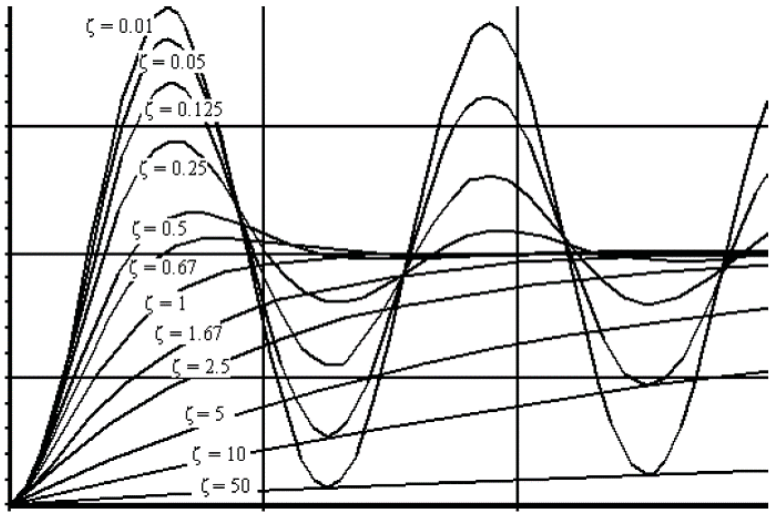
$$\zeta = \frac{R}{2}\sqrt{\frac{C}{L}} \quad \text{or} \quad Q = \frac{1}{R}\sqrt{\frac{L}{C}}$$

  – When $(\zeta > 1) Q < 0.5$ then the system is over damped.

  – When $(\zeta < 0.5) Q > 1$ then the system is under damped.

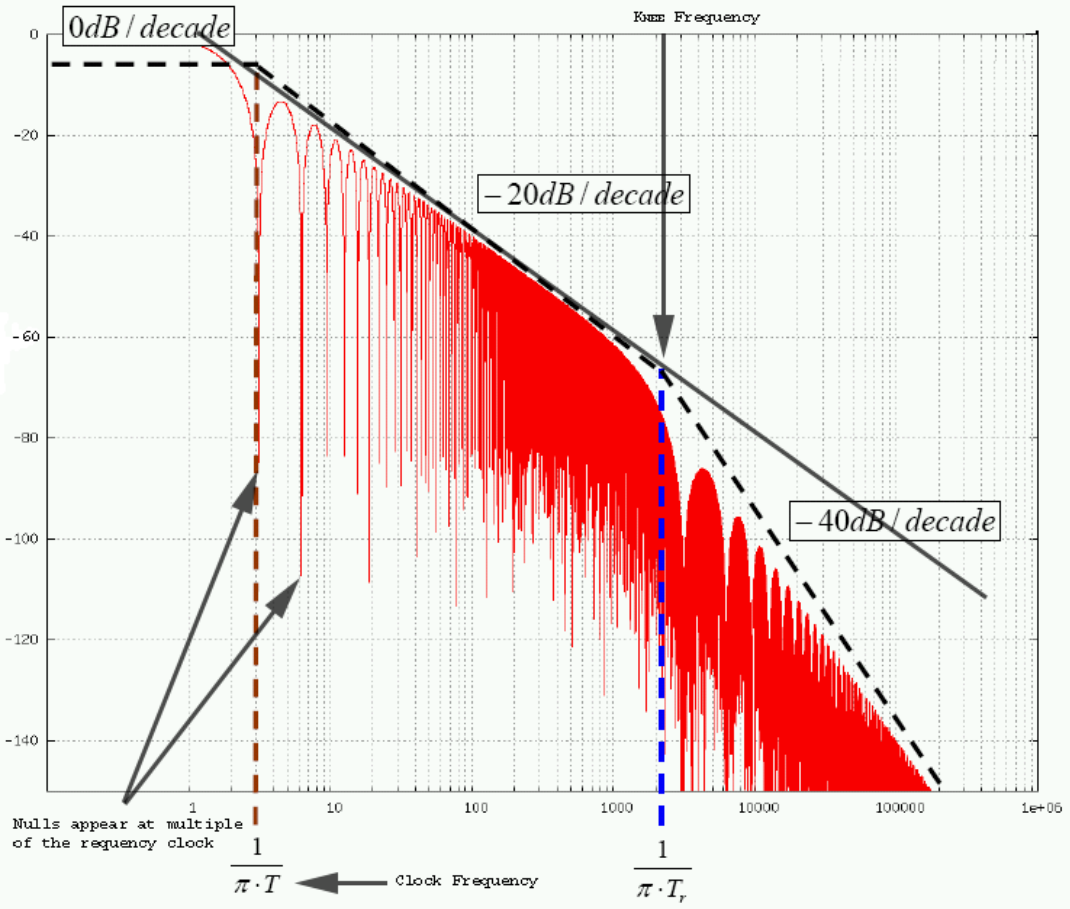
  A correct setting can be considered as a trace with a Q value between 0.5 and 1 or a ζ value from 1 down to 0.5.

Figure 3-2. Impact of Damping Factor on Step Response Behavior



Both values, *L* and *C,* allow us to compute the ringing frequency value (the natural frequency of the second order system). With this, and the spectral spreading of the edge, (through the previously calculated F_{KNEE} frequency for each buffer library), we can assume where the resonance frequency of the trace is in relation to the spectral spreading of the edge. Figure 3-3 shows an example of spectral breakdown according to the clock and F_{KNEE} frequencies. From the clock frequency to the F_{KNEE} frequency, slope of -20 dB / decade can be observed; after this point, the energy can be disregarded.

Figure 3-3. Clock Frequency, F_{KNEE} and Slope Spectral Spreading



To avoid ringing behavior, the goal is to reduce the *Q* factor on those short traces. The use of a termination resistor, close to the output driver, i.e. close to the AT91 device, will allow us to decrease the quality factor and to obtain a “quiet” behavior with a damped second order response. A high resistor value should not be added because adding this resistor deteriorates edge time of course, but be certain to be in compliance with the setup and hold times between AT91 and the SDRAM Memory device. This is a reason why resistor values are often selected from 10 to 33 Ohms.

The second and favorable effect of the termination resistor is to reduce the spike current on IO power supply pins. The Simultaneous Switching Output of 32 bits, due to the data bus activity, is the major source of IO power supply noise and ground bounce. The current control, through the serial resistor, reduces this phenomenon. This point is further developed when discussing the IO Power Supply bypass method.

3.2 Propagation Time, Characteristic Impedance: Distributed System

As seen, by comparing the buffer output impedance value (5 Ohms up to 10 Ohms, approximately) and the typical characteristic impedance (50 Ohms up to 100 Ohms), adding a termination resistor can be anticipated, thereby reducing the *Q* quality factor in a localized system. In addition, this method facilitates the current drive control on each IO and decreases the needs on the bypass capacitor in terms of qualitative performance.

Next, we consider a significant trace size in comparison with the rising or falling time.

Note:
In order to obtain the relationship between edge time and trace length, refer to the Atmel Application Note: "AT91-AN02: Signal Integrity and AT91 Products (Basic Relationships between IBIS Data and your PCB)".

In case the trace length is too long, we have to take into account the impedance homogeneity from the driver to the load(s). The trace cannot be compared to a simple second order system. It is not enough to add a termination serial resistor to reduce a *Q* factor without paying attention to the trace impedance (Z_0). In this case, the IBIS Model helps to match the driver output to the transmission line where the goal is to have:

$$Z_0 = R + R_S \quad (6)$$

Where:

- Z_0 is the line characteristic impedance of the trace
- R is the driver output impedance (called Z_{OH} or Z_{OL} in Section 2.1 "Output Buffer Impedance for Address, Data and Control Busses" on page 6)
- R_S is the needed termination resistor

Refer to the Atmel Application Note: "AT91-AN02: Signal Integrity and AT91 Products (Basic Relationships between IBIS Data and your PCB)" in order to obtain relationships between Z_0, R and R_S. This document provides the method to calculate the most closely adapted serial resistor value:

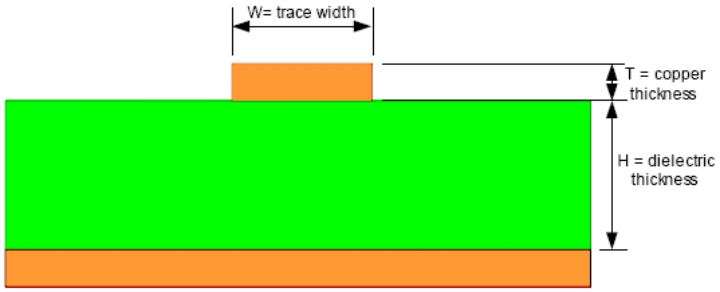
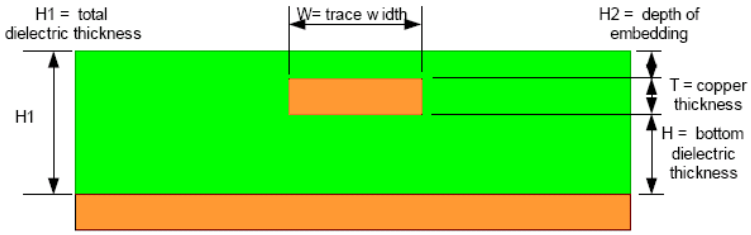
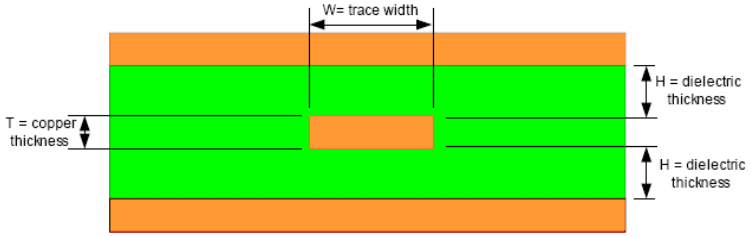
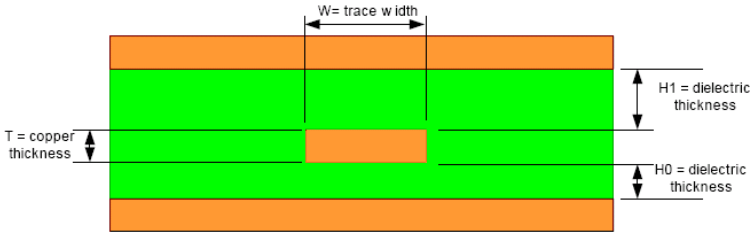
$$R_S = R - Z_0 \quad (7)$$

Without knowing Z_0, it is not possible to give the R_S resistor value.

3.3 Reminder: Characteristic Impedance of a Trace

The Z_0 impedance does not depend on the trace length, but on the geometrical characteristics, the position in terms of layout of the trace, and the nature of the PCB (dielectric constant of the material). Below are some formulas to calculate the Z_0 electrical parameter. With ε_r being the dielectric constant of the board material (FR4, Bakelite,…), in Napierian logarithms.

Table 3-1. Relationship between the Z0 Characteristic Impedance and the Trace Geometry

Geometric Designation	Figure (Corresponding Z_0 values are shown below)	Z_0 Values
Microstrip		$Z_0(W,H,T,\varepsilon_r) := \frac{87}{\sqrt{1.41+\varepsilon_r}} \cdot \ln\left(\frac{5.98 H}{T + 0.8 W}\right)$
Embedded Microstrip		$Z_0(W,H,H1,T,\varepsilon_r) := \frac{60}{\sqrt{\varepsilon_r}\left(1-\exp\left(-1.55\frac{H1}{H}\right)\right)} \cdot \ln\left(\frac{5.98 H}{T + 0.8 W}\right)$
Symmetric Stripline		$Z_0(W,H,T,\varepsilon_r) := \frac{60}{\sqrt{\varepsilon_r}} \cdot \ln\left[1.9\frac{(2 H + T)}{(0.8 W + T)}\right]$
Asymmetric Stripline		$Z_0(W,H_1,H_0,T,\varepsilon_r) := \frac{80}{\sqrt{\varepsilon_r}} \cdot \ln\left[1.9\frac{(2 H_0 + T)}{(0.8 W + T)}\right] \cdot \left(1 - \frac{H_0}{4 H_1}\right)$

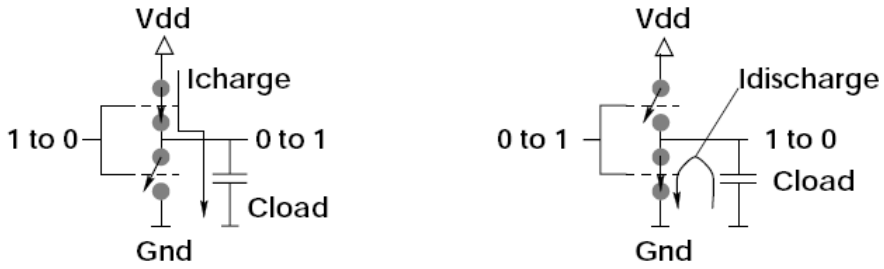
4. Power Supply Bypass

4.1 Quick Reminder on Dynamic CMOS Current Consumption

In static mode, the CMOS logic does not consume (leakage current can be neglected). The current consumption appears only during clock transitions. As shown in Figure 4-2. “Short Circuit Current in a Static CMOS Inverter”, it is easy to understand that dynamic power consumption becomes a constraint when:

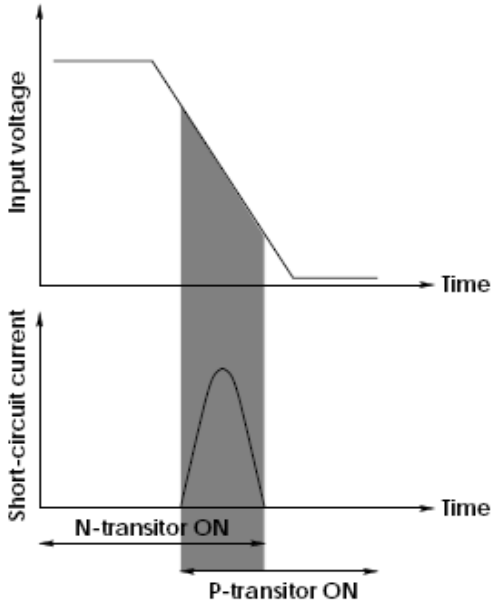
- Rising and falling times are very small (increasing of di/dt value)
- Simultaneous switching of *n* Input/Output appears in the application (*n.[di/dt]* at the same time)

Figure 4-1. CMOS Dynamic Current Consumption



There is another current consumption in CMOS digital logic that increases this phenomenon at clock transition. This is the short-circuit current when the elementary gate is switching high-to-low level or inversely. For a very short delay (when transistors are switching) N-transistor and P-transistor are in short circuit as shown below.

Figure 4-2. Short Circuit Current in a Static CMOS Inverter



At first, we are compelled to recall that reducing the VDD and GND noise can be achieved by designing these power systems through planes rather than in simple traces. This PCB design rule decreases intrinsic trace resistor ESR.

Generally speaking, the second effect of using the ground plane is to reduce ESL. The loop area of the current flowing (from a data bus line, for example) becomes a space between data trace and return (GND plane). The trace-inductance relationship is related to the area between the drive current on a data trace and its return (GND plane). For boards with power and return planes, the remaining inductance is caused by the capacitor body, solder pads, microstrip traces, and vias that connect the capacitors to the planes.

Then, in order to remove these stray trace effects on the power supply system, the addition of bypass capacitors (close to each VDD and GND pin) increases the noise reduction. By applying a bypass capacitor, current surges are restricted to a local loop between the bypass capacitor and the device powers pins. But, to guarantee this function, the bypass capacitor must have good characteristics at high frequencies. (The importance of placement and routing is not discussed here). Using “bypass capacitance” is to bypass stray parameters such as ESL of power supply traces. But, if we use bypass capacitors with significant intrinsic ESL at working frequency, the needed result will not be achieved. Throughout the following bypass study, it is assumed that all necessary energy, during switching events (from 0 to 1), will be provided through the bypass capacitor and not through the power supply system. This is the safest condition.

The graphs shown in Figure 4-3 and Figure 4-4 give information concerning the optimal working domain relative to the capacitance series (in terms of capacitance value) and dielectric material.

Figure 4-3. Ceramic Capacitor Behavior vs. the Working Frequency Domain

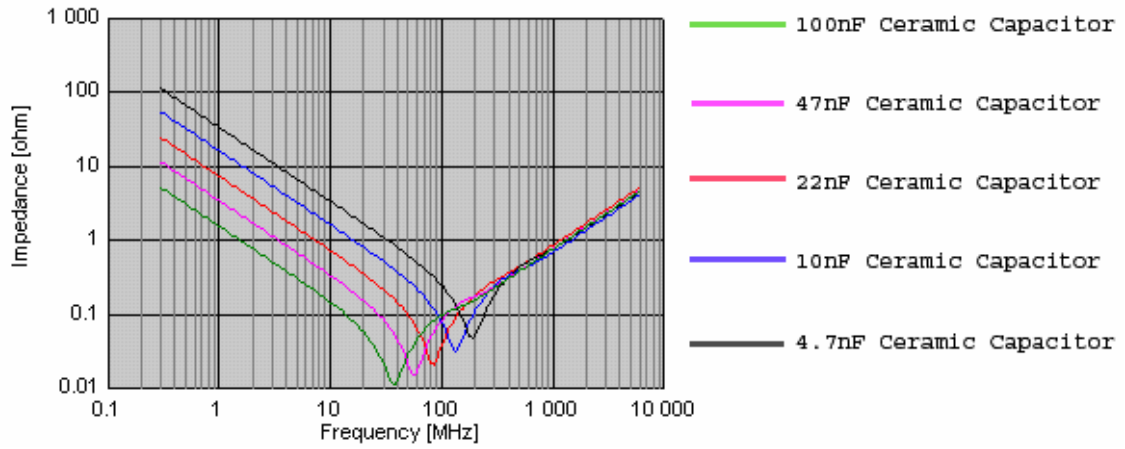
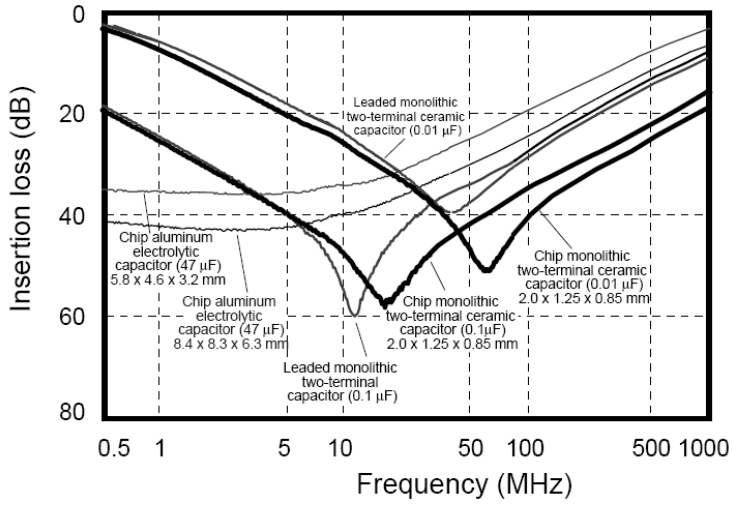


Figure 4-4. Capacitor Response vs. Frequency, Technology, and Value



4.2 Main Bypass Capacitance Value on Core Rail

All through this paragraph, we speak about digital power supply rails (the noise sources) and not about analogical power supply.

At first, the value of the main bypass capacitance must be evaluated as described below:

- Specify the allowed maximum voltage ripple on VDD (core and IO) during the worst transient event
- Know the transient duration
- Predict the current consumption

Then, we have to evaluate the qualitative needs of this capacitor according to the frequency behavior.

To define the bypass capacitance, compile the peak current (I_{MAX}), the delay while there is a current consumption (Δt) and the maximum ripple voltage (ΔV_{DD}) parameters into Equation "(8)":

$$C = \frac{\Delta t}{\Delta V_{DD}} . I_{MAX} \quad (8)$$

For the core rail, the electrical characteristics section of the AT91SAM9260 datasheet gives numbers for some conditions. In this example, I_{MAX} is the current consumption when the device is in "Active" mode (the ARM Processor is running with all peripherals being clocked at maximum frequency). This value is given with nominal rather than worst conditions. It is necessary to predict a current consumption a bit higher than this number, in order to assure a safety margin: 50% I_{MAX} of the current.

To evaluate Δt, understand that the current consumption is not restricted to a spike but to a "current consumption span" after the rising edge. The core consumption is the sum of elementary consumption spikes spread over time. There is no simple rule to deduce the consumption duration after a clock edge and the current consumption shape. An example of current consumption of a digital peripheral as shown in Figure 4-5. "Simplified Model of Digital Circuitry" is given in

Figure 4-6. “Current Consumption in Digital Peripheral”. This waveform is not extracted from an actual simulation but rather provides an idea of the current shapes.

Figure 4-5. Simplified Model of Digital Circuitry

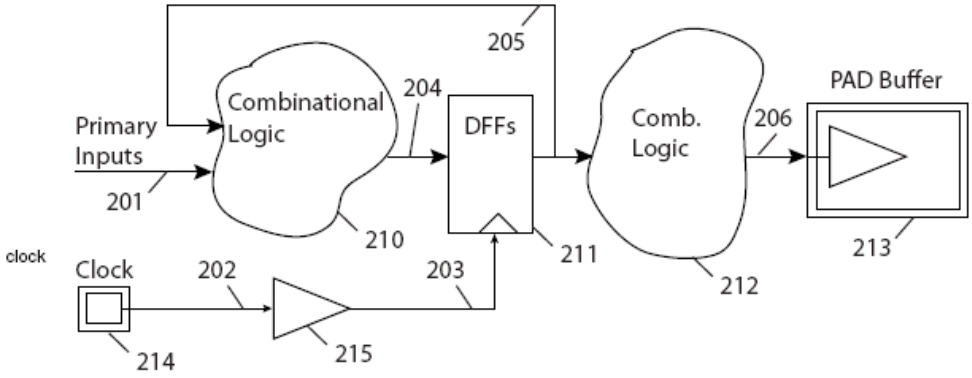
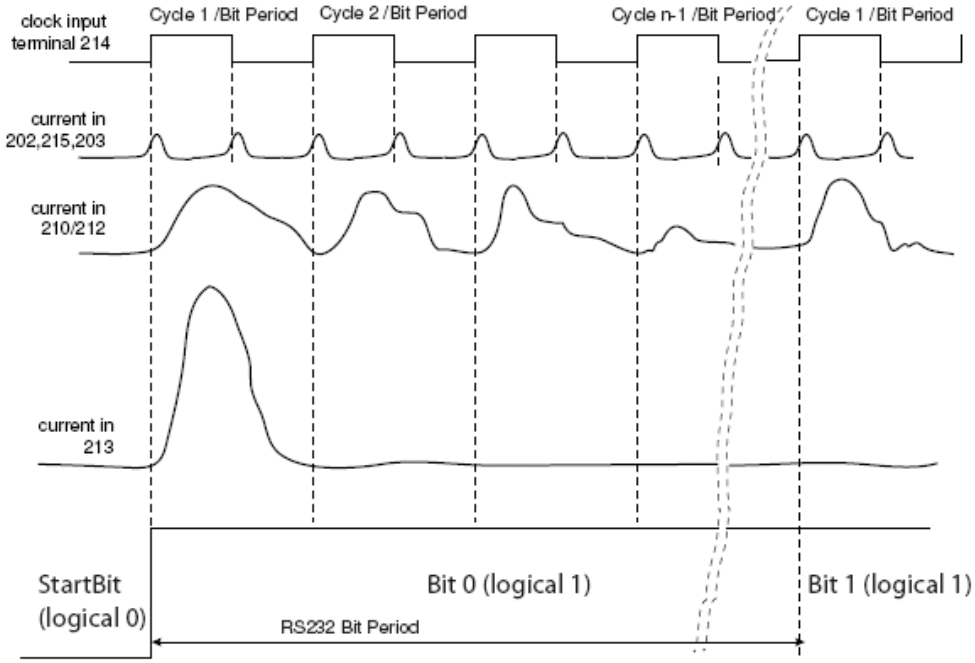


Figure 4-6. Current Consumption in Digital Peripheral



It is certain that the necessary current, for all internal state machines, will be completed during one clock period with a chip running at full speed. Of course, the maximum frequency for the peripherals (bus clock) is not always equal to the maximum frequency of the processor (processor clock in ARM9™ Based Microcontrollers), but we take the worst case into account for our study: the maximum consumption duration while the chip consumes the I_{MAX} current. This duration corresponds to one clock period of the maximum bus clock frequency.

Now, by using Equation "(8)" and replacing I_{MAX}, Δt and ΔV_{DD}, we can deduce the bypass capacitance.

Current Consumption I_{MAX} + 50% (in mA)	Minimum Bus Period Δt (in ns)	Maximum Allowed Ripple Voltage ΔV_{DD} (in mV)	Bypass Capacitance Value (in nF)
130 + 65 = 195	11	50	71.5

Now the first stage is completed, it remains to determine the quantitative value: the minimum capacitance value.

In the second stage, we have to select the capacitance value according to its effective response vs. the frequency working domain (Qualitative characteristic).

The maximum tolerated common-path impedance is R_{MAX} and is equal to:

$$R_{MAX} = \frac{\Delta V_{DD}}{\Delta I_{MAX}} \quad (9)$$

In the example, we obtain:

$$R_{MAX} = \frac{50mV}{195mV} \cong 0.25\Omega$$

If we apply this to the internal intrinsic impedance of the bypass capacitor, this maximum impedance gives the highest impedance limit over which the bypass capacitance will not be effective.

We want the system to work up to F_{KNEE}. Knowing the capacitor impedance due to its intrinsic inductance, ESL, we are going to calculate how much inductance can be tolerated at that high frequency:

$$L_{tot.capacitor} = \frac{R_{MAX}}{2\pi F_{KNEE}} = \frac{0.25}{2 \times \pi \times 100 \times 10^6} = 0.4nH$$

4.2.1 Note Concerning "Pseudo F_{KNEE} Frequency" on the Chip Core

Referring to Figure 4-6. "Current Consumption in Digital Peripheral", assume the shape of the current consumption increasing is completed around one half period of the highest clock frequency. The highest clock frequency, in this case, will be the processor clock frequency (and not the bus clock like previously).

Max. Allowed Impedance R_{MAX}	Min. Processor Period (in ns)	Pseudo F_{KNEE} (in MHz)	Number of VDDCORE Pins	Total Stray Intrinsic Inductance of Capacitor
0.25	5	$F_{KNEE} = \frac{0.5}{5ns} = 100$	4	0.4 nH

For example:

Using XR7 capacitor series, with a value equal to 22 nF, it is possible to predict an intrinsic equivalent serial inductance (ESL) equal to 0.13 nH for each capacitor. The result will be better, in terms of ESL, because the parallel capacitor network improves the resulting capacitance.

4.3 Main Bypass Capacitance Value for the SDRAM Power Supply Rail (VDDIOM): Quantitative Study

Compared to the study presented in Section 4.2 “Main Bypass Capacitance Value on Core Rail”, the maximum current consumption is not available in the AT91 product datasheet. This is an application dependent parameter. The method, in the first step, is to evaluate (by measurement, or estimation) the trace impedance and the external load per one IO. In the second step, to calculate the total bypass capacitance on the IO rail, we will assume the worst current consumption arises only when 32 output buffers switch simultaneously (SSO) from a low to a high level. The resulting drive current will be equal to 32 times that of one IO with the previously calculated load (trace plus the end load). In this condition, we only have to evaluate a minimum bypass capacitance value to drive the 32 distributed loading capacitances through each IO, without exceeding a maximum ripple voltage of more than a targeted limit (noise constraint).

We start the study by recalling Equation “(8)”:

$$C_{decoupling} = \frac{\Delta t}{\Delta V_{DD}}.I_{MAX}$$

The same equation can be used on the load side:

$$C_{TotalLoad} = \frac{\Delta t}{V_{DD}}.I_{MAX}$$

For both equations, I_{MAX} and Δt are equal and we can deduce the following relation:

$$C_{decoupling} = C_{TotalLoad}\frac{V_{DD}}{\Delta V_{DD}} \quad (10)$$

Where:

- V_{DD} is the maximum step between a low to a high logical voltage (3.3V for SDRAM Busses),
- ΔV_{DD} is the allowed voltage variation at the bypass capacitor level (50 mV are taken into account),
- $C_{TotalLoad}$ is the sum of all loads for all 32 Outputs

By replacing V_{DD} and ΔV_{DD} we obtain:

$$C_{decoupling} = C_{TotalLoad}\frac{3.3}{0.05} = 66.C_{TotalLoad}$$

The table below summarizes the bypass capacitance on VDDIOM

Table 4-1. Bypass Capacitance on VDDIOM

AT91 Parameters		Current Capability per IO (in mA)	F_{KNEE} Frequency[1] on Rising Edge (in MHz)	Capacitance Value per IO[2] (in pF)	Total Load Capacitance (in pF)	Needed Bypass Capacitance on VDDIOM (in nF)
Power Rail	Library					
VDDIO	ASCCT33BDAUP	32	945	25	32 x 25 = 800	0.8 x 66 = 53
VDDIO	ASCCT33OCK	1	1,050	25	1 x 25 = 25	0.025 x 66 = 1.7

Notes: 1. Refer to Section 2.3 “Extracting Data for Rising and Falling Time” on page 9, the nominal case.

2. Predicted value because it is an application dependent parameter. For example, a typical SDRAM signal input capacitance is around 7 pF and assumes about 18 pF for trace and stray capacitances.

4.4 Bypass Capacitance on SDRAM Power Supply Rail: Qualitative Study

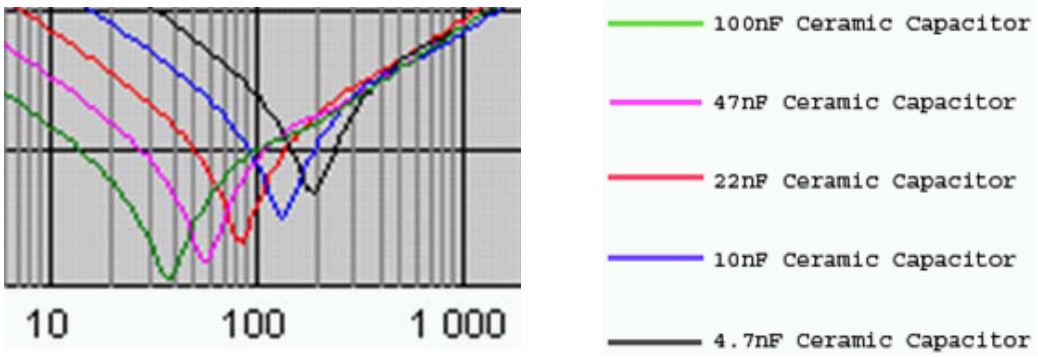
The objective of this paragraph is to select the necessary capacitors to overlap the necessary found bypass value (see Table 4-1) according to the frequency response of capacitors. As was shown on previous paragraph (see Figure 4-3. “Ceramic Capacitor Behavior vs. the Working Frequency Domain”), after a domain frequency, a capacitor is not a capacitance due to its ESL.

Without entering into all details, the main goal is to select capacitors with the characteristics that follow:

- The lowest intrinsic ESR and ESL
- Having the best response around the maximum bus frequency (around 100 MHz)

Referring to Figure 4-3. “Ceramic Capacitor Behavior vs. the Working Frequency Domain”, the 22 nF ceramic capacitor can be taken as an optimal working example. Its low ESL value allows a high working frequency domain up to the maximum internal bus clock.

Figure 4-7. Ceramic Capacitor Behavior Around the Resonance Frequency



A quick calculation gives the necessary minimum impedance that the supply distribution circuitry must not exceed under the following conditions:

- Keep the switching noise under 50 mV,

- Number of VDDIOM Pins, 3 for the BGA.
- Use the typical output impedance of the ASCCT33BDAUP buffer, 14 Ohms,
- 32 outputs as the worst simultaneous switching case

If we assume the drive current is limited only by the output impedance of the buffer, it is easy to deduce the maximum drive current:

$$I_{perIO} = \frac{V_{DD}}{Z_{OH}} = \frac{3.3}{14} = 0.23mA$$

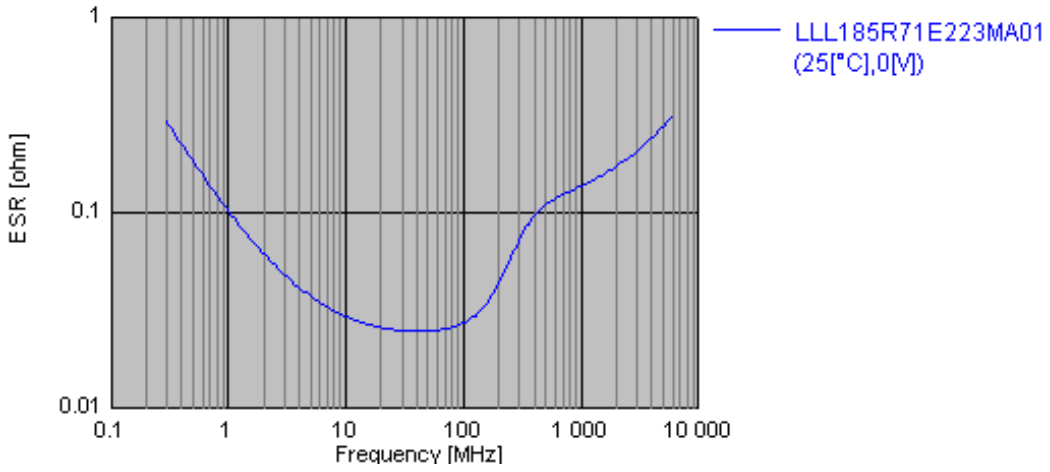
The 32 simultaneous buffer switching outputs are supplied through 3 power pins. There are 11 buffers per power pin. Therefore, the maximum drive per VDDIOM will be equal to 2.45 A.

With these conditions, the power circuitry must have a maximum impedance per VDDIOM pin equal to:

$$X_{MAX} = \frac{\Delta V_{DD}}{I_{MAX}} = \frac{50mV}{2.45} = 0.02\Omega$$

The following shows the ESR characteristics curve.

Figure 4-8. ESR Characteristics vs. Frequency



Using two 22 nF per VDDIOM pin seems to be a correct bypass network.

All previous computation results (from table in Section 4.2.1 on page 24 and Table 4-1 on page 26) can be summarized in Table 4-2.

Table 4-2. Bypass Capacitor on AT91SAM9260

Voltage Rail	Total Needed Bypass Capacitance	Number of VDD Pins	Number of 22 nF Bypass Capacitors per Pin
VDDCORE	71.5 nF	4	1
VDDIO	56.7 nF	3	2 due to ESR

4.5 Experimental Results on the AT91SAM9260-EK

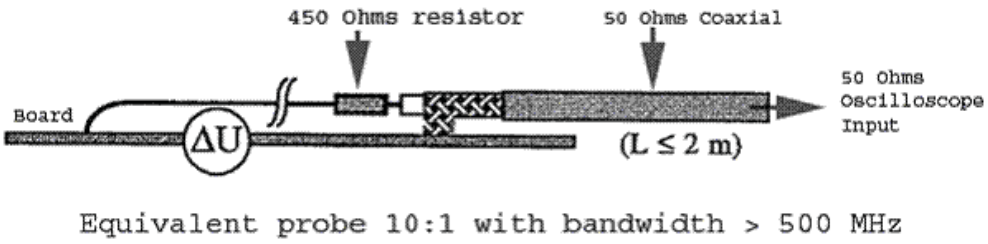
It is not realistic to only investigate Signal Integrity in theory, computing values of an AT91SAM specific product and writing a summary on this study, without results obtained in practice. For Atmel, this dual approach is crucial before concluding with the recommended design layout.

In order to make things more palpable on an experimental application, VDDCORE and VDDIOM paths have been degraded by adding a wire instead of power consumption jumpers. By adding a wire in the power supply path, ESL is increased. High frequency current cannot correctly supply AT91 microcontroller rails. Under these conditions, only bypass capacitors are capable of delivering high frequency current. Without resorting to this trick, it is not easy to demonstrate the bypass capacitor's efficiency.

We made measurements on both power supply rails with both configurations, i.e., with 100 nF standard Ceramic capacitors, and with specific 22 nF Ceramic capacitors. In both studies, we performed spectral analysis to compare the residual noise levels at Processor and Bus fundamental frequencies.

4.5.1 Measurement Conditions

Figure 4-9. Resistive Probe



Remark: Using this probe adds -20 dB to all measurement results. This factor is taken into account in Table 4-3, "Results of the VDDCORE Spectral Analysis," on page 29 and Table 4-5, "Results of the VDDIOM Spectral Analysis," on page 31.

VDDCORE and VDDIOM	Degraded power supply path with a 0.3 m flying wire
Processor Clock Frequency	198.65 MHz
Bus Clock Frequency	99.32 MHz
Processor Current Consumption	around 100 mA Includes the ARM926™ processor, internal caches, Linux® OS + the MP3 decoder application

4.5.2 VDDCORE Rail (100 nF/22 nF)

Spectral analysis on VDDCORE power rail as shown in Figure 4-10 represents VDDCORE with 100 nF decoupling capacitors for the upper screen capture and 22 nF decoupling capacitors for the one below it (color print in color blue).

Figure 4-10. Spectral Analysis on VDDCORE Power Rail (100 nF/22 nF)

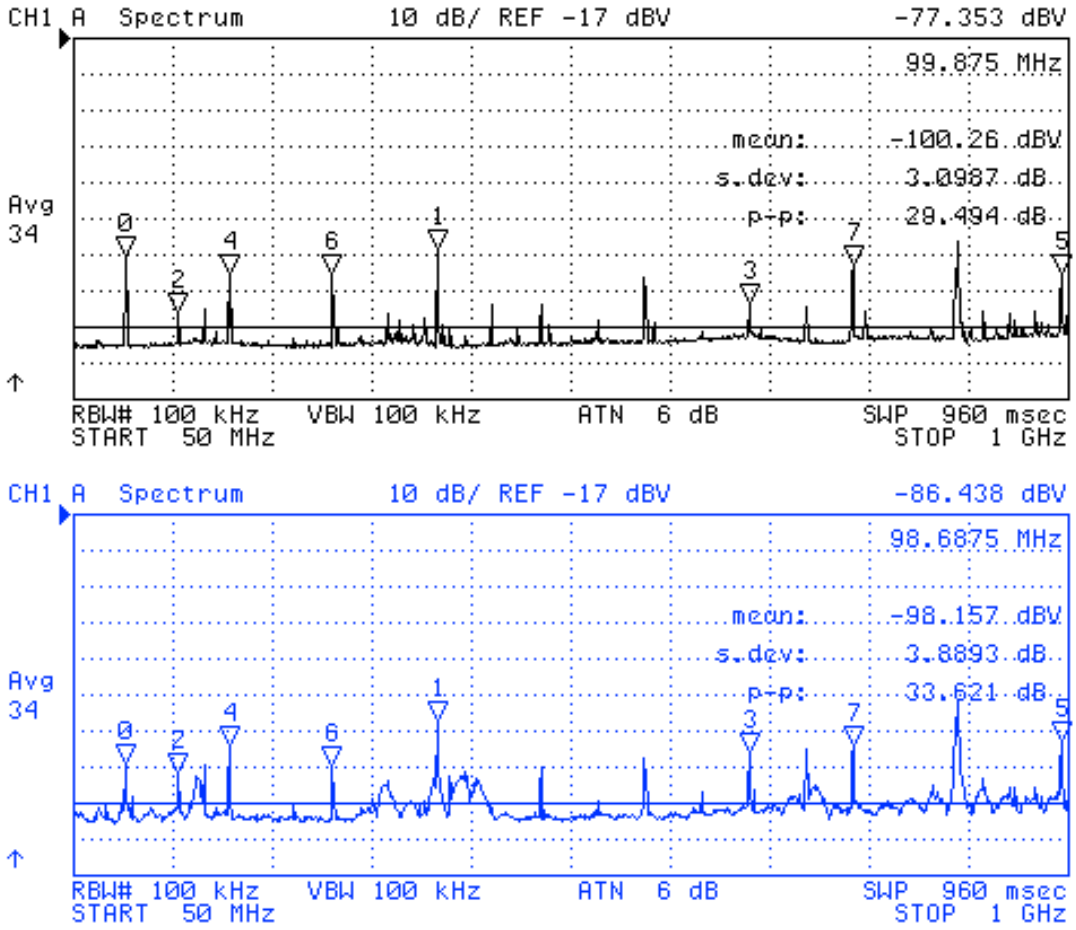


Table 4-3. Results of the VDDCORE Spectral Analysis

100 nF Capacitor			22 nF Capacitor		
Cursor ID	**Frequency (in MHz)**	**Level value (in dBV)**	**Cursor ID**	**Frequency (in MHz)**	**Level value (in dBV)**
0	99.87	-77	0	98.68	-86
2	149.75	-92	2	149.75	-91
4	198.43	-82	4	198.43	-81
6	297	-83	6	297	-87
1	396.75	-76	1	396.75	-75

Table 4-3. Results of the VDDCORE Spectral Analysis (Continued)

100 nF Capacitor			22 nF Capacitor		
Cursor ID	**Frequency (in MHz)**	**Level value (in dBV)**	**Cursor ID**	**Frequency (in MHz)**	**Level value (in dBV)**
3	694.81	-91	3	694.81	-83
7	794.56	-80	7	794.56	-81
5	992.87	-83	5	992.87	-80

A synthesis of the graphs shows that theory and practice confirm the stated predictions as presented up to this point. By comparing the theoretical capacitor response curves (see Figure 4-7. "Ceramic Capacitor Behavior Around the Resonance Frequency") with the 100 nF and 22 nF experimental spectral measurements, the conclusion is shown in Table 4-4:

Table 4-4. VDDCORE: Observation of Capacitor Frequency Response vs. Experimental Measurement

Frequency Domain	**Observation from the Theoretical Computation (refer to Figure 4-7)**	**Practical Measurements (refer to Figure 4-10)**
0 - 65 MHz	In low frequency, 100 nF capacitor has better behavior than 22 nF capacitor due to low ESR vs. 22 nF capacitor. Max. effect is around 40 MHz frequency.	No clock signal down to this frequency domain.
65 - 198 MHz	Around 65 MHz, 22 nF capacitor is more efficient than 100 nF capacitor. Hence, better effects on noise at bus frequency can be expected.	Around 98 MHz, up to 10 dBV voltage noise reduction by using 22 nF capacitor instead of 100 nF capacitor.
Over 200 MHz	In the upper frequency domain, 22 nF and 100 nF have the same behavior.	Experimental levels coincide with the theory.

4.5.3 VDDIOM Rail

Spectral analysis on VDDIOM power rail as shown in Figure 4-11 represents VDDIOM with 100 nF decoupling capacitors for the upper screen capture, and 2 x 22 nF decoupling capacitors for the one below (color print in color blue.)

Figure 4-11. Spectral Analysis on VDDIOM Power Rail (100 nF/2x22 nF)

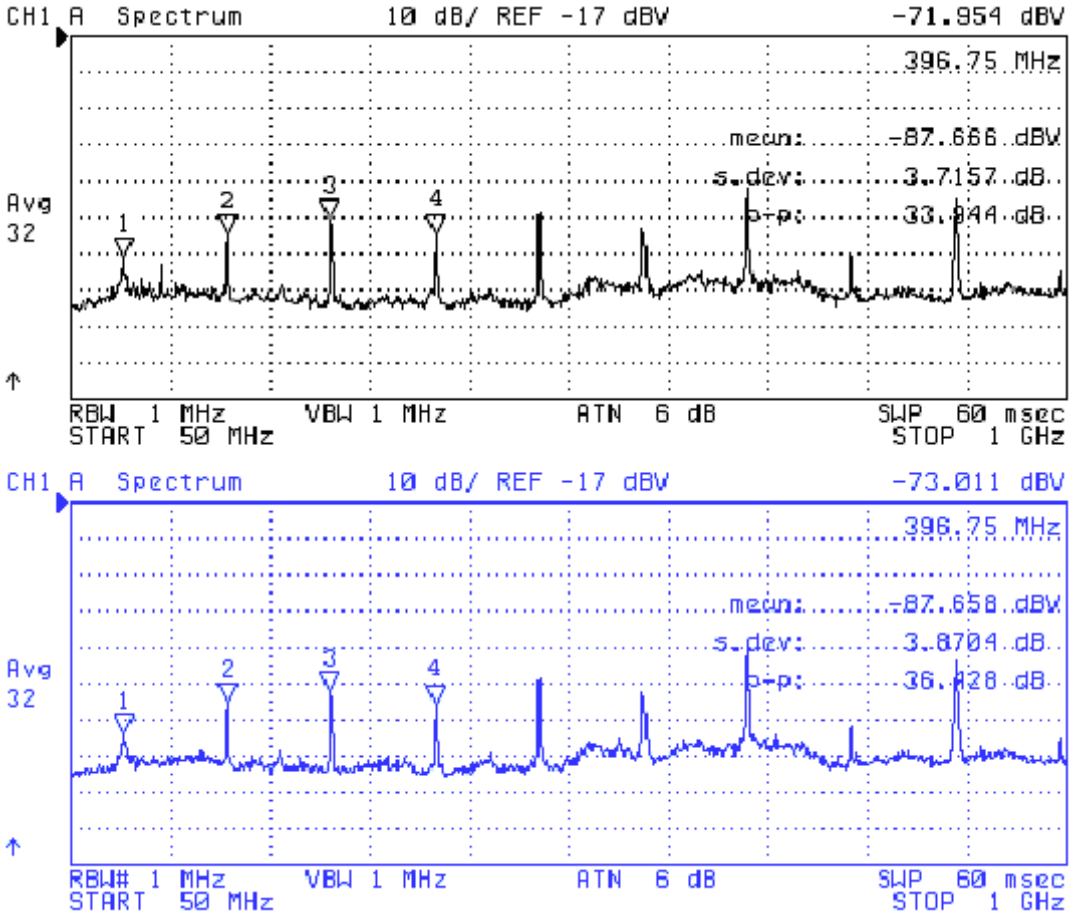


Table 4-5. Results of the VDDIOM Spectral Analysis

100 nF capacitor			2 x 22 nF capacitor		
Cursor ID	**Frequency (in MHz)**	**Level value (in dBV)**	**Cursor ID**	**Frequency (in MHz)**	**Level value (in dBV)**
1	98.68	-78	1	98.68	-82
2	198.43	-72	2	198.43	-73
3	297	-68	3	297	-70
4	396.75	-72	4	396.75	-73

By comparing the theoretical capacitor response curves (see Figure 4-7. “Ceramic Capacitor Behavior Around the Resonance Frequency”) with the 100 nF and 2 X 22 nF experimental spectral measurements, the conclusion reached is shown in Table 4-6 below:

Table 4-6. VDDIOM: Observation of Capacitor Frequency Response vs. Experimental Measurement

Frequency Domain	Observation from the Theoretic Curves (refer to Figure 4-7)	Practice Results (refer to Figure 4-11)
0 – 65 MHz	In low frequency, 100 nF capacitor has better behavior due to low ESR vs. 2 x 22 nF capacitor. Max. effect is around 40 MHz frequency.	No clock signal down to this frequency domain
65 – 198 MHz	Around 65 MHz, 2 x 22 nF capacitor is more effective than 100 nF capacitor. Hence, better effects on noise at Bus frequency can be expected.	Around 98 MHz, up to 4dBV voltage noise reduction by using 2 x 22 nF capacitor vs. 100 nF capacitor.
Over 200 MHz	In the upper frequency domain, 2 x 22 nF and 100 nF have the same behavior.	Experimental levels coincide with the theory.

4.6 Bypass Method

The majority of designs are made using 100 nF decoupling capacitors, which offer good signal Integrity results at working and qualitative levels. The quick study presented here has shown some differences concerning intrinsic capacitance parameters such as ESR and ESL, between 22 nF and 100 nF. But it is not so obvious: The lower ESR value about 100 nF vs. the 22 nF compensates its worse ESL value vs. the 22 nF.

In the next section, we present two designs using specific 22 nF capacitors subsequently in concordance with the previous study. These board projects are examples and have to be considered as an "absolute design rule" at bypass level. The use of power planes instead of power traces prevents us to be in a dilemma with the use of 100 nF or another value (like 22 nF). Customers will be able to plan the use of standard 100 nF capacitors without any problem.

Important things to remember about the choice of bypass capacitors and their use:

- in quantitative terms, a 100 nF capacitor per pin/ball is more than enough under 100MHz
- in qualitative terms, for higher frequency domains, the serial parasitic inductance of these bypass capacitors degrades the "bypass" function.

As a conclusion, the use of only one 100 nF per pin avoids having two 22 nF capacitors per pin, but the customer should be able to use a 100 nF / 22 nF capacitor couple to have better results.

5. From Theory to Practice: QFP and BGA Routing Examples

This section provides partial board designs about the SDRAM bus and their termination resistors by taking the AT91SAM9260 as an example. Regarding the bypassing capacitors, the design is not optimal because of power planes constraints. Accordingly, in BGA package, the bypassing method is more a plane bypassing than a power ball bypassing.

At the beginning of the project, we have to plan the stack-ups being used. The PCB layer stack-up and thickness are assigned to the manufacturer when the board is ordered and not during the routing Layout process. The PCB layer stack-up and thickness need to be defined early in the design stage before working in Layout, since the stack-up will determine how many layers to

enable and how many power and ground planes to establish. The strategy for stacking up a PCB depends on a number of things such as the capabilities of the board manufacturer, the circuit density (both routing and parts), the frequency (analogical) and rise/fall times (digital) of the signals, and the acceptable cost of the board.

By stacking combinations of various "core" thicknesses and sheets of "prepreg", a wide variety of finished board thicknesses can be achieved as shown in Figure 5-1:

Table 5-1. Typical Finished Standard Board Thicknesses

Mils	Millimeters
20	0.51
30	0.76
40	1.02
62	1.6
93	2.4
125	3.2
250	6.4
500	12.7

As described in Section 2.1 “Output Buffer Impedance for Address, Data and Control Busses” on page 6 or in “AT91-AN02: Signal Integrity and AT91 Products (Basic Relationships between IBIS Data and your PCB)”, nearly every detail of a board's stack-up affects two key characteristics of the trace segments on a board:

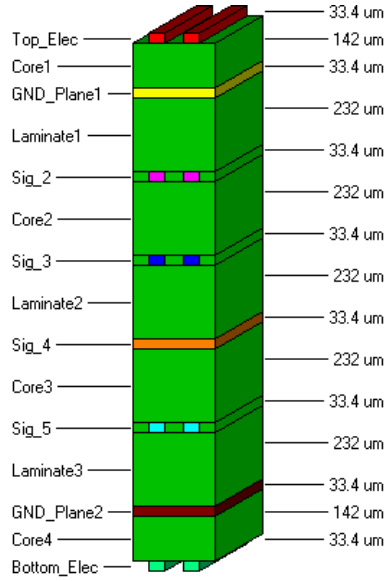
- Characteristic impedance (Z0)
- Propagation velocity

Together, these parameters determine how signals interact with and propagate along the board traces.

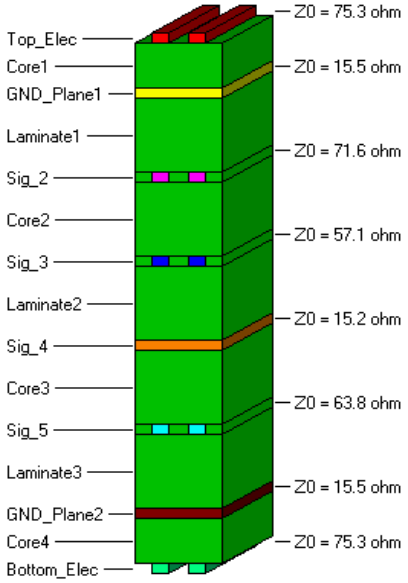
For our projects, we use the PCB stack-ups shown below. The total board thickness is approximately equal to 1700 µm but this choice is just one solution example.

Table 5-2. Board Stack-up for AT91SAM9260 LQFP (a) and (b), and BGA (c) and (d)

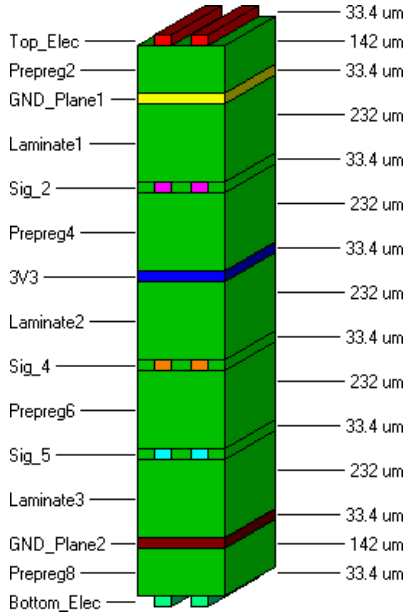
(a)



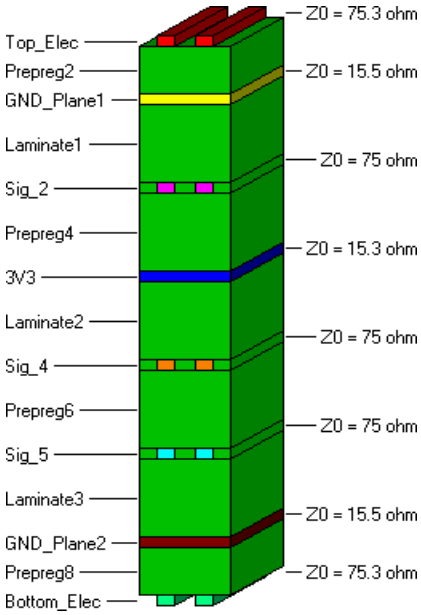
(b)



(c)



(d)



A second technical common point between both projects is the bypassing capacitors and the termination network resistors being used.

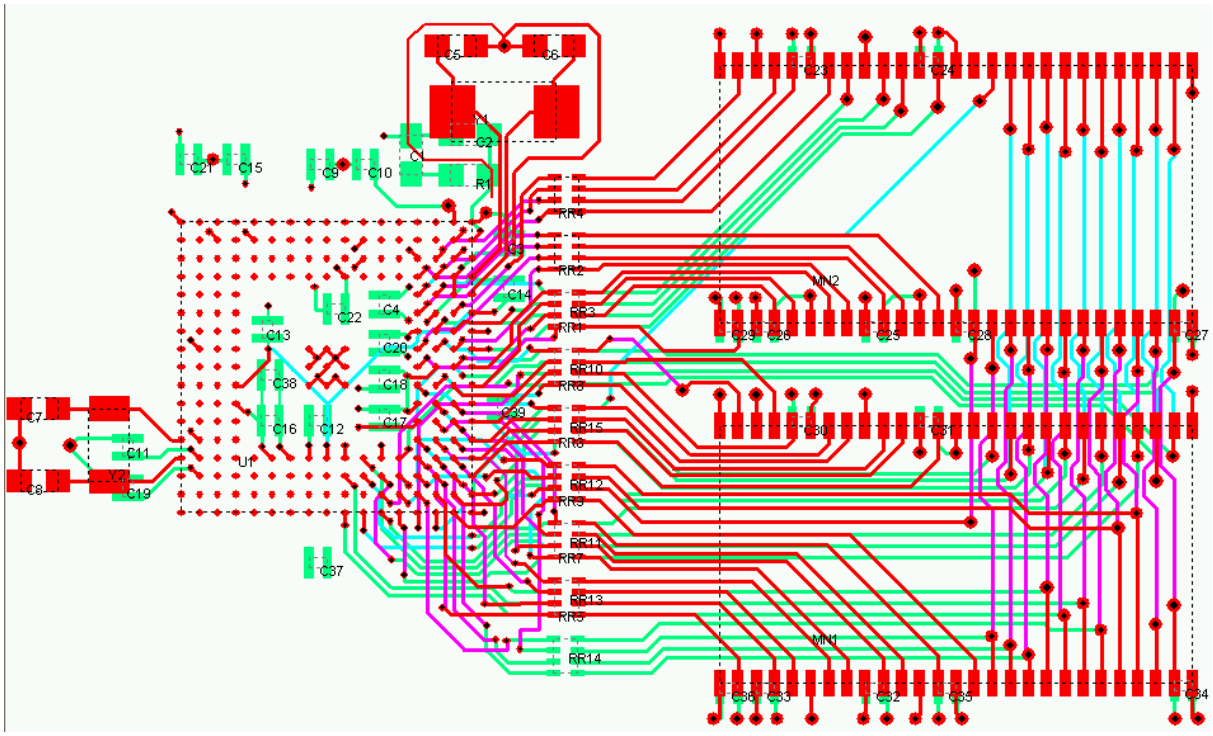
Bypassing capacitor component references: On VDDCORE and VDDIOM pins, we plan to use LLL185R71E223MA01 capacitors from Murata, for example. This is the optimal choice but it is not mandatory.

Termination network resistors references: Bourns Resistor Network CAT10-J series (http://www.bourns.com), 4 isolated resistors in a 0804 size package to minimize the PCB being used.

Note: In the BGA design example, some bypassing capacitors are not well positioned. The ball density constraints prevent from having capacitors close to the targeted power balls, as the power supply is provided through local power plans instead of traces. For this reason, the bypassing capacitors are connected to GND through a via on one side, and to the local power plan on the other side; it is acceptable to have a capacitor number greater than the power ball number.

5.1 AT91SAM9260, AT91SAM9G20 in BGA Package: Typical PCB Design

Figure 5-1. AT91SAM9260 (or AT91SAM9G20, AT91SAM9XE) Optimal Board Design



In this design example, the trace lengths, the necessary PCB surface, and the signal Integrity at SDRAM bus signals level have been optimized.

Extracted from "HyperLynx® BoardSim" V7.7 by Mentor Graphics®, the following trace data gives the propagation delay, the physical length, and the effective net impedance according to the stack-up choice and trace geometry.

Table 5-3. Statistics for the Longest Net (A7)

Selected-net name	A7
Total copper delay of all segments	0.3783 ns
Total length of all segments	6.101 cm
Number of segments	24
Number of vias	4
Minimum segment Z0	53.1 ohms
Maximum segment Z0	64.6 ohms
Total receiver capacitance	6.580 pF
Total segment resistance	0.210 ohms
Effective net Z0	45.6 ohms

Figure 5-2. Electrical Behavior on A7 Signal Trace

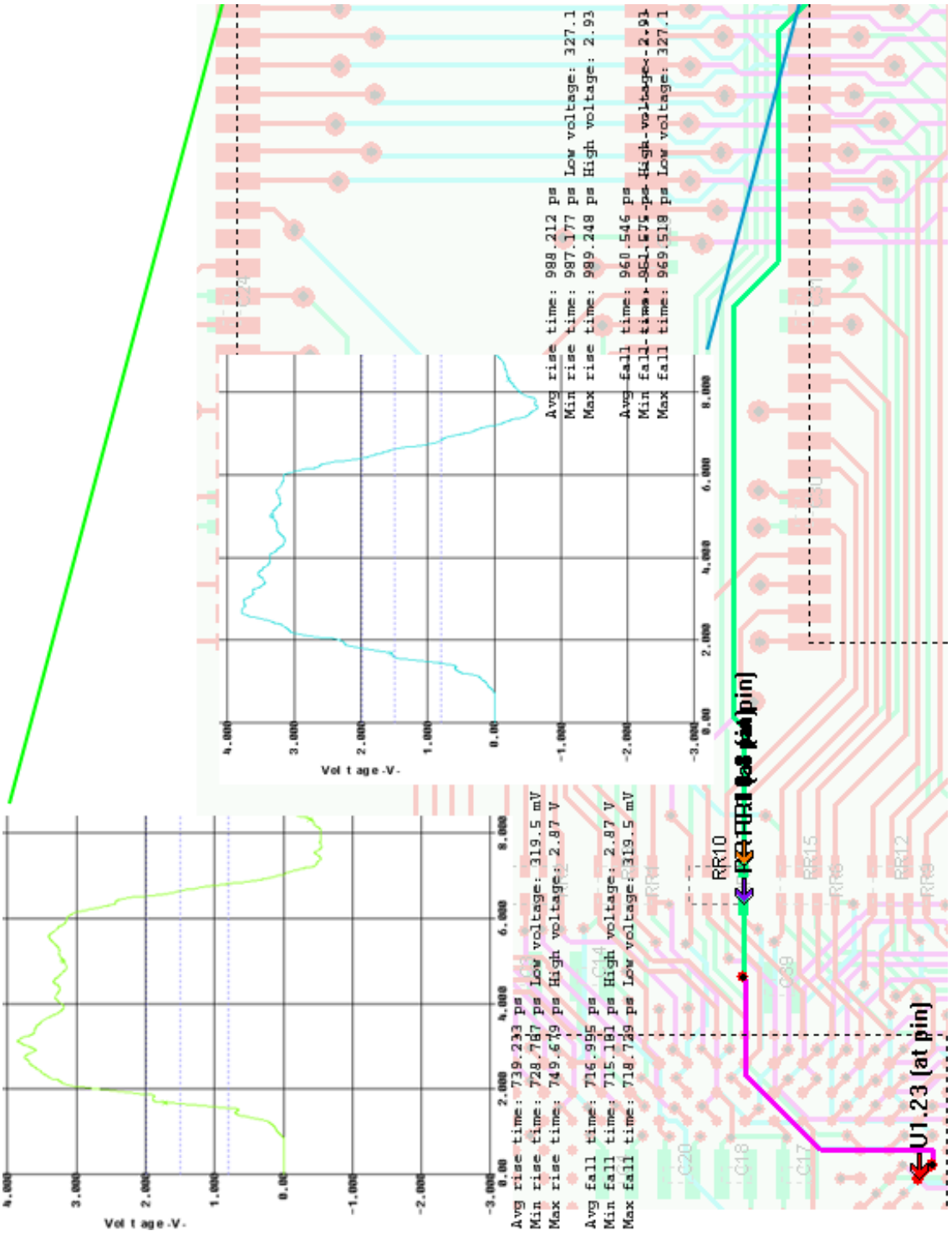


Table 5-4. Statistics for the Shortest Net (D16)

Selected-net name	D16
Total copper delay of all segments	0.0980 ns
Total length of all segments	1.585 cm
Number of segments	12
Number of vias	2
Minimum segment Z0	53.1 ohms
Maximum segment Z0	64.6 ohms
Total receiver capacitance	3.890 pF
Total segment resistance	0.055 ohms
Effective net Z0	46.4 ohms

Figure 5-3. Electrical Behavior on D16 Signal Trace

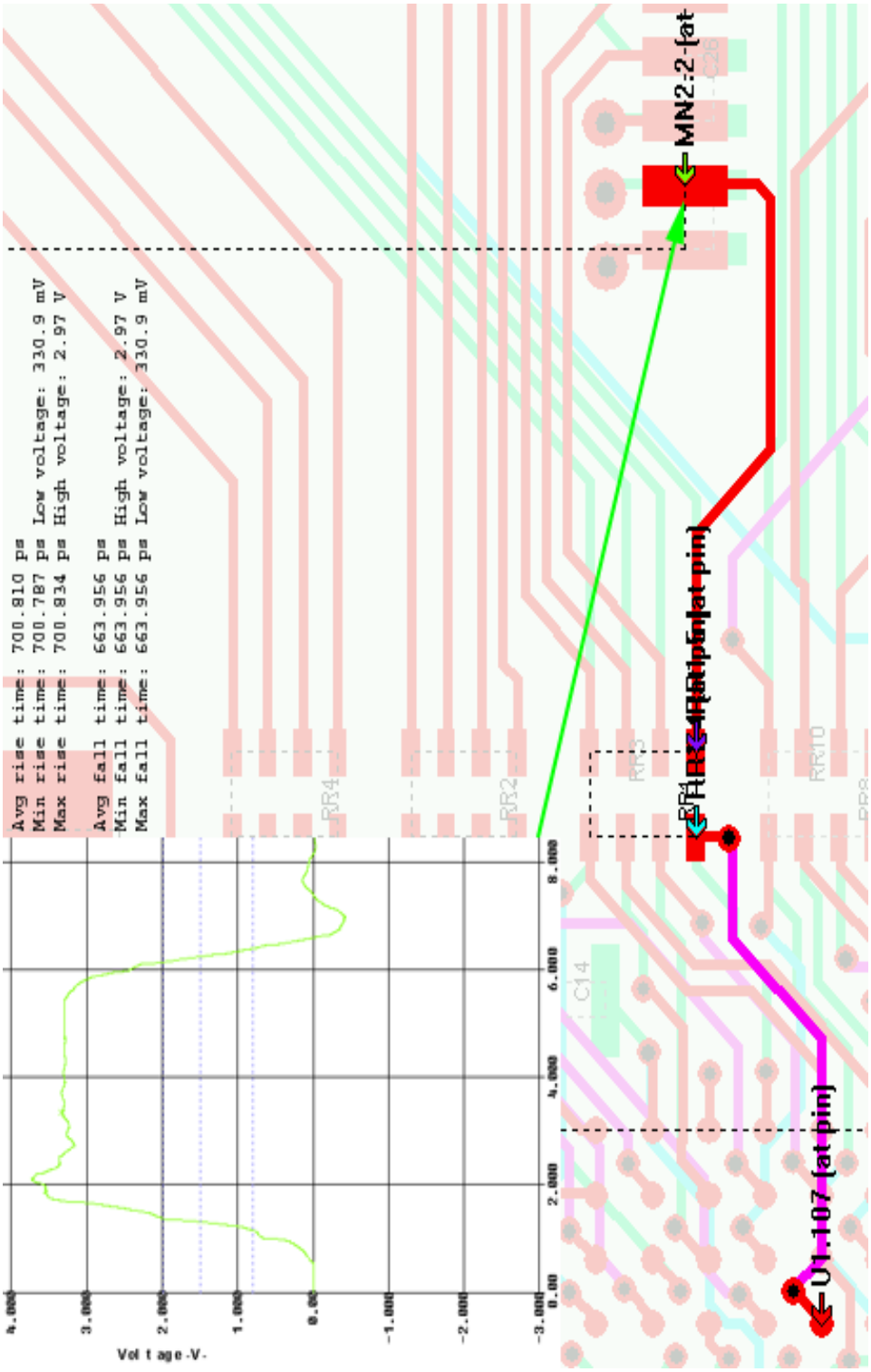
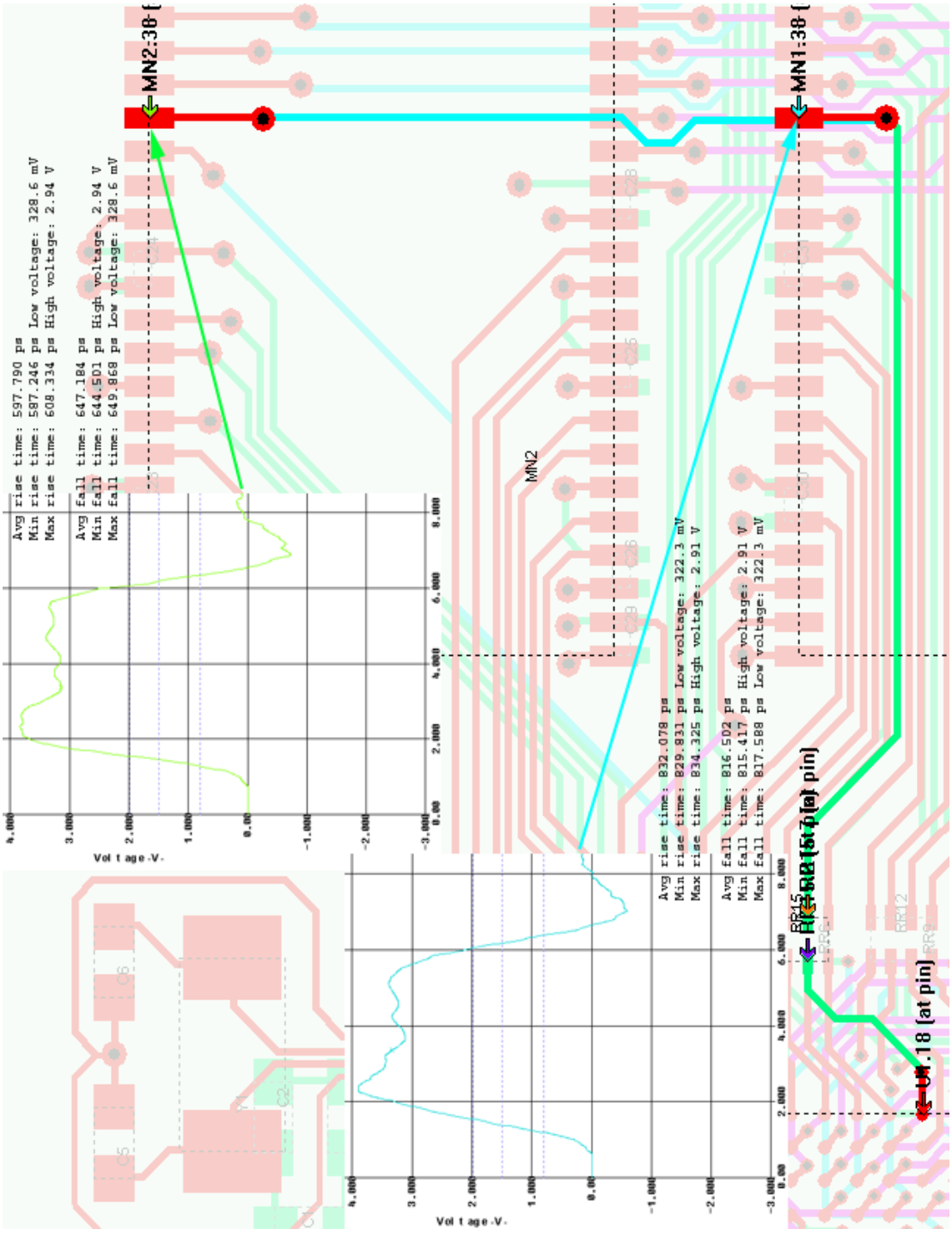


Table 5-5. Statistics for the SDRAM Clock Net (SDCK)

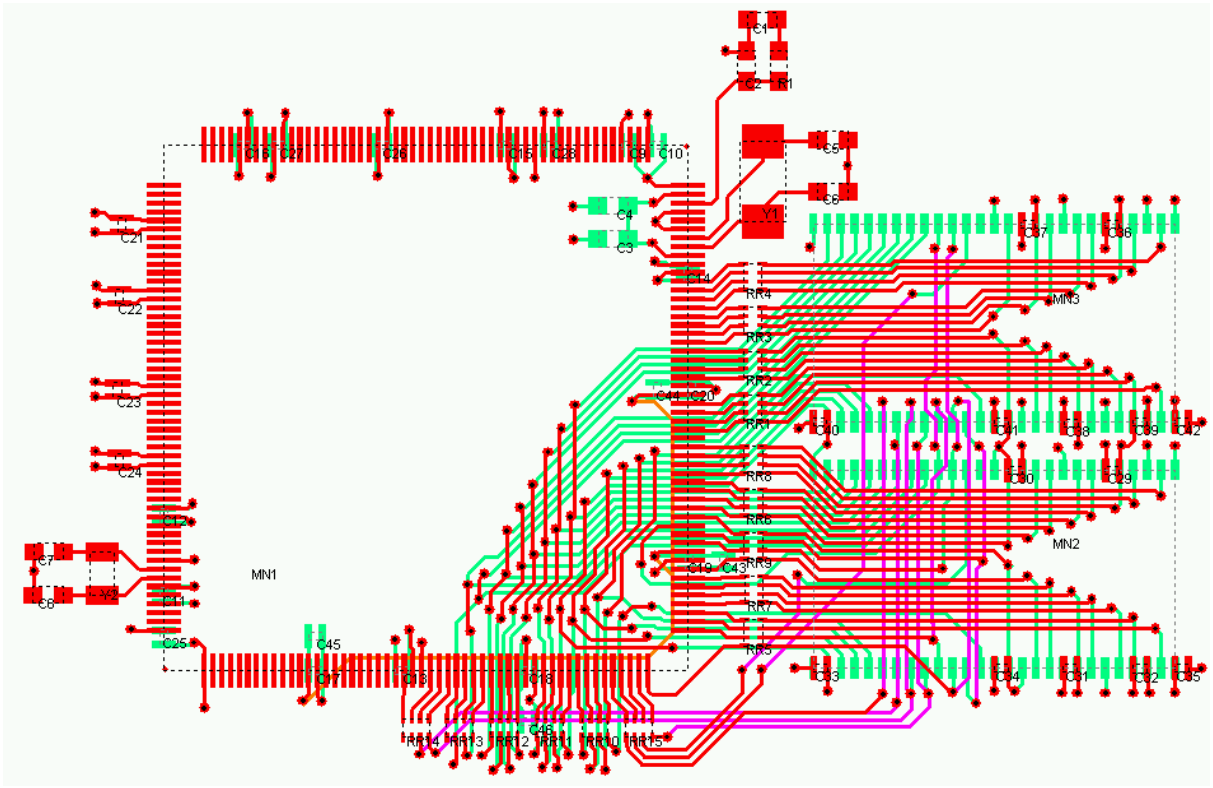
Selected-net name	SDCK
Total copper delay of all segments	0.2796 ns
Total length of all segments	4.568 cm
Number of segments	16
Number of vias	3
Minimum segment Z0	60.6 ohms
Maximum segment Z0	64.6 ohms
Total receiver capacitance	5.440 pF
Total segment resistance	0.157 ohms
Effective net Z0	47.9 ohms

Figure 5-4. Electrical Behavior on SDCK Signal Trace



5.2 AT91SAM9260 in QFP Package: PCB Design Example

Figure 5-5. AT91SAM9260 (or AT91SAM9G20, AT91SAM9XE) Board Design Example



In this design example, the trace lengths, the necessary PCB surface, and the signal integrity at SDRAM bus signals level have been optimized.

Extracted from "HyperLynx BoardSim" V7.7 by Mentor Graphics, the following trace data gives the propagation delay, the physical length, the effective net impedance, …, according to the stack-up choice and trace geometry.

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Table 5-6. Statistics for the Longest Net (A14)

Selected-net name	A14
Total copper delay of all segments	0.4572 ns
Total length of all segments	7.911 cm
Number of segments	19
Number of vias	3
Minimum segment Z0	67.7 ohms
Maximum segment Z0	67.7 ohms
Total receiver capacitance	4.120 pF
Total segment resistance	0.371ohms
Effective net Z0	27.9 ohms

With this trace (the longest), by adding a serial termination resistor equal to 27 Ohms, a simulation gives the following result at SDRAM device level:

Figure 5-6. Electrical Behavior on A14 Signal Trace

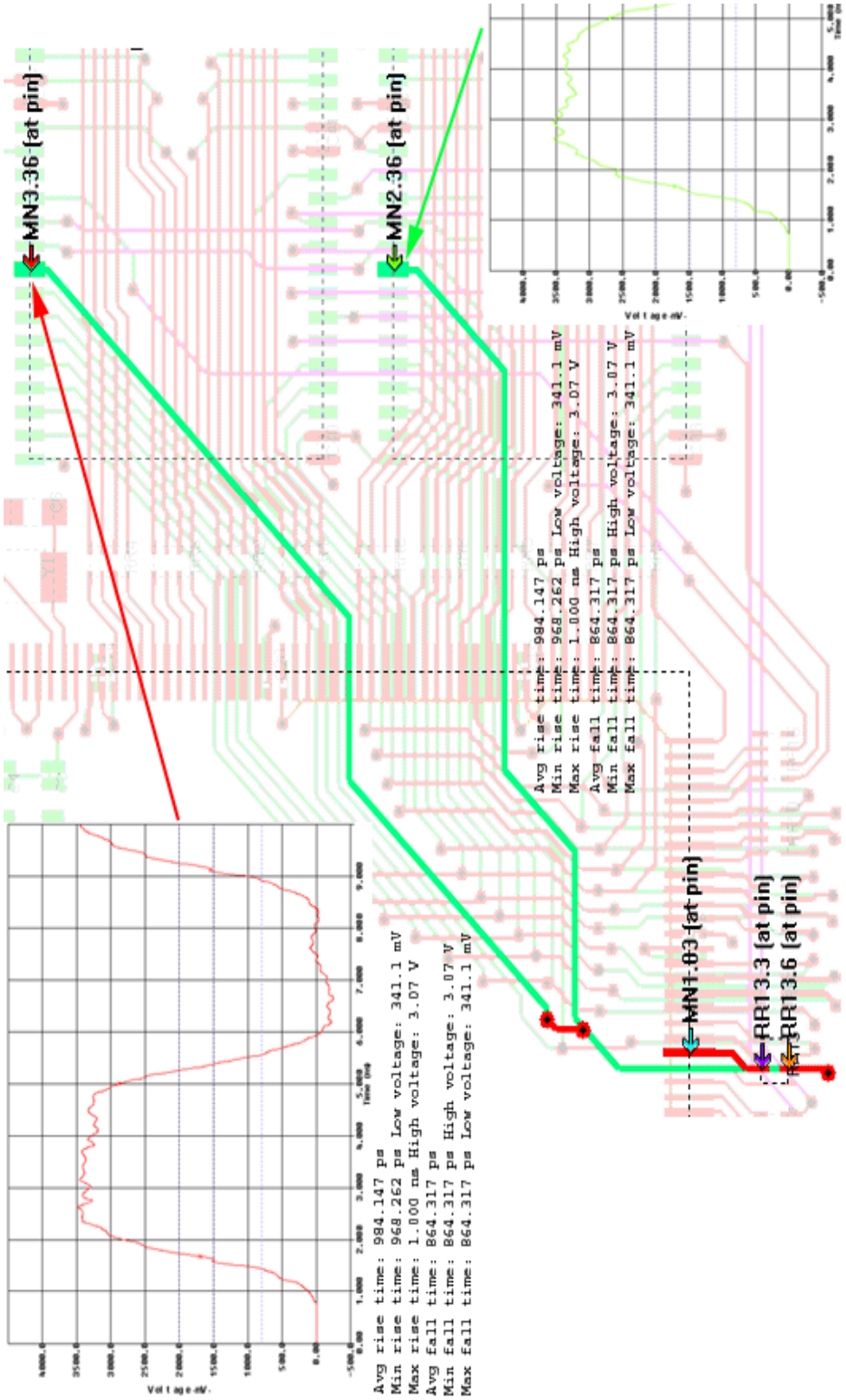
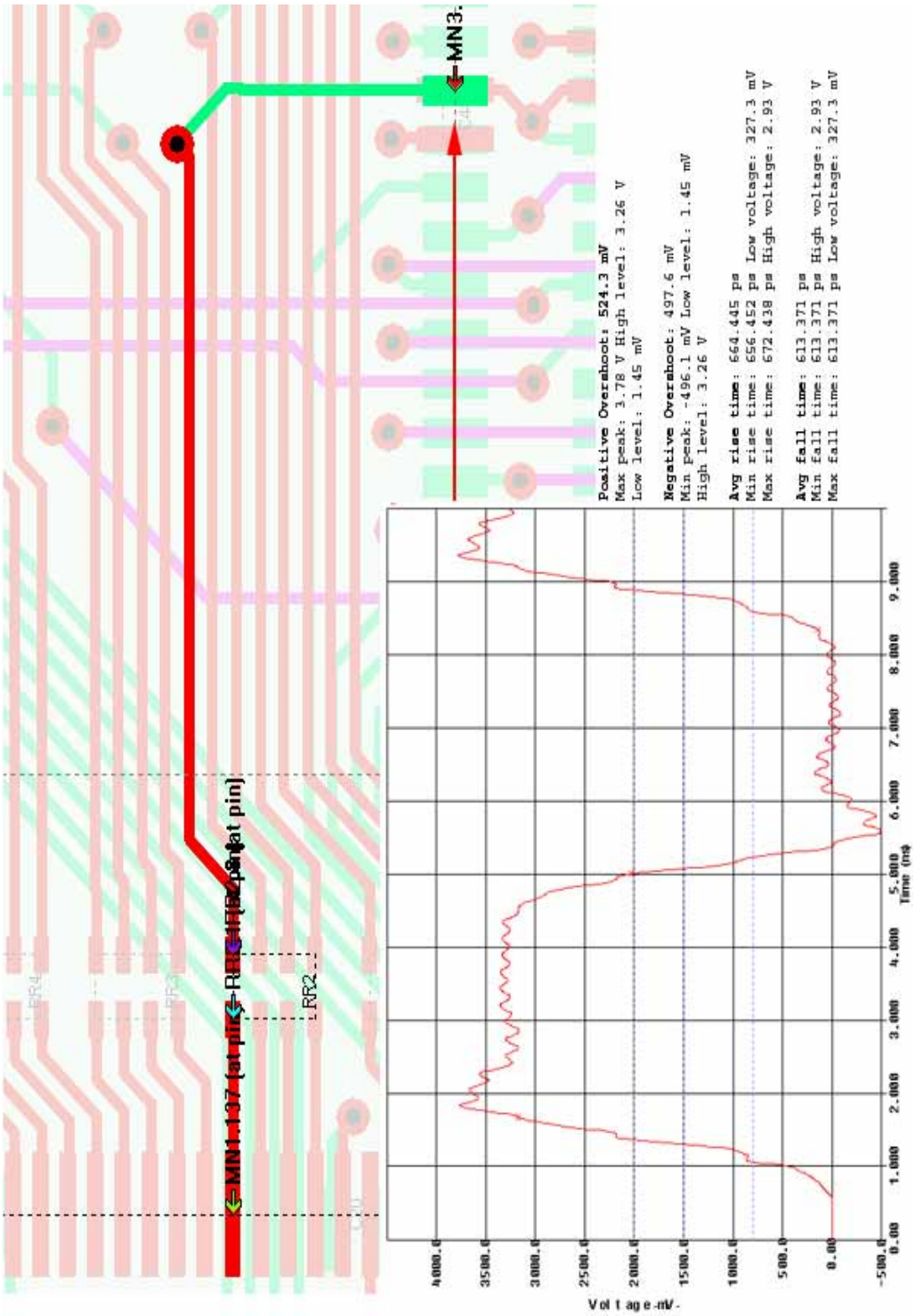


Table 5-7. Statistics for the Shortest Net (D23)

Selected-net name	D23
Total copper delay of all segments	0.1274ns
Total length of all segments	2.204 cm
Number of segments	8
Number of vias	1
Minimum segment Z0	67.7 ohms
Maximum segment Z0	67.7 ohms
Total receiver capacitance	2.300 pF
Total segment resistance	0.103 ohms
Effective net Z0	57.9 ohms

With this trace (the shortest), and by adding a termination resistor equal to 27 Ohms, a simulation gives the following result at SDRAM device level:

Figure 5-7. Electrical Behavior on D23 Signal Trace



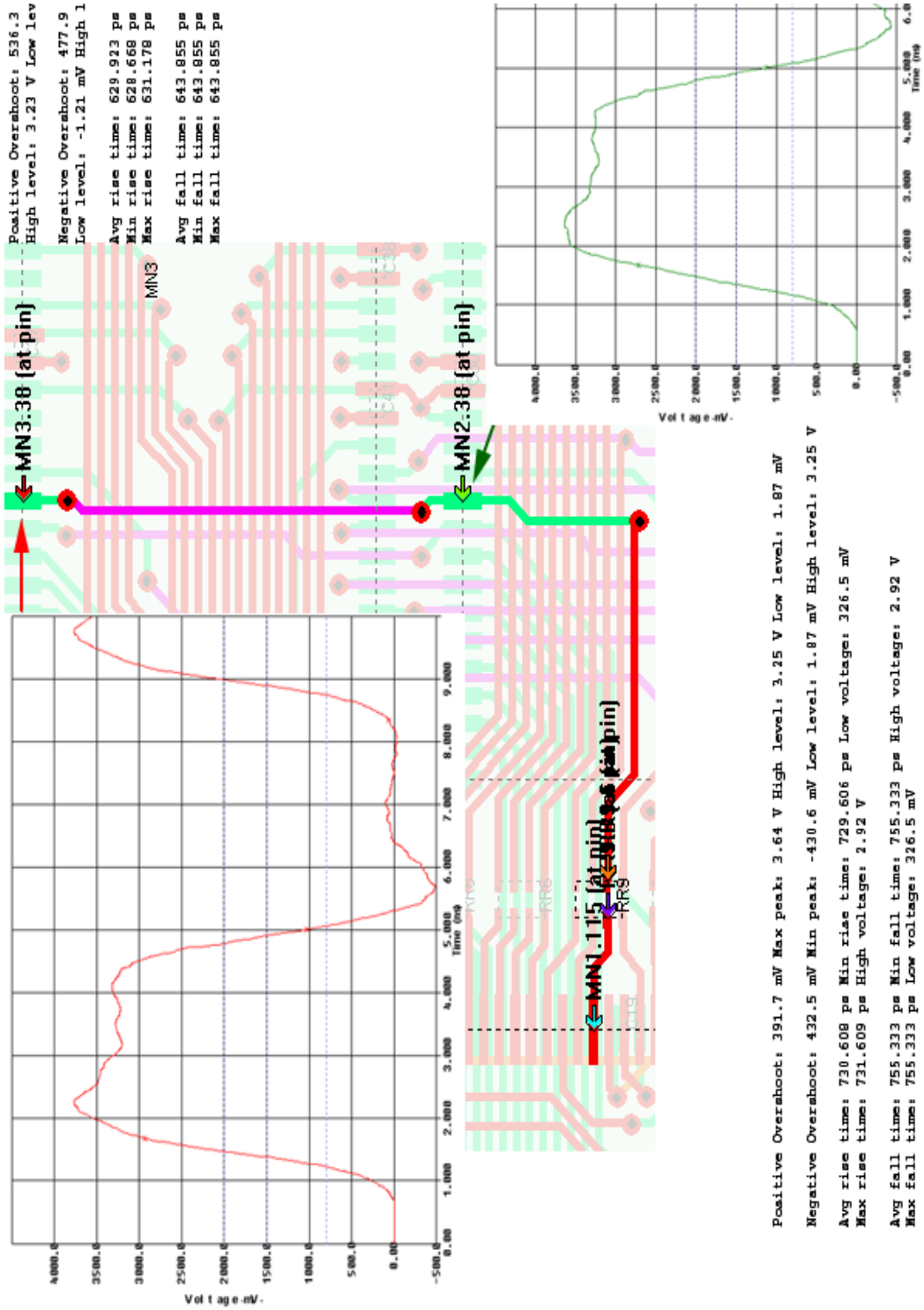
The next simulation has been made on SDCK signal. As described in this document, Atmel uses a faster driver than the other output drivers for data, address and control buses.

Table 5-8. Statistics for the SDRAM Clock Net (SDCK)

Selected-net name	SDCK
Total copper delay of all segments	0.2092 ns
Total length of all segments	3.397 cm
Number of segments	16
Number of vias	3
Minimum segment Z0	42.1 ohms
Maximum segment Z0	67.7 ohms
Total receiver capacitance	3.820 pF
Total segment resistance	0.133 ohms
Effective net Z0	45.5 ohms

With this trace, by adding a serial termination resistor equal to 27 Ohms, a simulation gives the following result at SDRAM device level:

Figure 5-8. Electrical Behavior on SDCK Signal Trace



5.3 Information on Provided Layout Files

This Application Note is delivered with an archive file containing layout example applicable to the AT91SAM9260, AT91SAM9G20 or AT91SAM9XE microcontrollers. Both layout project examples, for QFP and BGA packages, are available from this archive file.

In addition to the Zuken CadStar project, you will find, in the attached files, all possible exported formats with this version of software.

Revision History

Doc. Rev	Comments	Change Request Ref.
6386A	First issue	

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