Abhishek Agrahari

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Profile

12+ years of **relevant** rich experience in various domains.

- **2** years as **Advanced Product Engineer** for Questa Static Verification, Lint/CDC at **Siemens EDA**, NOIDA
- **6** years as **QA Lead for Precision and Oasys tool** at **Siemens EDA**, NOIDA
- **1** year as a **Senior Design Engineer** at, **Wipro** Technologies Bangalore
- **3** years as a **Senior Application Engineer** in **CoreEL** Technologies, Bangalore.

Currently working as a **Product Engineering (PE) for Questa Lint/CDC tool** at **Siemens EDA (Mentor Graphics) I Pvt. Ltd, NOIDA, India.**

Skill Set

- **Operating System:** Linux, Windows
- **Languages:** VHDL, Verilog, SV, JQL
- **Protocol:** Basic understanding of **AMBA**
- **Scripting Languages:** Shell, TCL, UNIX, Linux Commands, **JIRA, Agile** Methodology Python, Basic **Assertion** Checks, **ABV**
- **Tools Usage : Xilinx** (ISE, XST, Vivado, ISIM, Chip scope),**LAB VIEW**, **Oscilloscopes** , **Mentor Graphics** (Questa **Lint** , **CDC**, Precision, Modelsim, **Calibre**, Formal Pro, Powerpro, Oasys, **DFT** Advisor, **ATPG**, MBIST , NITRO , IC Station), **Cadence (**PSpice , **Virtuso), Matlab, Camtasia , MS Word, PPT, Excel**
- **FPGA Families: Xilinx** (Spartan3e, VirtexII, Virtex 4, **Zynq** Series, Cool runner CPLD, Core generator **IP Cores**), **Altera** (Quartus), **Libero** (Polarfire, Igloo, RTG4) , **Digital Design**
- **Technology Awareness:** IC fabrication process, RTL to GDSII design flow, FPGA AND **ASIC design flow**, **PDK**, **DRC, LVS**, TSMC technology library, **IC Testing**, **DFT , CAD Tools**
- **Version Control Software:** Perforce, Clear Quest, CVS, SVN, Git, **Devops-Jenkins, CI-CD**

Work Experience

Siemens EDA (Mentor Graphics) I Pvt Ltd, NOIDA **[Oct 2012 – Jan 2024]**

- **Advanced Product Engineer- Questa Lint/CDC**
- **Project Management for Precision tool using JIRA Agile Methodology**
- **QA Lead -Precision FPGA and Oasys ASIC synthesis Tool**

Project Details:

Currently I am working as a **Product Engineer** for ***Questa Lint/CDC tool***. I have also performed **QA Lead** for **Precision and Oasys synthesis Tool and Project management for Precision Tool using JIRA.**

Responsibilities:

- Assisting field and AE teams by offering support on Questa static verification tool, **Lint and CDC** tool
- Providing technical support to the customers in their **ASIC and FPGA** development design cycle
- Working on Standard checks like **STARC, RMM, DO-254** and **Custom Checks**
- Lint FPGA Design flow implementation
- Helping in **collateral development** like documentation support, developing AE training material, AppNote creation, Field Training etc.

- QA Lead for **Precision and Oasys** Synthesis tool
- Analyzing daily regression run for different builds in Mainline and Trunk.
- Culprit analysis on different builds, bug analysis and fixing, tracking issues and reporting to RnD
- QoR Analysis for different nightly builds
- **Automation of regression** analysis using **Jenkins** and Scripting
- Implementation of **unit testcases for issues** debugging using HDL (**VHDL, Verilog/SV**)
- Product release testing, (Check point, License testing, Regression)
- Newly added **feature testing** for the latest product release

Wipro Technologies, Bangalore [**July 2011– Sep 2012]**
Senior Project Engineer
Project Details:

Worked as a senior project engineer for different client projects.

Responsibilities:

- Design and implementation of PMIC IC in Verilog
- Group of 4 members were deployed to the project. Everyone has their own responsibility.
- I was working on one major module i.e. Coulomb Counter
- Worked on **FPGA prototyping** module; Implementation of baseband modulation of transceiver 802.16e -WiMAX.
- Performed RTL coding in Verilog/VHDL for the dedicated Module, testbench Verification, Assertion based verification Synthesis, **STA**, checking **CDC** issue and perform **Lint** checks for the same.

CG-CoreEL (I) Pvt Ltd, Bangalore **[Apr 2008 - June 2011]**
Application Engineer (Xilinx and Mentor Graphics Products)
Project Details:

Worked as an Application Engineer for Xilinx and Mentor Graphics Tools

Responsibilities:

- Providing technical support to the customers those were using Xilinx FPGAs (Spartan,Virtex) and Mentor Graphics tools in their projects.
- Providing demos to the customers, onsite training and **FPGA prototyping** project support.
- Hands on training to Xilinx and Mentor tools usage and support.
- Creating training materials, documentation, Lab and PPTs materials for customers

Academic Qualifications

- **MTech** (Research) 2007-2011 in VLSI design from **NIT Surat,** Gujarat. 7.5 CGPA
- Research Associate ,2006-2007, in SMDP Project, **NIT Surat,** Gujarat
- Certification Course in **VLSI design** ,2005-2006, **Pune,** Grade A
- BTech in Electronics & Communication, 2000-2004, UPTU, Lucknow,70%
- 12th ,Math, 1998-2000, U.P Board, 74%
- 10th ,Science, 1996-1998, U.P. Board,77%

Personal Details

- **Date of Birth**: July 1984
- **Marital Status**: Married
- **Current Address**: Sector 70, NOIDA, U.P.