DESIGN OF LOW POWER PULSE GENERATE FLIPFLOP DESIGN BASED ON A SIGNAL FEED-THROUGH SCHEME

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ABSTRACT

In this project, analysis of average power, delay and power delay product is done by shift register (PIPO) using 90nm technology. Low power flip-flops are crucial for the design of lowpower digital systems. As Metal Oxide Semiconductor Field Effect Transistor (MOSFET) devices are scaled down to nanometer ranges, Complementary MOS (CMOS) circuit's total Power consumption has a new definition. Due to integration of millions of components and shrinking process technology, nowadays leakage power tends to play a major role in total power consumption. A low power pulse triggered flip-flop with signal feed through scheme using Conditional Pulse Enhancement technique is presented in this paper. The proposed design adopts a modified True Single Phase Clock Latch structure and employs a signal feed through scheme to enhance the delay. The long discharging path problem in conventional explicit type pulse triggered flip flops are successfully solved through this method. In order to further enhance the speed and power performance, a conditional pulse enhancement technique is employed at the discharging path. Post layout simulation results based on TSMC 180 nm technology reveals that proposed flip flop features better power delay product when compared to conventional flip flops like epDCO, CDFF, SCDFF, MHLFF, SCCER and flip flop based on signal feed through scheme.

KEYWORDS- Optical nano-antennas, Energy harvesting, Electron –beam, Fabrication, Low cost, Nano-disk, Plasmonic, Nano-laser

I.INTRODUCTION

Flip-Flops (FFs) are the basic storage elements used extensively in all kinds of digital designs. The digital designs nowadays often adopt intensive pipelining techniques and employ many FF rich modules and also estimated that the power consumption of clock system, which consists of clock distribution networks and storage elements is as high as 20% to 45% of the total system power. Pulse triggered flip flop (P-FF) is considered as a popular

alternative to the conventional master slave based FF in the application of high speed operations. Besides the speed advantage, its circuit simplicity is also beneficial to lowering the power consumption of the clock tree system. A P-FF consists of a pulse generator for generating strobe signals and a latch for data storage. Since triggering pulses generated on the transition edges of the clock signal are very narrow in pulse width, the latch acts like an edge triggered FF. The circuit complexity of a P-FF is simplified since only one latch, as opposed to two used in conventional master slave configuration, and is needed. P-FFs also allow time borrowing across clock cycle boundaries and feature a zero or even negative setup time. P-FFs are thus less sensitive to clock jitter. The pulse generation circuitry requires delicate pulse width control in the face of process variation and the configuration of pulse clock distribution network. Depending on the method of pulse generation, P-FF designs can be classified as implicit or explicit. In an implicit type P-FF, the pulse generator is a built in logic of the latch design, and no explicit pulse signals are generated. In an explicit-type P-FF, the designs of pulse generator and latch are separate. Implicit pulse generation is often considered to be more power efficient than explicit pulse generation. This is because the former merely controls the discharging path while the latter needs to physically generate a pulse train. Implicit-

In the past few years, an stimulating development in nano-optical research has position in with the recognition that metallic nano particles with their plasmon resonances may be used in a approach very analogous to the way electrical engineers of the twentieth century have developed radio-frequency (RF) antennas. This introduces the idea of optical nano-antennas. Following many of the same rules that relate to RF antenna design, also the properties of optical nano-antennas can be customized to execute desired functions. Like their RF counterparts, nano-optical antennas may be seen as impedance matching devices between free space radiation and the radiation/photon source. In receiving mode the antenna is capable to confine free space radiation to a sub wavelength region in the locality of the structure. With the control of emission rates and directions of quantum emitters like individual molecules or quantum dots at the nano scale enabling well-organized coupling to more conventional optical technologies could have technological applications in building single photon detectors on the nano-scale. This is especially interesting for the development of the sources required in quantum cryptography. Being the trendiest option in terrestrial TV

II.DIFFERENT TYPES OF FLIP FLOP

A.Proposed Double Edge Pulse Triggered Flip Flop Design

The four circuits considered above experience the worst case timing during the data transitions occurring at 0 to 1. The proposed design employs a signal feed-through technique to improve this delay. The SCDFF design and the proposed design have the static latch structure and a conditional discharge scheme to avoid continuous switching at an internal node. The major differences made in this design lead to a unique TSPC latch structure and make the proposed design distinct from the previous one. An approach suitable for high-performance, low power applications is the use of dual edge-triggered (DET). Substantial

Power savings in the clock distribution network can be achieved by reducing the clock frequency by one half. This can be done if every clock transition is used as a time reference point instead of using only one transition of the clock.

In the proposed design pulse generator circuit is designed using the transmission gates. This pulse generator is suitable for double-edge sampling. In the first stage of the TSPC latch a pull-up pMOS transistor with gate connected to the ground is used which gives rise to a pseudo-nMOS logic style design. Thus the charge keeper circuit for the internal node X can be saved. This approach also reduces the load capacitance of node X, which makes the circuit simpler. Also a pass transistor MNx controlled by the pulse clock is included so that input data can drive node Q of the latch directly (the signal feed-through scheme). Along with the pull-up transistor MP2 at the second stage inverter of the TSPC latch, this extra passage facilitates auxiliary signal driving from the input source to node Q. The node level can thus be quickly pulled up to

P-FF Design Based on Signal Feed through Scheme

The proposed design employs a static latch structure and a conditional discharge method to keep away from surplus switching at an internal node connection. On the other hand, the differences which lead to an exclusive TSPC latch structure and make the proposed design separate from the earlier one. Firstly, a weak pull-up pMOS transistor MP1 with gate connected to the ground is used in the first phase of the TSPC latch, which gives growth to a pseudo-nMOS logic procedure design, and the charge keeper circuit for the internal node X. In addition to the circuit simplicity, this approach also reduces the load capacitance of node. A pass transistor MNX forced by the pulse clock is included so that input data can compel node Q of the latch directly

A. Plasmonic Dipole UWB Nano-antennas

Dual-Vivaldi nano-antenna arrays were intended, fabricated, and optically characterized. The antenna arrays were characterized by measuring the scattered light at infrared and visible spectral ranges. A new technique for antenna and load impedance measurements using scattering data has been developed.The radiation efficiency and the spectral response of the antennas were initiate to be in good agreement through geometric simulations. The results presented here demonstrate the particularly wideband nature of the Dual-Vivaldi nano-antennas and the strong impact of load at the antenna terminals on its scattering response. These properties, as well as their several degrees of freedom for design, deliver the Dual-Vivaldi nano-antennas excellent candidates for optical sensing applications and energy harvesting. Various applications of nano-antennas will be discussed.

B. Plasmonic Dimer Nano-Antenna

We report on the fabrication and dark-field spectroscopy characterization of Au dimer nanoantennas located on top of SiO2 nanopillars. The reported process enables the fabrication of nanopillar dimers with gaps behind to 15 nm and heights up to 1 μm. A clear hope of the plasmonic resonance situation on the dimer gap is observed for smaller pillar

heights, viewing the high uniformity and reproducibility of the process. It is shown how mounting the height of nanopillars extensively affects the recorded flexible scattering spectra from Au nanoantennasThe outcome are compared to finite-difference time-domain (FDTD) and finite-element method (FEM) simulations. Additionally, measured spectra are accompanied by dark-field microscopy images of the dimers, viewing the well-defined modify in color. Placing nanoantennas on nanopillars with a height analogous to the in-plane dimer magnitude results in an enhancement of the scattering reaction, which can be implicit through concentrated interface of the near-fields with the substrate. When increasing the pillar height more, scattering by the pillars themselves manifests itself as a well-built tail at lower wavelengths.

Additionally, well-built directional scattering is expected as a effect of the interface between the nanoantennas and nanopillars, which is in use into account in simulations. For pillars of height secure to the plasmonic resonance wavelength, the scattering spectra become new complex due to additional scattering peaks as a consequence of larger geometrical nonuniformities.

C. *Plasmonic Characterization Of Integrated Circuit With High Efficiency Nano-antennas*

Four types of nanoantennas have been intended and characterized at 1.55 μm wavelength: Dipole antenna, Yagi-Uda antenna, dipole antenna array and bowtie antenna. The spectrum, coupling efficiency, and far field radiation patterns are also investigated. We also quantitatively characterized the correlation between the couple-in efficiency and the spot size of the incident light. For the three dipole-type antennas, the couple-in and couple-out efficiencies have been precise experimentally. A plasmonic integrated circuit has also been designed and fabricated with these four types of nanoantennas.

D. *Plasmonic Bowtie Nano-antennas*

Bowtie nanoantennas characterize the extension of dimer nanoantenna model. We report on a temperature-reactive tunable plasmonic device that incorporates together bowtie nanoantenna arrays (BNAs) with a submicron-thick, thermosensitive hydrogel coating. The coupled plasmonic nanoparticles present an intrinsically higher field enhancement than conventional individual nanoparticles. The favorable scaling of plasmonic dimers at the nanometer scale and ionic distribution at the submicron scale is leveraged to attain strong optical resonance and rapid hydrogel response, respectively. We exhibit that the hydrogel-coated BNAs are able to sense environmental temperature variations. The phase transition of hydrogen leads to 16.2 nm of significant wavelength shift for the hydrogel-coated BNAs, whereas only 3 nm for the uncoated counterpart. The response time of the device to temperature variations is only 250 ms, due to the small hydrogen depth at the submicron scale.

The demonstration of the capacity of the device to tune its optical resonance in answer to an environmental stimulus suggests a possibility of making many other tunable plasmonic devices throughout the incorporation of attached plasmonic nanostructures and various environmental-responsive hydrogens.

III.DIELECTRIC NANO-ANTENNAS

An optically resonant dielectric nanostructure is a new path in nanophotonic research which gives a strong promise to tribute or alternate plasmonics in many possible application areas. The main advantages of significant dielectric nanostructures over conventional plasmonics are low victims, wide variety of applicable dielectric materials and strong magnetic resonant answer. So far most of explore in this field has been conducted with silicon as a material for nanostructures due to its one of the highest rate of refractive index at optical frequencies and CMOS compatibility. For these reasons in recent studies examine focus starts shifting towards other fitting materials such as III-V semiconductors, e.g. GaAs or GaP, and wide-bandgap semiconductors such as TiO2.

IV.SYSTEM SPECIFICATION

E. *HFSS*

Antennas are almost everywhere from commercial application such as smart phones, RFID tags ,and wireless printers, to security application such as phased array antennas for aircraft radar systems or satellite based , to provide incorporated ground based communication systems. Electromagnetic simulation is a precious tool in antenna design and platform combination providing the trendy, the ability to virtually design and estimate what if scenarios as well as verify the final artificial design.

F. *Antenna simulation technologies in HFSS*

HFSS offers the subsequent simulation methods and tools depending upon the kind of troubles you want to solve :

1. Finite element method (Enabled with HFSS)

2. Integral equations (Enabled with HFSS-IE)

3. Physical optics (Enabled with HFSS-IE)

4. FEM Transient (Enabled with HFSS-TR)

5. Antenna design toolkit provided with HFSS including over 50 standard antenna designs.

G. *Dielectric Yagi-uda Nano-antennas*

Conventional antennas, which are widely engaged to transmit radio and TV signals, can be used at optical frequencies as long as they are shrink to nanometer-size dimensions. Optical nanoantennas made of metallic or high-permittivity dielectric nanoparticles permit for attractive and manipulating light on the scale much slighter than wavelength of light. Based on this facility, optical nanoantennas tender unique opportunities regarding key applications such as optical communications, photovoltaics, non-classical light emission, and sensing. From a large number of suggested nanoantenna concepts the Yagi-Uda nanoantenna, an optical analogue of the deep-rooted radio-frequency Yagi-Uda antenna, stands out by its competent unidirectional light emission and development.

Following a brief introduction to the emerging field of optical nanoantennas, here we analysis recent theoretical and tentative activities on optical Yagi-Uda nanoantennas, including their intend, fabrication, and applications. We also discuss numerous extensions of the conventional Yagi-Uda antenna design for broadband and tunable action, for applications in nanophotonic circuits and photovoltaic devices.

H. ***Nano-anntennas***

The Yagi-uda nano antennas also have the prospective to act as cooling devices that illustrate waste heat from buildings or electronics without using electricity. The nano antennas intention mid-infrared rays, which the Earth constantly radiates as heat after fascinating energy from the sun during the day. In contrast, traditional solar cells can only unvisible lightinterpretation them idle after dark. Infrared radiation is an mainly rich energy source because it also is generated by industrial processes such as coal-fired plants. The nano antennas are little gold squares or spirals set in a particularly treated form of polyethylene, a material used in plastic bags. While others have successfully invented antennas that accumulate energy from lower-frequency regions of the electromagnetic spectrum, such as microwaves, infrared rays have verified more indefinable.

I. ***Dielectric Optical Nano-antennas***

Infrared near-field microscopy can be used to examine the local field of photonic structures. Near-field images of a resonant infrared antenna demonstrate the clear signature of a dipolar oscillation mode on the Au rod. The amplitude image exhibits a high signal at the rod ends which are 180° out of phase. If the antenna structure is adapted by a cut at the centre of the Au rod, the near-field images reveal two dipolar oscillation modes on the segments. Systematic studies allow to examine the coupling between the segments and to illustrate the optical properties of the antenna structures. Polarized measurements allow to filter out specific components of the optical field related to photonic structures or devices and to examine the field in the antenna gap.

V.CONCLUSION

In digital VLSI, sequential elements are most power consuming components. Flip-Flops are the basic storage elements and subsystem of clock distribution network which consume large amount of power. Nowadays for digital design, designers use pipelining techniques to design flipflop based systems, such as shift registers and register files. In this paper, Pulse Triggered Flipflop (P-FF) is discussed and Serial in Serial out (SISO) shift register is designed as its application. The main objective of this paper is to optimize the area and power of the shift register for use in Application Specific Integrated Circuits (ASICs) and embedded systems. This paper demonstrates the design of SISO shift registers in three different ways. First shift register is simple in structure and designed only by using P-FF. Second shift register uses clock gating circuit to reduce the switching power consumption and third design of shift register, pulse generator of P-FF is shared among all the latches. These three different SISO shift registers are compared in terms of power dissipation and

transistor counts. Shift register has been designed at schematic level and simulated using Tanner EDA at CMOS 32nm BSIM4 technology. The simulation results of SISO shift register with common pulse generator shows effective reduction of power consumption and transistor count. In this Paper, We have presented the modified proposed p-flip flop design by incorporating adiabatic logic circuit. The key idea is to provide a signal feed through from input source to the internal node of the latch, which provide extra driving facility to shorten the transition time. This paper presented different architectures of a low power flip flop structure. In this paper we have studies the basic architectures of a Flip flop design of CDFF, EP-DCO FF and Pulsed triggered flip flop for low power consumption with their comparative results.

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