Design and Analysis of a Master Slave Synchronous D-Flipflop for 3-bit Asynchronous Down Counter

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***Abstract*—The main aim of the project is to design of a Synchronous Master Slave D-Flip-flop by using minimum transistor sizes for the gates at both schematic and layout level implementation and analysis of the designed flip-flop did by calculating hold times, setup time, clock to Q delay at different capacitive loading conditions and at different transistor widths. The flip-flop also tested under different V_{DD} (supply voltages) and compared the power dissipation and delay values. The simulated results and the values of both the schematic level and layout level are compared and graphs are represented. Finally we implemented the 3-bit Asynchronous down Counter by using the designed flip-flop and got the simulated results. Moreover we presented the area required to implement the layout of both flip-flop and counter. The design and analysis part were done by using CMOSIS5 600nm Technology in Cadence tool.**

***Index Terms*— Asynchronous Down Counter, Load Capacitance, Master Slave Synchronous D-Flip-flop(MSSDF), NMOS transistor width (N), PMOS transistor width(P), Power Dissipation, Transistor Sizes.**

I. INTRODUCTION

D flip flops are also known as Delay flip-flop or Data flip – flop because they are used to store the 1-bit of data. They are widely using in digital electronics. In this paper, we are using master slave synchronous d-flip-flop, it is of negative edge triggering flip-flop that means whenever the clock transition from 1 to 0 (falling transition) the output Q follows the input data D and holds its value until next clock falling edge. The MSSDF reduce the glitches in the output that generally appears in the D-Flip-flop. Here, we can eliminate the race around condition that occurs in JK flip-flop because giving only one input D and it is inverting by using the inverter. The basic MSSDF, truth table and graphical representation represented below.

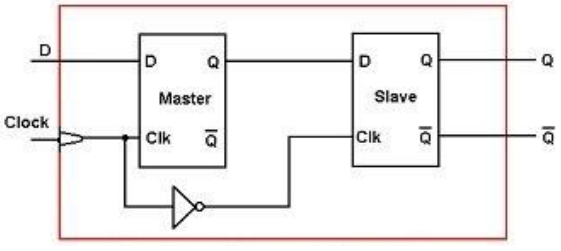

Fig 1 Master Slave Synchronous D-Flipflop[2]

Clk	D	Q	Q bar
0	0	Q	Q bar
0	1	Q	Q bar
1	0	0	1
1	1	1	0

Table 1 Truth Table for Master Slave D-Flipflop

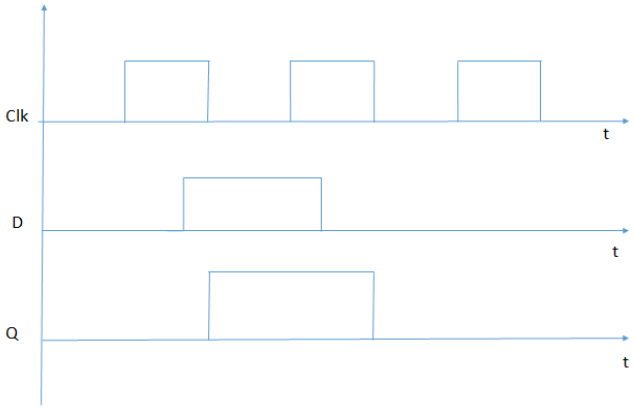

Fig 2 Timing Diagram Of Master Slave D-Flipflop

The MSSDF are used in many applications including Data storage registers, Counters, Shift registers and Frequency division circuits. Here we are designing a 3-bit asynchronous down counter which counts the input pulses from 111 to 000 in binary. The proposed counter basic diagram is represented below.

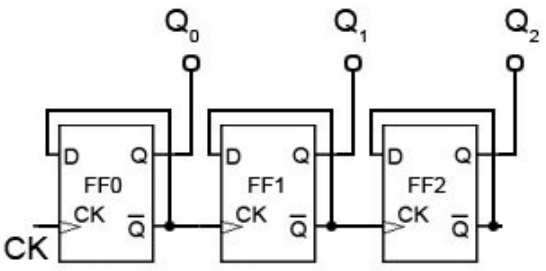

Fig 3 3-Bit Asynchronous Down Counter [2]

II. PROPOSED FLIP-FLOP DESIGN AND TRANSISTOR SIZES

We choose the basic inverter width as 2.5µm (P: 1.5 µm and N: 1.0 µm) based on the assumption to get the least average delay as we know least delay for P=$\sqrt{\mu}$ [1]. Here the value of µ is 2 which is the basic width of the PMOS. The P: N ratio is 1.5. The basic inverter diagram is represented below.

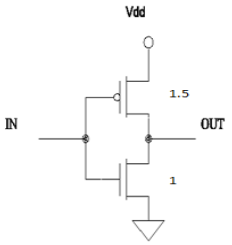

Fig 4 Cmos Inverter with Transistor Width

Here the same clock is used for the master and slave but we are inverting the clock while giving it to the slave. The transistor widths for inverting the clock are P: 5 µm and N: 1 µm. these widths are chosen for equal rising and falling delay.

The proposed MSSDF is shown below indicating the sizes of the transistors PMOS and NMOS of each gate in µm.

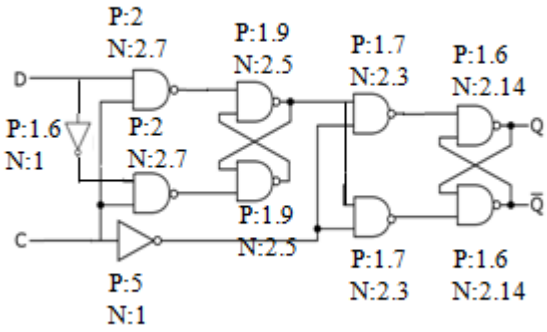

Fig 5 Design Implementation of MSSDF Indicating Size of Each Gate

The widths of the transistors are calculated based on the assumption that the Logical effort of the flipflop is equals to unity because we are designing an application counter by using the proposed flipflop in which one flipflop driving the other.

H=1

Here we calculated the sizes by assuming branching is equal to unity because the leakage through the feedback path is very low as compared to other paths for the proposed flipflop.

B=1

Then by using the stage effort and number of stages we calculated the widths of each transistor in the gates.

III. DESIGN IMPLEMENTATION OF MSSDF

Here we are giving a supply voltage V_{DD} = 3.3volts and the clock is generated at a voltage of 3.3volts for both schematic and layout level implementation of the MSSDF.

A. Schematic Level

The below diagram shows the schematic level circuit of the proposed flipflop. Here the buffer is used to give inputs to the Flipflop to smoothen the input waveforms. The transistor level diagrams of the gates in the circuit with sizes indicated are in the appendix.

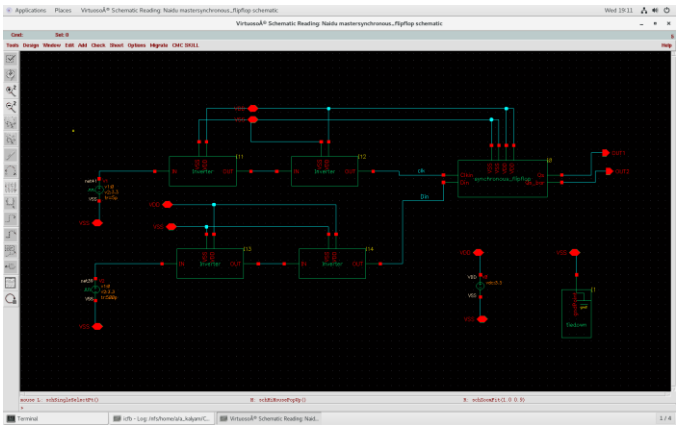

Fig 6 Flipflop at Schematic Level

The Clock to Q delay achieved was 332.2ps. The value indicating in the simulation below,

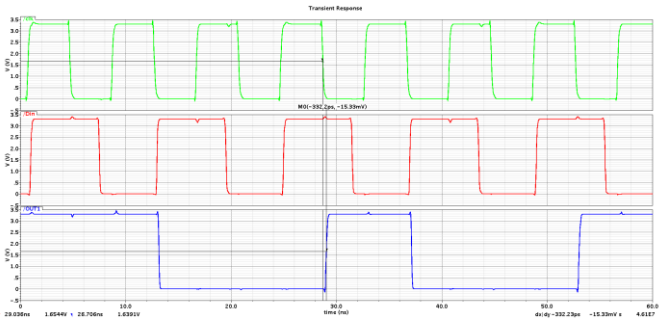

Fig 7 Delay of Flipflop at Schematic Level

B. Layout Level

The layout of the proposed MSSDF is shown below,

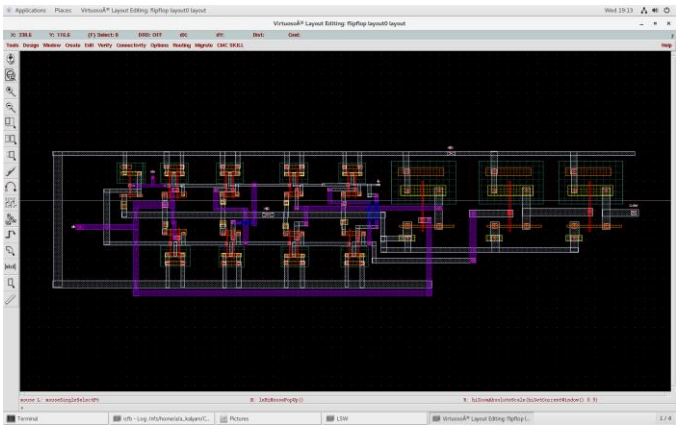

Fig 8 Layout of the MSSDF

In this we also placed a buffer at the output of Q_bar to smoothen because it is given as input to D and Clock in the counter

The post layout circuit diagram of the flipflop with connections shown below

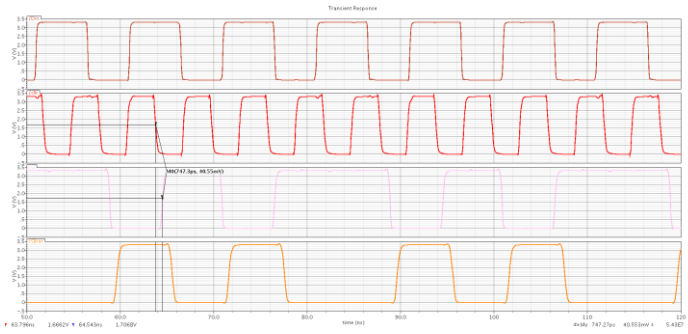

Fig 9 Delay of the MSSDF at Layout Level

The clock to Q delay achieved was 747.3ps. The results are indicating in the simulation below.

Here the clock Q delay of the MSSDF at layout level is more than at schematic level because at the layout level the parasitic capacitance is automatically included by the design tools such that the delay increased while at the schematic level parasitic capacitance is neglected.

IV. DESIGN IMPLEMENTATION AND ANALYSIS OF 3-BIT ASYNCHRONOUS DOWN COUNTER USING SYNCHRONOUS FLIPFLOP

Here we are giving a supply voltage V_{DD} = 3.3volts and the clock is generated at a voltage of 3.3volts for both schematic and layout level implementation of the counter using MSSDF.

A. Schematic level:

The 3-bit counter was build using the proposed MSSDF and the schematic level circuit diagram is shown below

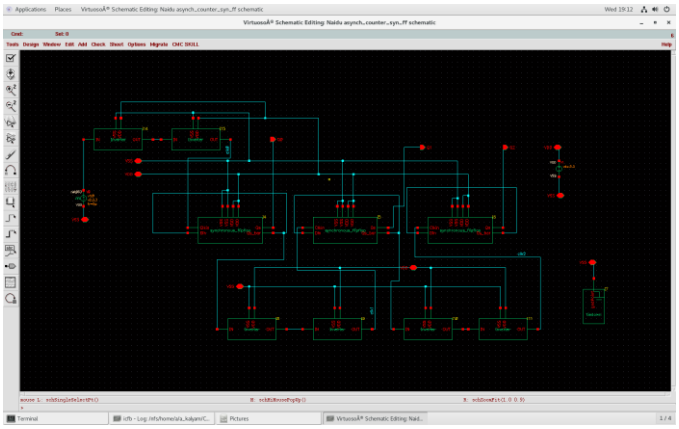

Fig 10 Asynchronous Counter at Schematic Level

The simulation results are shown in the graph below

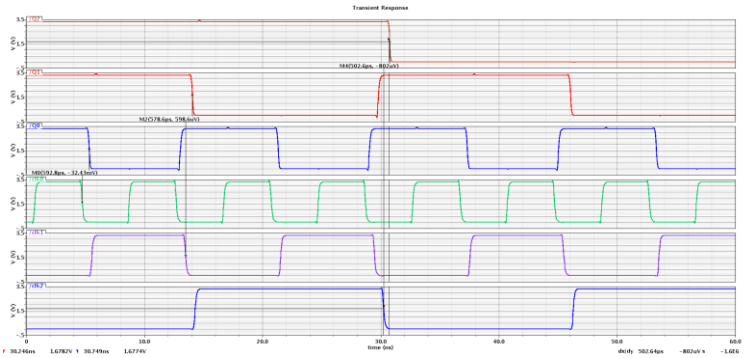

Fig 11 Delay of Counter at Schematic Level

B. Layout level implementation

The 3-bit asynchronous counter layout by using the proposed layout of MSSDF is shown below

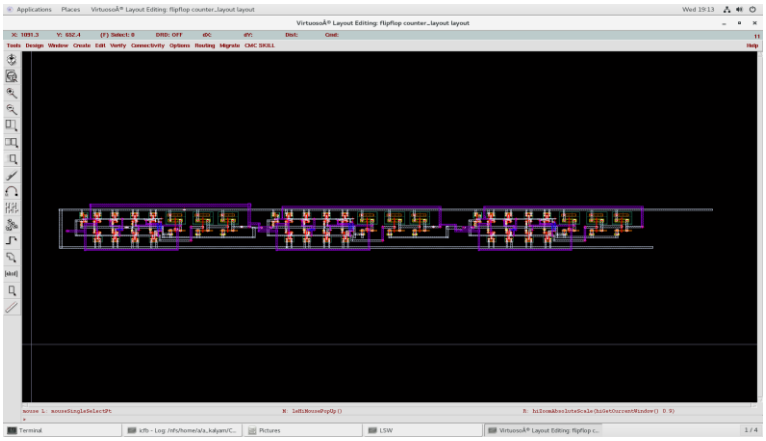

Fig 12 Layout of the 3-Bit Counter

Here, the three MSSDF are connected in series as per the circuit diagram of the 3-bit synchronous down counter.

The post layout simulations of input and output are shown below

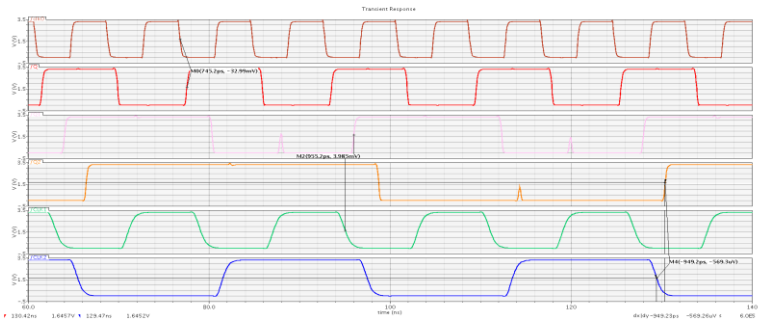

Fig 13 Delay of Counter with the MSSDF

We observe that in both the schematic level simulation and post layout simulations the counter is counting the input pulses down from 111 to 000 and again it starts from the first.

V. Results & Observations of MSSDF

A.Input Capacitance:

The input capacitance of the proposed flipflop are calculated below at both D input and clock input and is represented in the below table

INPUT CAPACITENCE		
input to	schematic	layout
D	1.70E-14	2.50E-14
Clock	8.00E-15	1.60E-14

Table 2 Input Capacitance

Here, it is observed that the input capacitance at the D input is more than the clock input in both schematic and layout level implementation of proposed Flipflop.

B.Setup time and Hold time:

The setup time and hold time of the implemented layout and schematic level of MSSDF is represented at the table below.

Setup time and hold time(sec)		
	SCHEMATIC	LAYOUT
setup time	3.89E-10	5.52E-10
hold time	2.89E-10	4.79E-10

Table 3 Setup & Hold Time

Here, it is observed that the setup time and hold time of the flipflop at layout level is more than the schematic level.
The minimum capturable pulse width of a proposed flipflop is calculated by using setup time and hold time. The simulated graphs of setup time and hold time calculations and their violation cases are represented in appendices (fig 21- fig 27).

Minimum capturable pulse width = setup time + hold time

At schematic level, Minimum capturable pulse width = 678ps
At layout level, Minimum capturable pulse width = 1.03ns

C.Delay (clk to Q) under different loads:

The below table represents the delay of the proposed schematic and layout of the flipflop under different capacitive loads. The loads are varied from 1pF to 300pF and the delay values are calculated. The delay is increasing as the load increases.

	Delay(clk to Q)(sec)	
Load capacitance(F)	schematic	layout
1.00E-15	4.28E-10	7.62E-10
5.00E-15	4.29E-10	7.88E-10
1.00E-14	4.55E-10	7.90E-10
1.50E-14	4.70E-10	8.37E-10
2.50E-14	4.91E-10	8.85E-10
3.50E-14	5.10E-10	9.43E-10
6.00E-14	5.72E-10	1.09E-09
9.00E-14	6.39E-10	1.20E-09
1.00E-13	6.55E-10	1.30E-09

Table 4 Delay under various loads

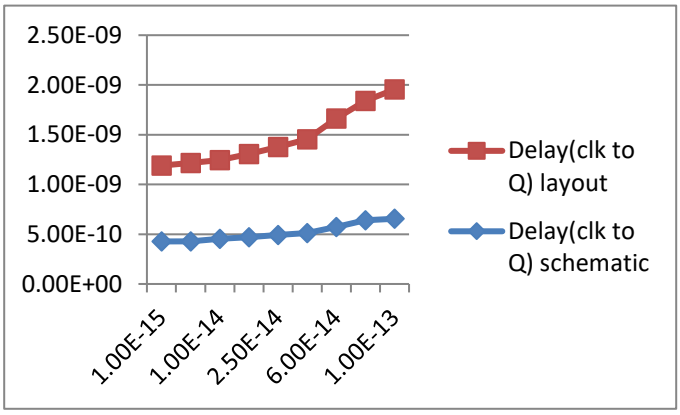

Fig 14 Load Capacitances vs Delay (schematic & layout)

It is also observed from the graph that delay of the flipflop at layout level is more than at schematic level.
The maximum load capacitance that the proposed d-flipflop without undergoing distortions in the output Q was 300pF at schematic level and at layout level it can load up to 100pF.

D.Performance of MSSDF under different supply voltages:

The supply voltage (V_{DD}) of the Flipflop changes and observed the power dissipation and delay. The power dissipation was calculated by finding the current (I_{DD}) from the simulations tools.
Power dissipated = $V_{DD} \times I_{DD}$
The table and graph below represents the power dissipation, delay, current of the flipflop at different supply voltages.

1. Schematic Level

V_{DD}(v)	Delay(sec)	I_{DD}(A)	Power Dissipation(W)
1.7	1.18E-09	6.92E-05	1.18E-04
2.7	5.34E-10	1.14E-04	3.08E-04
3.3	4.22E-10	1.43E-04	4.72E-04
4.3	3.49E-10	2.15E-04	9.26E-04
5.3	2.70E-10	6.30E-04	3.34E-03
5.8	2.50E-10	1.07E-03	6.21E-03

Table 5 performance of MSSDF for Different Voltages

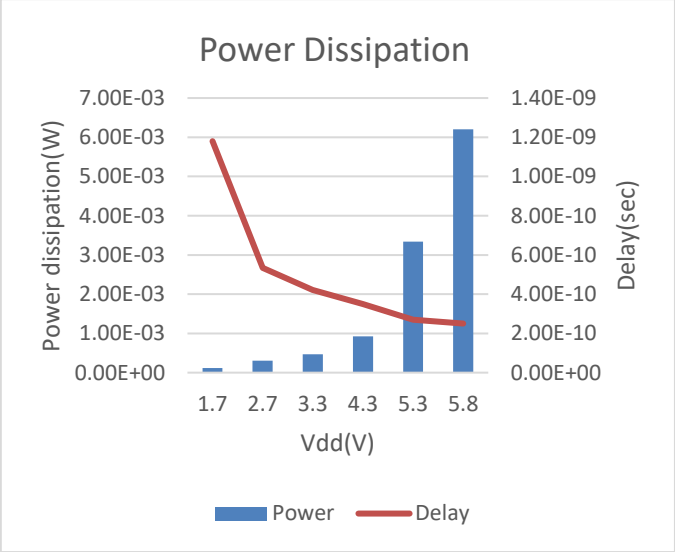

Fig 15 power vs vdd vs Delay of MSSDF

2. Layout Level

V_{dd}(v)	Delay(sec)	Current(A)	Power(W)
1.7	2.40E-09	1.57E-04	2.67E-04
2.7	9.75E-10	2.72E-04	7.34E-04
3.5	7.54E-10	3.40E-04	1.19E-03
4.3	5.59E-10	4.79E-04	2.06E-03
5.3	4.57E-10	9.56E-04	5.07E-03
5.8	4.28E-10	1.42E-03	8.24E-03

Table 6 performances of MSSDF at layout level for various loads

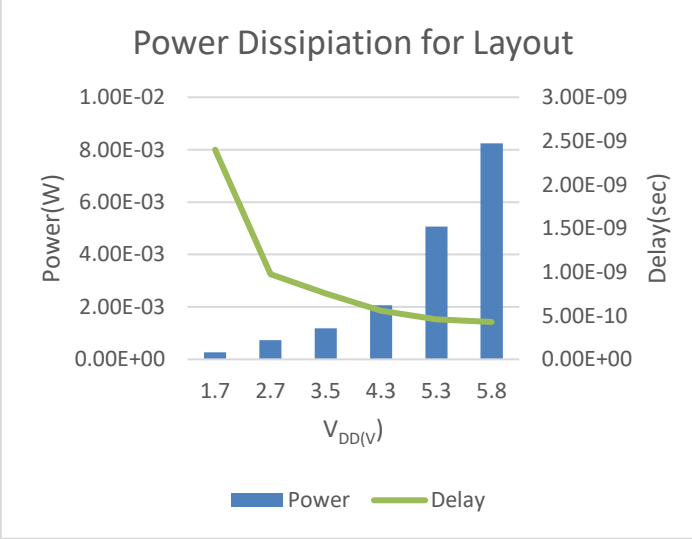

Fig 16 Power Dissipation for the Layout

In both the schematic level the power dissipation increases as the supply voltage increases and the delay decreases. Moreover, it is observed that power dissipation and delay at layout level is more than the schematic level implementation of proposed MSSDF.

3. Performance of MSSDF under different transistor sizes:

At schematic level proposed transistor widths of the PMOS is changed by keeping the NMOS widths constant at 1µm and the delays are calculated and is represented in the below table and the corresponding graphs are drawn.

Pmos Width	Delay(sec)
1.5	4.11E-10
2	4.21E-10
3	4.66E-10
3.5	4.98E-10
4	5.18E-10
5	5.62E-10

Table 7 delay for various transistor width

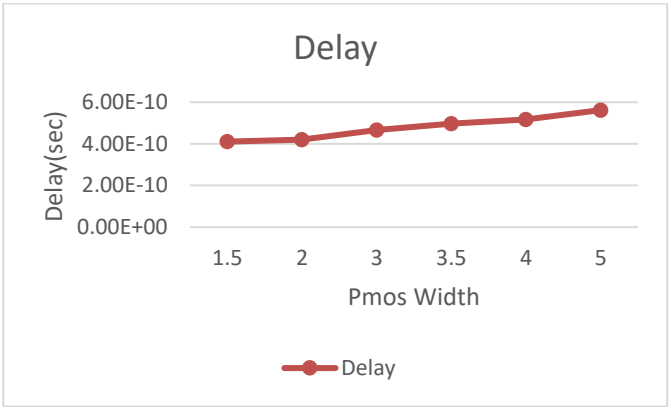

Fig 17 Delay Vs Transistor Width

It is observed that delay increases as the PMOS width increases but it varies from 400ps to 600ps.

VI. IMPORTANT OBSERVATIONS:

The power dissipation and current of proposed flipflop and counter at both schematic level are represented below.

	I_{DD}(A)		POWER DISSIPATION(mW)	
	SCHEMATIC	LAYOUT	SCHEMATIC	LAYOUT
MSSDF	1.43E-04	3.36E-04	0.47	1.11
counter	1.93E-04	3.91E-04	0.638	1.3

Table 8 power dissipation & current of MSSDF & counter

Area of the proposed MSSDF layout =73µm × 301 µm
Area of the proposed Counter using MSSDF
= 94µm × 951 µm
Area per Flipflop in the proposed counter
=31.33µm × 317 µm

VII. CONCLUSION

Hence, the layout and schematic level implementation of MSSDF done successfully by choosing minimum transistor sizes assuming H=1. The input capacitances at the gate inputs are indicated and the maximum load capacitances are calculated for the proposed MSSDF. The analysis part was did by calculating setup time and hold times, power dissipation at different V_{DD}, clock to Q delay at different loading conditions are calculated successfully. Moreover, the simulation results are obtained successfully at schematic-level simulation and post layout simulation. The implementation of the 3-bit Asynchronous counter using proposed MSSDF successfully and the simulation results are obtained. Finally area of the layout of proposed MSSDF and Counter are calculated.

VIII. REFERENCES

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[2] R.Arunya, A. Ramya. (2013, Mar.). Design of Asynchronous up-down using power efficient D-Flipflop. *ISSN2320-6802*.

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IX. APPENDICES

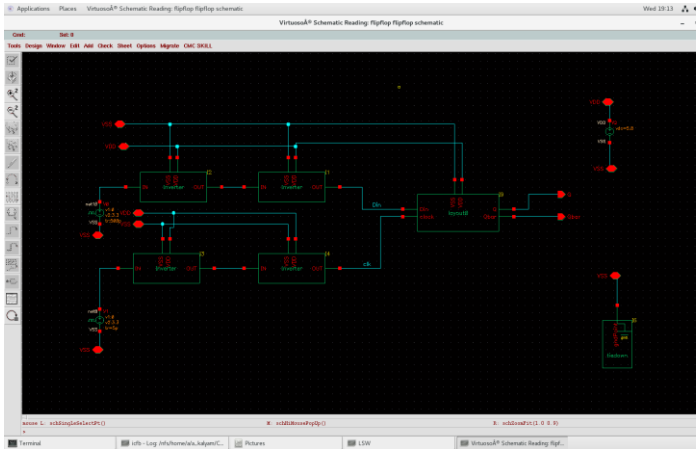

Fig 18 Post Layout Circuit Of MSSDF

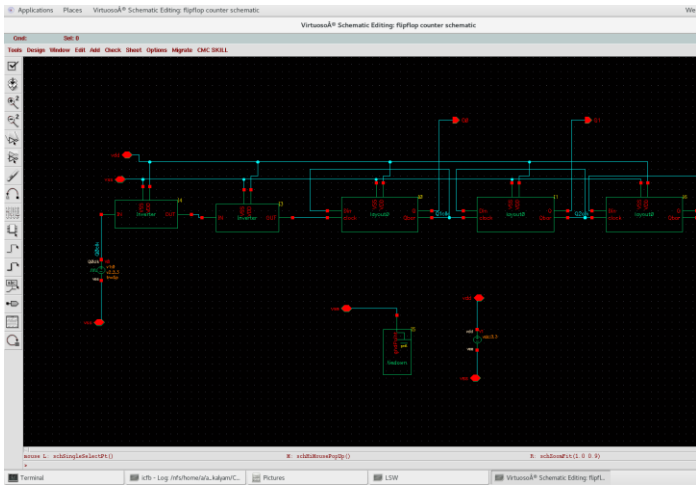

FIG 19 Post Layout Circuit of Counter with MSSDF

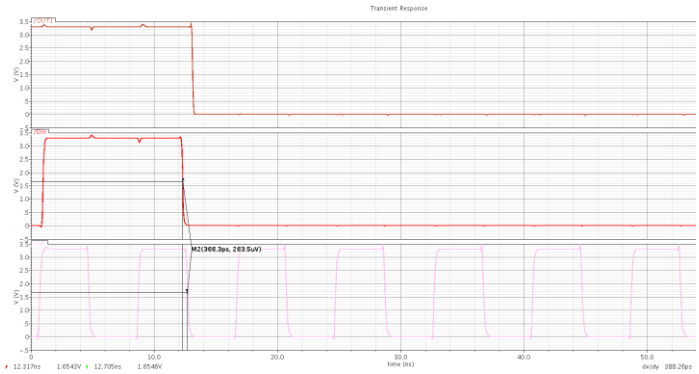

Fig 20 Setup Time of MSSDF at Schematic Level

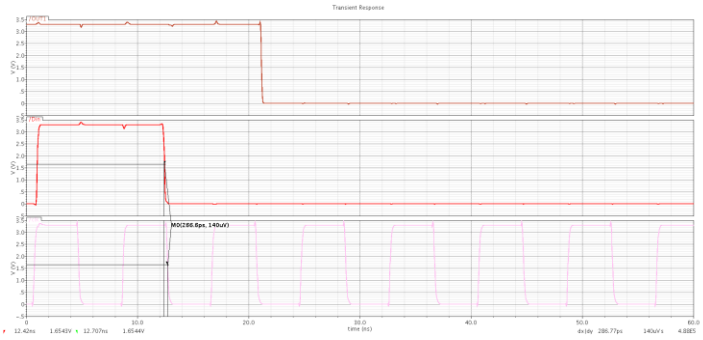

Fig 21 Setup Time Violation of MSSDF at Schematic Level

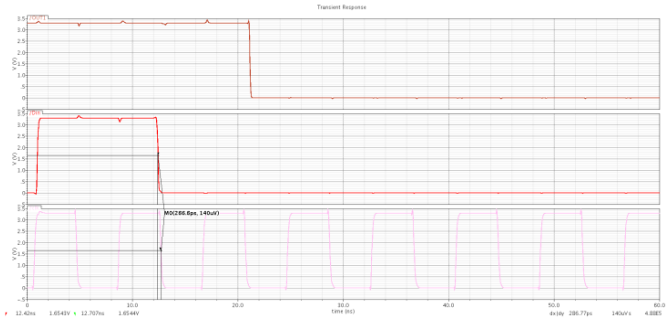

Fig22 Hold Time of MSSDF at Schematic Level

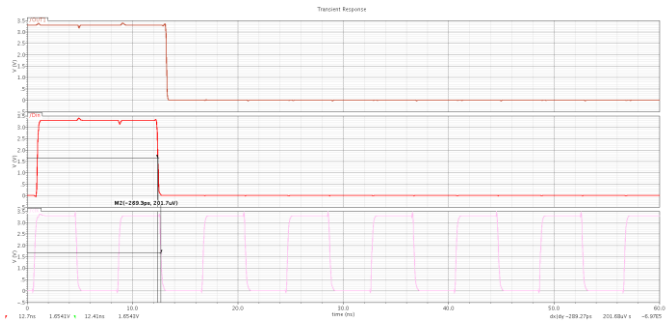

Fig 23 Hold Time Violation of MSSDF at Schematic Level

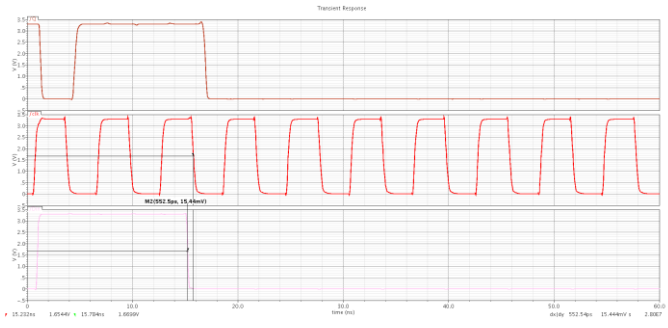

Fig 24 Setup Time of MSSDF at Layout Level

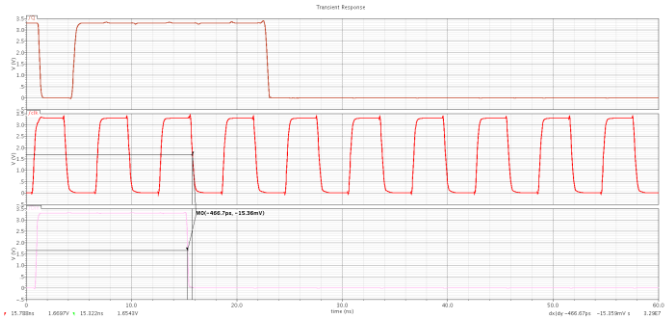

Fig 25 Setup Time Violation of MSSDF at Schematic Level

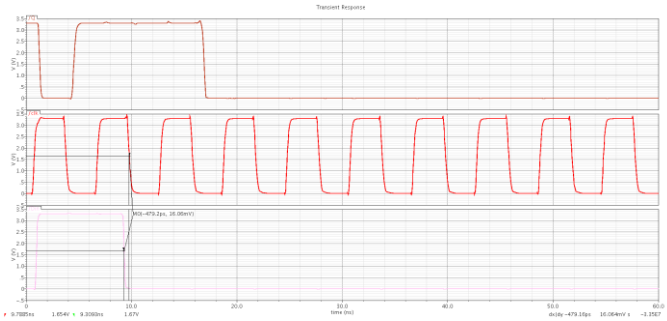

Fig 26 Hold Time of MSSDF at Layout Level

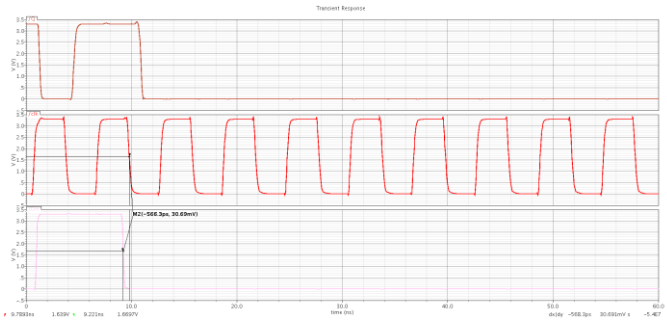

Fig 27 Hold Time Violation of MSSDF at Layout Level

Fig 28 clock parameters of flipflop at schematic level

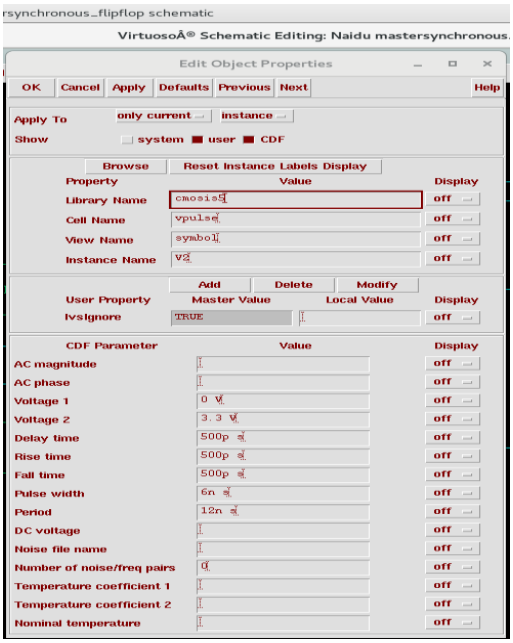

Fig 29 D parameters of flipflop at schematic level

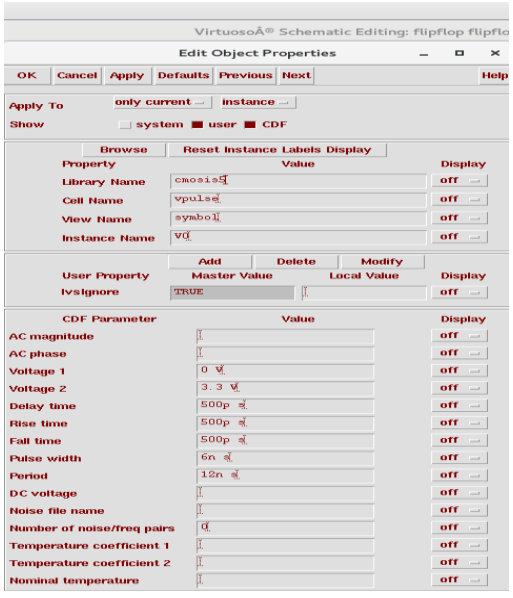

Fig 30 clock parameters of flipflop at layout level

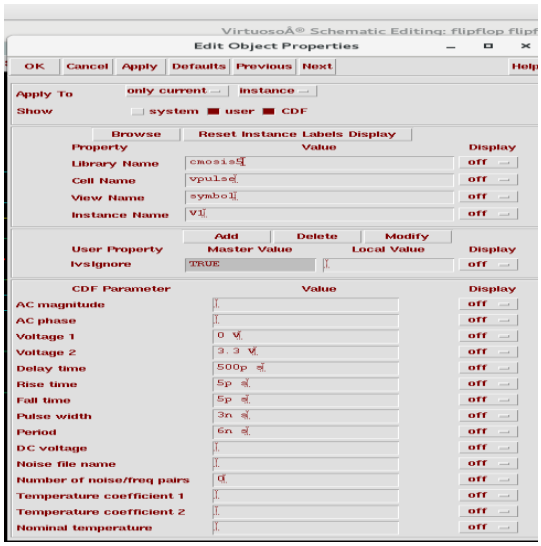

Fig 31 clock parameters of flipflop at layout level

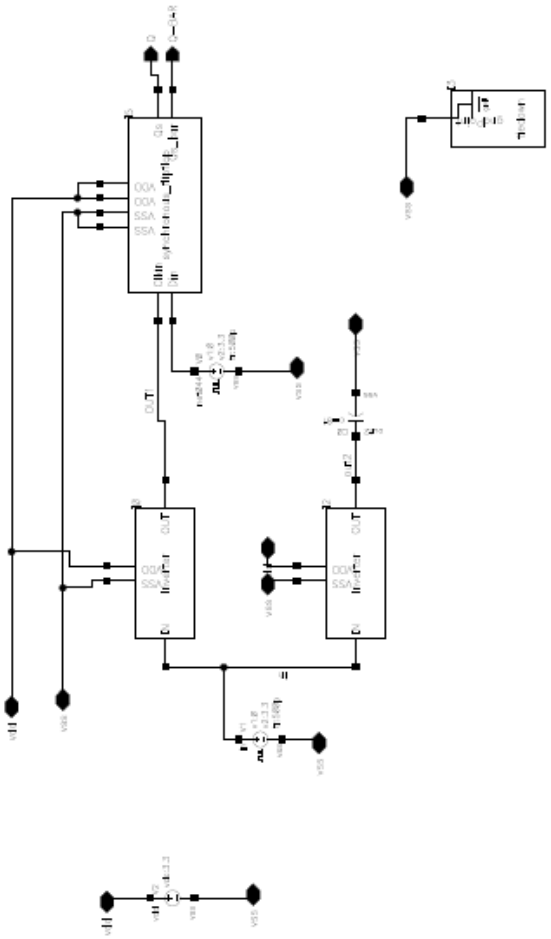

Fig 32 Calculation of input capacitance at clock input for schematic level

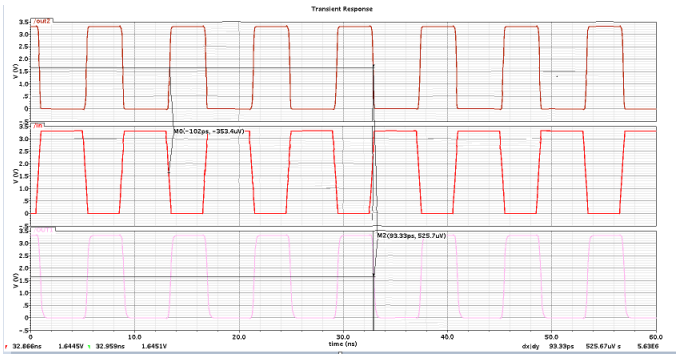

Fig 33 Delay matching of capacitance and MSSDF at the inverter outputs

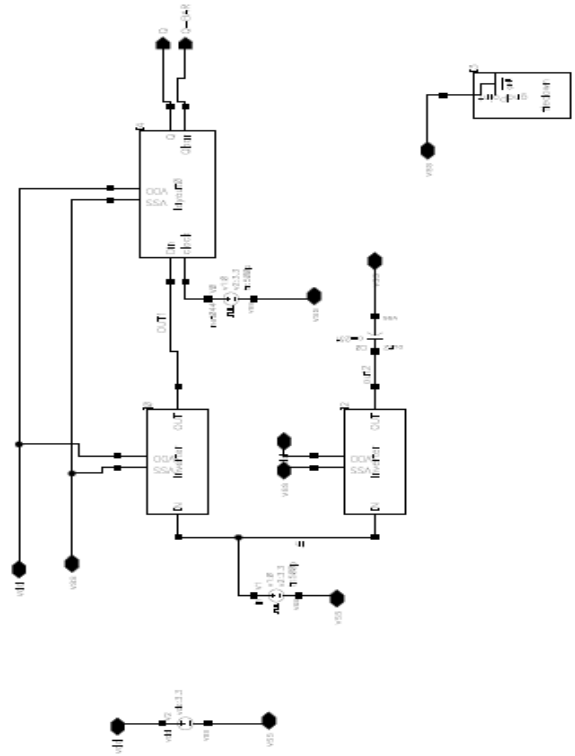

Fig 34 Calculation of input capacitance at D input for post layout circuit.

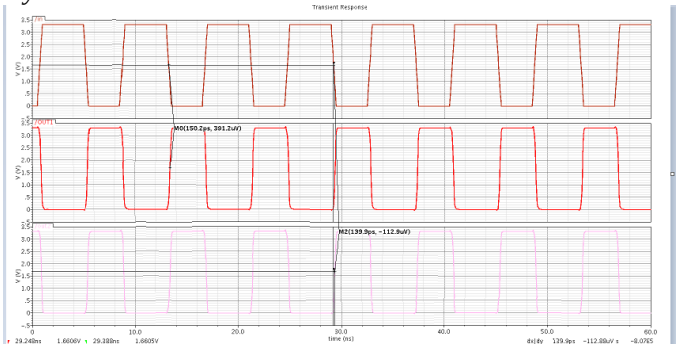

Fig 35 Delay matching of capacitance and MSSDF at the inverter outputs

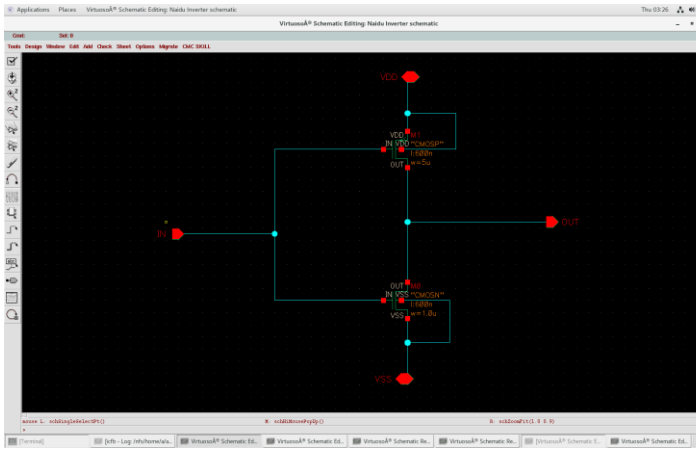

Fig 36 transistor level inverter in schematic level in MSSDF

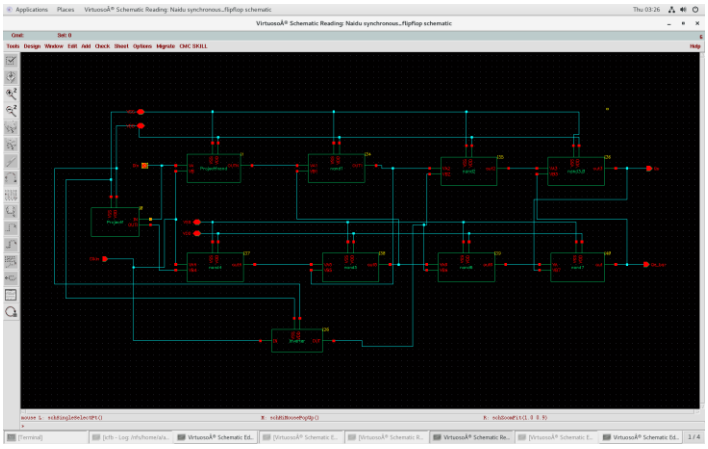

Fig 39 Proposed schematic level of MSSDF

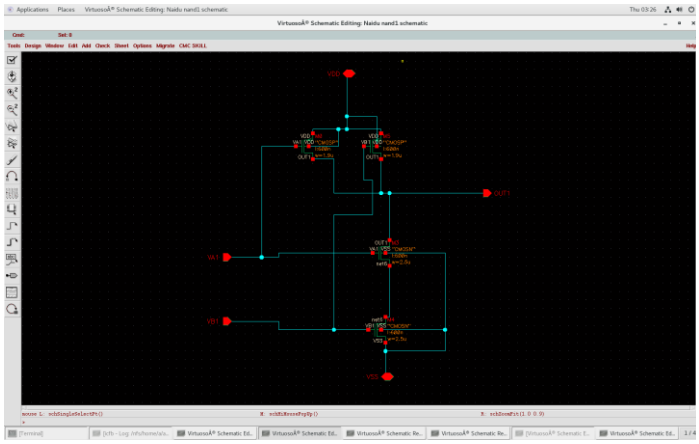

Fig 37 transistor level NAND in schematic level in MSSDF

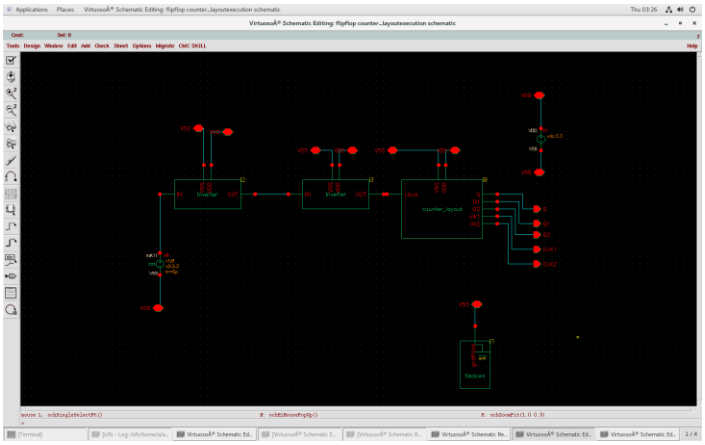

Fig 40 Post layout circuit diagram of 3-bit asynchronous down counter

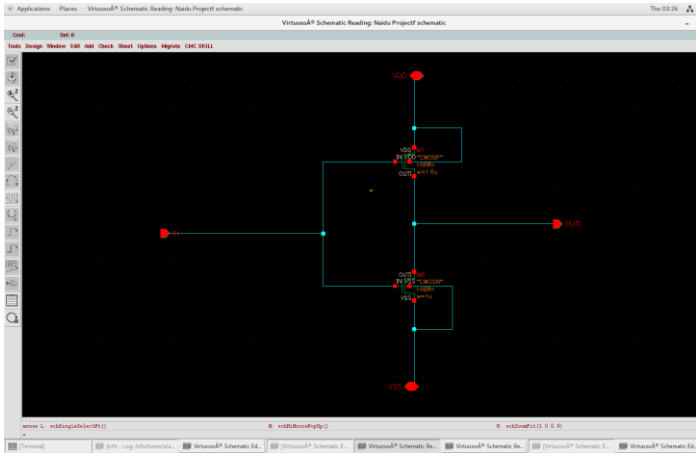

Fig 38 inverter used in buffer and inverting the clock signal

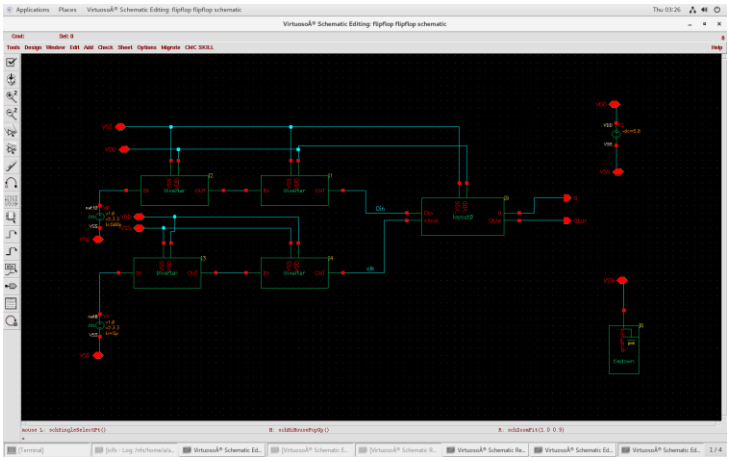

Fig 41 Post layout circuit diagram of MSSDF

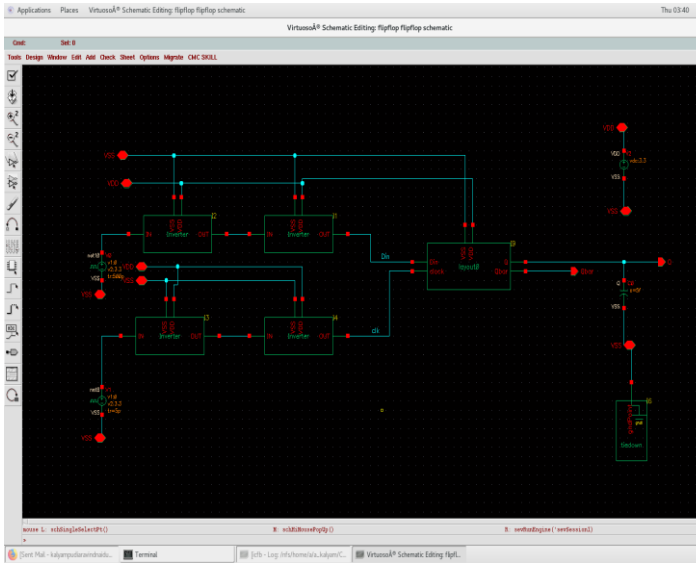

Fig 42 circuit of MSSDF loading at 5pF capacitance.

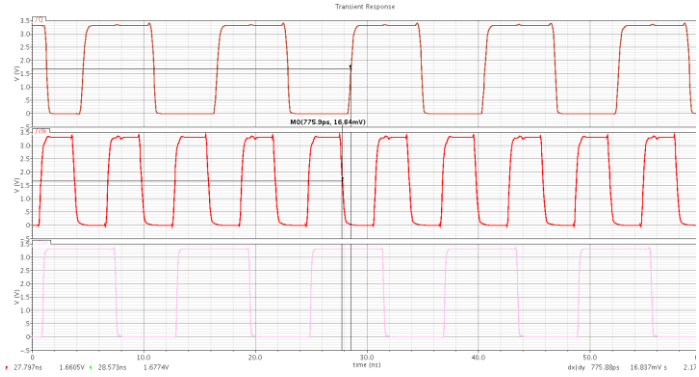

Fig 43 Delay of MSSDF loading at 5pF capacitance