Ministry of Electronics & IT

Government of India is democratizing Chip designing in India: India's semiconductor moment has arrived

Winners Announced: 'Analog & Digital Design Hackathons' (participated by 2,210 teams, 10,040 students)

Boosting Indigenization: M/s Vervesemi Microelectronics Pvt. Ltd. to design BLDC Motor Controller Chip with 90% BOM 'Made in India'

Next Big Leap: Launch of 'Digital India RISC-V (DIR-V) Grand Challenge'

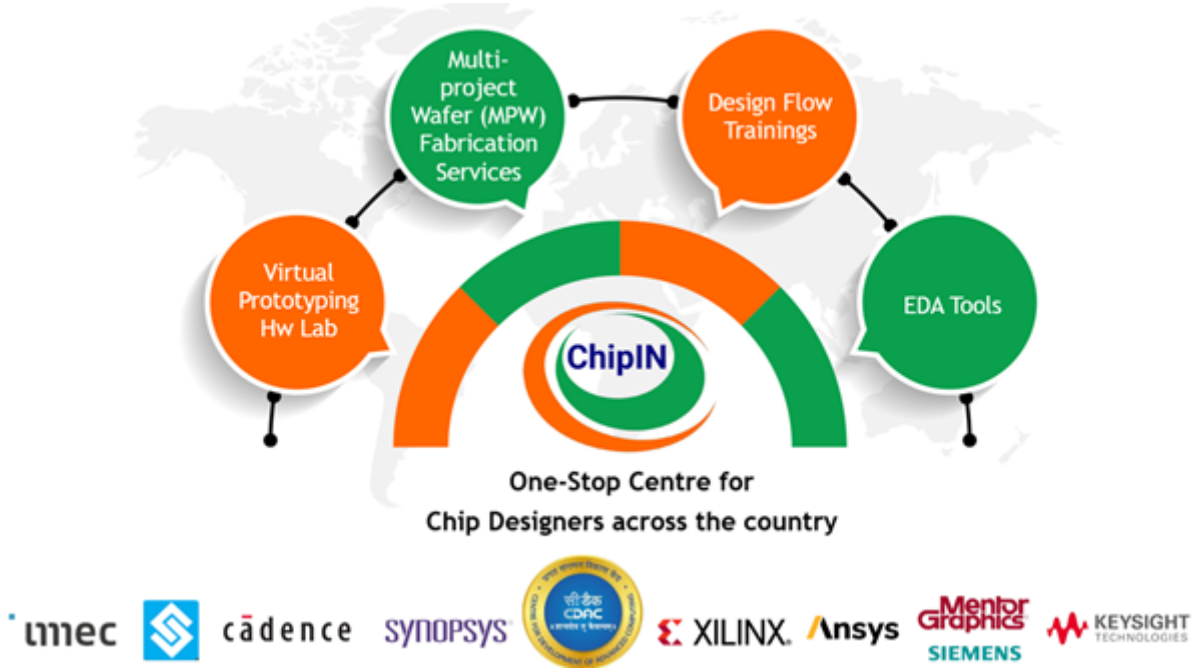
Posted On: 20 MAR 2025 8:05PM by PIB Delhi

Understanding chip design as a strategic necessity, Ministry of Electronics and Information Technology (MeitY) with its series of graded and proactive steps, is in the process of systematic overhaul of semiconductor design approach at 300+ organizations across the country (including 250 academic institutions and 65 start-up companies). These steps aim to debut an era of creative enablement where anyone with innate skills, anywhere in the country can get the semiconductor chips designed. In the process, chip design will be democratized in line with the vision of Hon'blePrime Minister of India Shri Narendra Modi that –'Design in India is as important as Make in India'.

The **C2S Programme** aims to generate 85,000 number of industry-ready manpower at B.Tech, M.Tech, and PhD levels specialized in semiconductor chip design. The Programme takes a comprehensive approach by offering students complete hands-on experience in chip design, fabrication, and testing. This is achieved through regular training sessions, conducted in collaboration with industry partners, and by providing mentorship and access to chip design, fabrication & testing resources to students, including EDA tools, access to semiconductor foundries for fabricating their chips etc. These opportunities include implementing the R&D projects for development of working prototypes of ASICs, SoCs, and IP Core designs.

ChipIN Centre has been setup under C2S Programme as one of the largest facilities established at C-DAC, aims to bring the chip design infrastructure at door-steps of semiconductor design community in the country. It is a centralized design facility, not only hosting the most advanced

tools for entire chip design cycle going up to 5nm or advanced node but also provide aggregate services for fabrication of design at foundries and packaging.



Under C2S Programme, following announcements were made by Hon'ble Minister- Shri Ashwini Vaishnaw with august presence of Secretary- Shri Krishnan, Additional Secretary- Shri Abhishek Singh and Group Coordinator- Smt Sunita Verma, MeitY on 20th March 2025.

i. After intense rounds of coding, design challenges, and expert-led training, 40 elite teams, 200 innovators battled it out in the Grand Finale of the 100-hour deep-tech "Analog and Digital Hackathons" launched in partnership of AMD, Synopsys and CoreEL Technologies. Armed with EDA & cloud resources, they tackled real-world problems—enhancing LIVE image processing on FPGA hardware in Digital Design and optimizing complex voltage regulator circuits in Analog Design. Six winning teams were announced by Hon'ble Minister:

Winners of the Analog Design Hackathon:

i. 1st Prize winner to the Team Intuition from IIT Delhi.
ii. 2nd Prize Winner to Team Analog Edge from NIT Rourkela.
iii. 3rd Prize Winner to Team FETManiacs from IIT Guwahati.

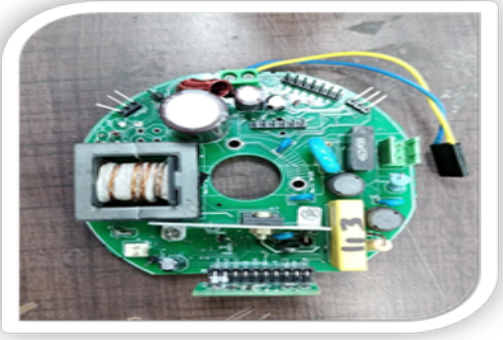
Winners of the Digital Design Hackathon:

i. 1st Prize winner to the Team RISCB from IIT Bombay.
ii. 2nd Prize Winner to Team Silicon Scripters from Saveetha Engineering College.
iii. 3rd Prize Winner to Team Daedalus from IIT (BHU Varanasi).

ii. The indigenous development of the 'BLDC Controller Chip' was awarded to M/s Vervesemi Microelectronics Pvt. Ltd.

This ‘BLDC Controller Chip’ has the following USP: 90% BOM made in India for self-reliant semiconductor solution, Complete power & control solution under $1.50 and Scalability at 10 million units/year.

Vervesemi is a fabless semiconductor company incorporated in 2017 and developing high performance ASICs for sensors and wireless, exploiting the expertise of state-of-art data converters and differentiated Analog IP. The ICs of VerveSemi has been taped out on 8nm, 22nm, 28nm, 40nm, 55nm, 90nm, 180nm, 110nm node of Samsung, UMC, TSMC, SMIC PSMC.



Supporting BLDC and SR motors <200W

iii. The launch of 'Digital India RISC-V (DIR-V) Grand Challenge' was announced – to start inviting applications from 10th April onwards. With VEGA Processors and SHAKTI Microprocessor at its core - the participants of DIR-V Grand Challenge will tinker innovative applications using them. The DIR-V Grand Challenge is technologically powered by VEGA Processor from C-DAC & SHAKTI Processor from IIT Madras with support from Renesas, LTSC, CoreEL Technologies and Bharat Electronics. MakerVillage will provide the coordination and incubation support.

While addressing the gathering, Hon'ble Minister Shri Ashwini Vaishnaw stated that we must all collectively adopt three approaches for India to become a product nation.

i. "While the country has made significant achievements in the service industry and it continues to grow, it must now become a product nation. Today's announcements on developing software & hardware products are a few successful steps toward that goal."
ii. These solutions should come from a broader category of stakeholders, involving partnerships across all tiers of academia, start-ups, students, and researchers, rather than just a select few.
iii. The incremental yet progressive approach needs to be ensured to achieve these solutions. Some chips may have low value but high deployment potential, while others may have high value but limited deployment potential. The entire spectrum should be targeted. While the BLDC Controller chip development announced today has significant volume deployment potential, RISC-V, being open-source, holds very high-value due to its use in designing CPUs, GPUs, and sustainable products for the country.

India today presents a significant opportunity for aspiring entrepreneurs and researchers to be at the forefront of designing and redefining the semiconductor systems, devices and products of the future. "Chips to Start-up (C2S) Programme" of Government of India and MeitY in alignment with the nation's unwavering commitment to building a robust and self-sustaining semiconductor ecosystem, is empowering the next generation of engineers, researchers and entrepreneurs to drive India's technological advancements and propel the nation towards becoming a global powerhouse.

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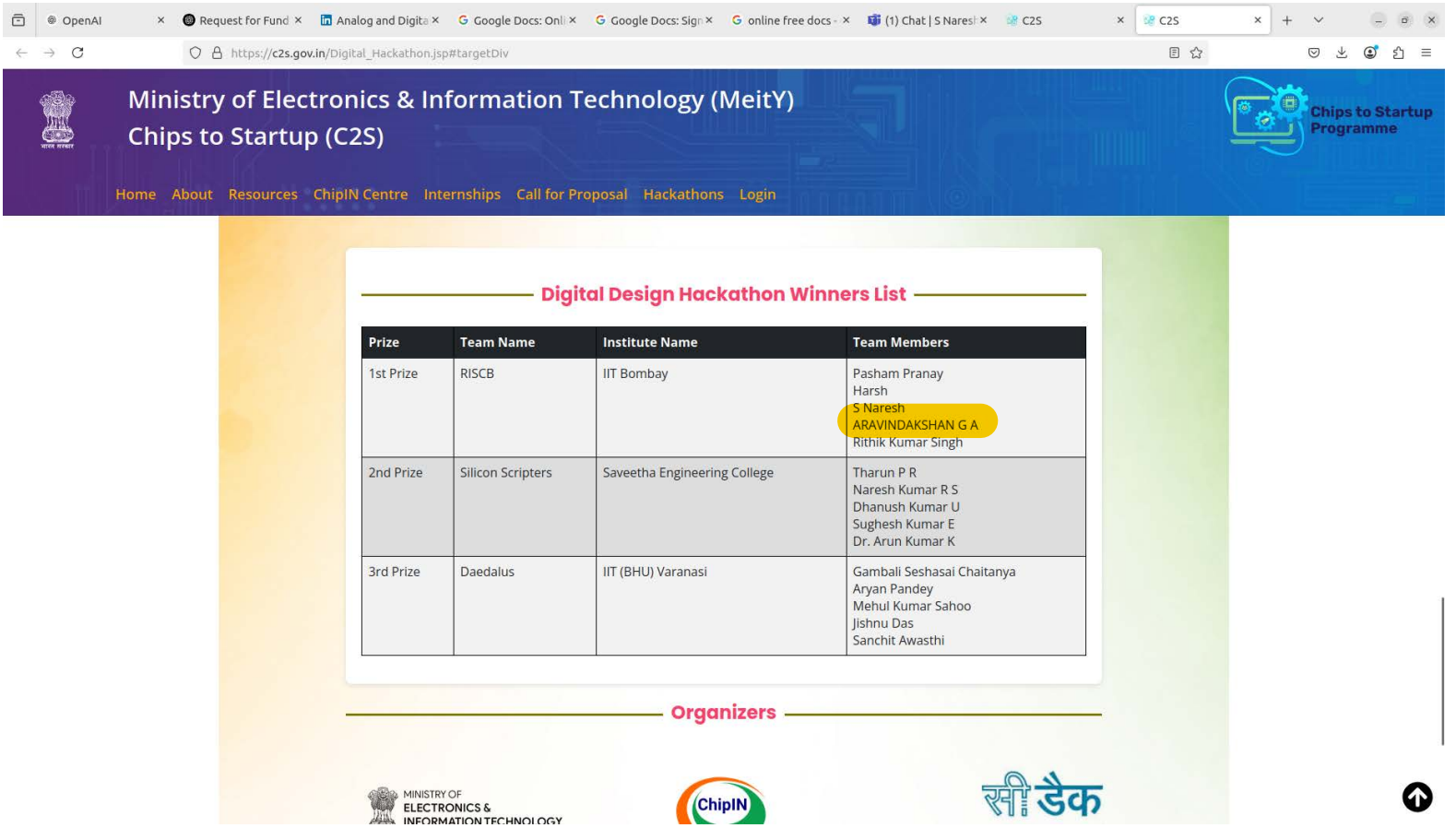
Dharmendra Tewari/ Navin Sreejith



WEBSITE LINK:

https://c2s.gov.in/Digital_Hackathon.jsp

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IIT Bombay

Date: 05/03/2025

No-Objection Certificate for Analog/Digital Hackathon under C2S Programme.

This is to certify that the students mentioned below are Bonafide students of the Department of Electrical Engineering, IIT Bombay.

Name	Roll Number	Branch
Mr. Pasham Pranay	23M1123	Integrated Circuit and Systems, Electrical Engineering
Mr. S Naresh	23M1200	Electronic Systems, Electrical Engineering
Mr. Harsh	23M1214	Electronic Systems, Electrical Engineering
Mr. Rithik Kumar Singh	22M1171	Integrated Circuit and Systems, Electrical Engineering
Mr. Aravindakshan G A	23M1188	Integrated Circuit and Systems, Electrical Engineering

The Electrical Engineering Department has no objection to the above-mentioned participation in the Hackathon organized by ChipIN Centre (C-DAC Bangalore), under the C2S Programme, funded by the Ministry of Electronics and Information Technology (MeitY), Govt. of India, scheduled to be held from **15th to 20th March** in Bangalore, Karnataka.

5/3/25

(Signature and Seal)

PROFESSOR & HEAD
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