Unit: 1:

MOS TRANSISTOR PRINCIPLES

VLSI

⇒ VLSI (Very large scale integration) is the process of creating and integrated circuits (IC) by combining thousands of transistors into a single chip.

⇒ Integrated circuit (IC) is developed which incorporated all the passive (Resistors, capacitors, Inductors) and active (Transistors) components on to a single chip.

Need for integration:

1) To reduce the size of the device.

2) To improve the speed.

3) This integration is classified based on the number of components or transistors to be integrated

on a single silicon chip.

1) SSI (Small scale Integration).

SSI have less than 10 gates or no. of transistors are less than 50.

Eg: (Gates → NAD, NOR etc)

2) MSI (Medium Scale Integration)

MSI systems have upto 50 - 500 Gates in one package or chip and No. of transistors. (100-1000).

Eg: (counters, Shift Registers, amplifiers, 4 bit microprocessor)

3) LSI (large Scale Integration)

LSI Systems have upto 1000 - 10,000 transistors integrated on a single chip

Eg: (RAM, ROM, 8 bit microprocessors)

4) VLSI (Very large Scale Integration)

VLSI Systems incorporate incorporate 10,000 to 1 million transistors in a single package.

Eg: (16 bit and 32 bit microprocessors)

5) ULSI (ultra large scale Integration)

In ULSI 1 million to 10 million transistors can be incorporated in a single package.

Eg: (Smart Sensor, Virtual reality machines)

6) GSI (Giant scale Integration)

More than 10 million transistors can be incorporated in this GSI systems.

Eg: ("Embedded" system)

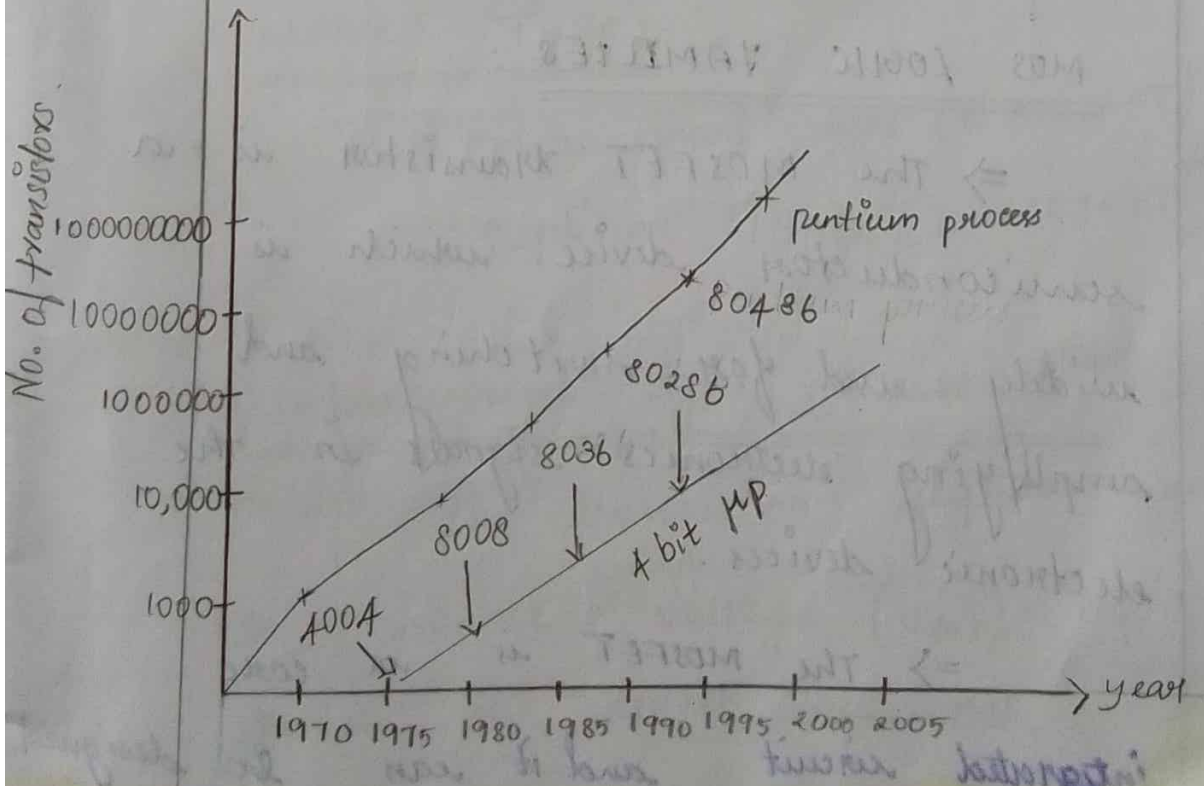
VLSI

VLSI is a technology in which 1 million transistors can be fabricated on a single chip.

Moore's law :

In 1965, "Gordon Moore" predicted that the no. of transistor on a chip double's every "18 to 24 months" this law is used in semiconductor industry to guide long term planning and to set targets for research.

Due to increase in no. of transistors the process speed also increase from 740KHz to 8MHz in 1970's from 2000-2009, the speed further increased from 1.3GHz to 2.8 GHz whereas the no. of transistor range ~~from~~ btw 37.5 million to 904 million.



Advantages of VLSI :

⇒ Reduce the size of circuit

⇒ Less expensive

⇒ Increase in operating speed.

⇒ Less power consumption.

⇒ More reliability

⇒ Occupies relatively smaller area

Applications of VLSI :

⇒ Computers

⇒ Automobiles

⇒ Voice and data communication

⇒ Digital signal processing

⇒ Industry automation.

MOS LOGIC FAMILIES :

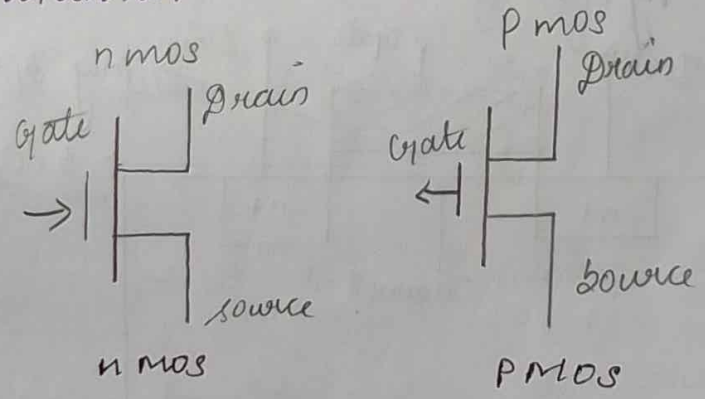
⇒ The MOSFET transistor is a semiconductor device which is widely used for switching and amplifying electronics signals in the electronic devices.

⇒ The MOSFET is a core integrated circuit and it can be designed

and fabricated in a single chip because of this very small sizes.

=> The MOSFET is a four terminal device with Source (S), Drain (D), Gate (G), Substrate (S).

=> MOS transistor is called a majority carrier device. The majority carrier of an nmos transistor or an electrons. The majority carrier are p mos transistor or an holes.



MOSFET TYPES :

1) Enhancement type (E MOSFET)
2) Depletion Type (D-MOSFET)

1) Enhancement type (E MOSFET)

The transistor requires gate to source voltage (V_{GS}) to switch the device into ON.

2) Depletion Type (D-MOSFET)

The transistor requires the gate to source voltage (V_{GS}) to switch the device into OFF.

1) nMOS Transistor

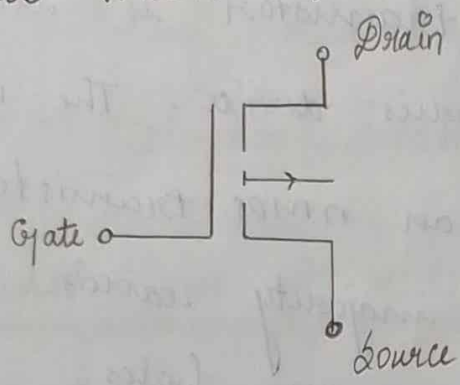


fig : n mos

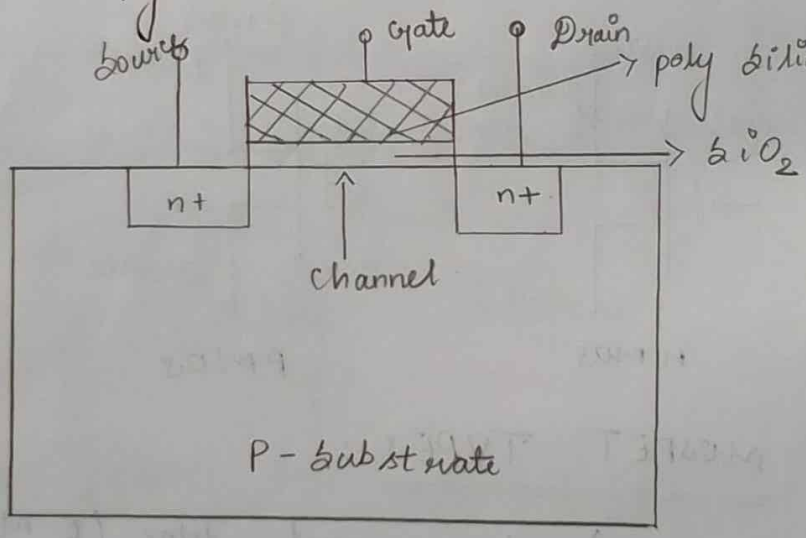


fig : NMOS Transistor

⇒ In nMOS Transistor, an n channel is formed on a p-type substrate of moderate dopping levels.

⇒ The source and drain regions

are made up heavily dopped n^+ type material to form depletion region.

⇒ These two diffusion regions are connected via metal to the external conductors.

⇒ The region between two diffused regions under oxide layer is called channel.

⇒ This channel provides a path for the majority carriers (in electrons) to flow between the source and Drain.

⇒ A thin insulating layer of SiO_2 is deposited over the channel.

TWO modes:

1) ENHANCEMENT mode
2) DEPLETION mode.

1) Enhancement mode:

i) $V_{GS} = 0$ (Gate to Source Voltage)

Current will not flow from Source to

drain at $V_{GS} = 0$.

2) V_{GS} is positive :

When Gate is applied with positive voltage relative to source, this electric field in turn attracts the electrons towards gate and repells the holes. So more number of current flow between source to drain.

3) V_{GS} is Negative :

When a negative voltage is applied to the gate, it attracts the positive charged holes to the region below the gate. So small amount of current flow between source to drain.

2) Depletion mode :

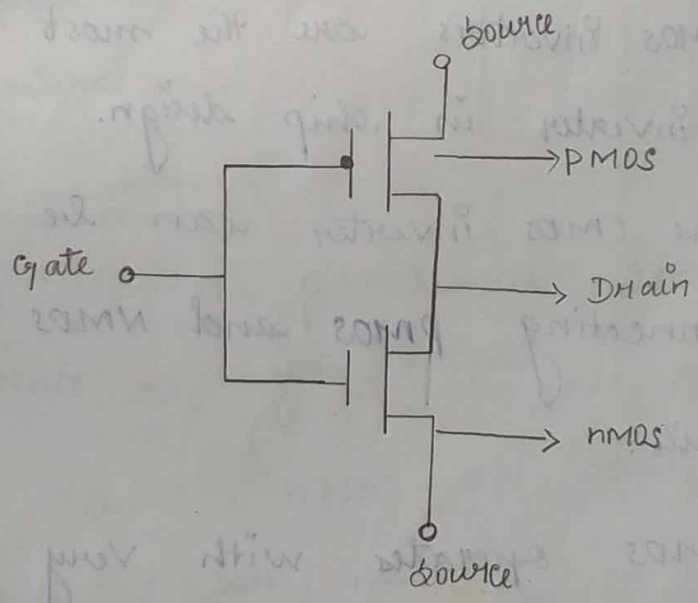
A negative voltage makes the device "depleted OFF" of the charge carriers. This is called depletion mode.

CMOS (complementary MOSFET)

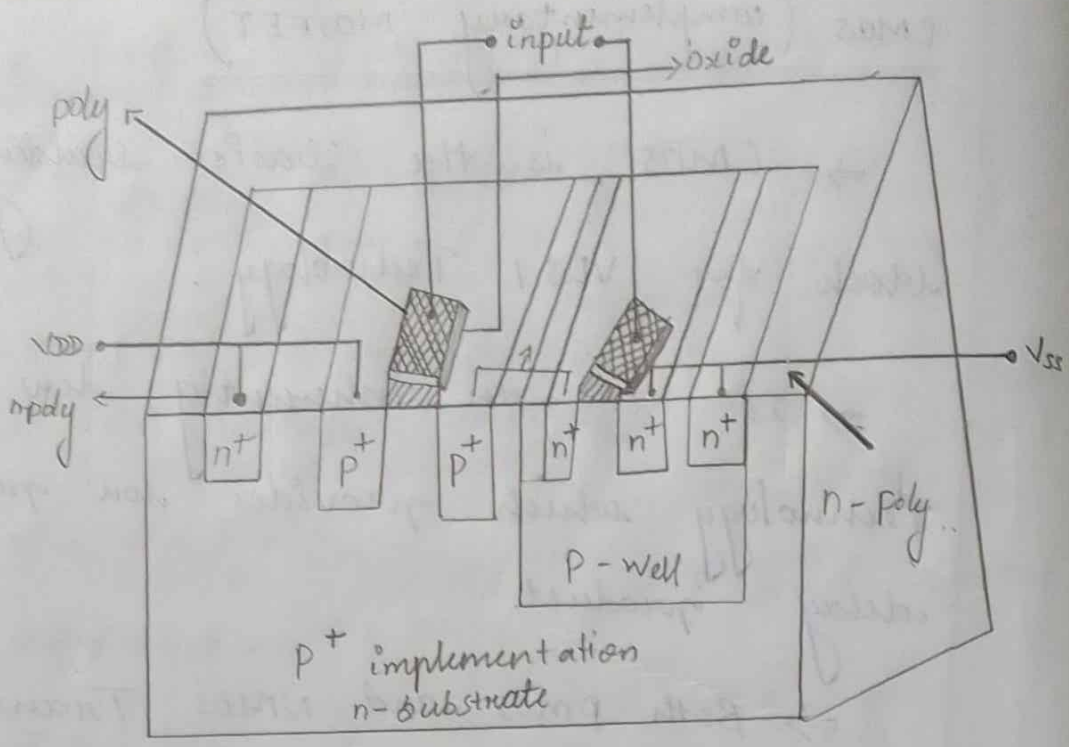
⇒ CMOS is the basic building block for VLSI Technology.

⇒ It is an inherently low power Technology which provides low power delay product.

⇒ Both PMOS and NMOS Transistors are combined to form CMOS Transistor.



CMOS



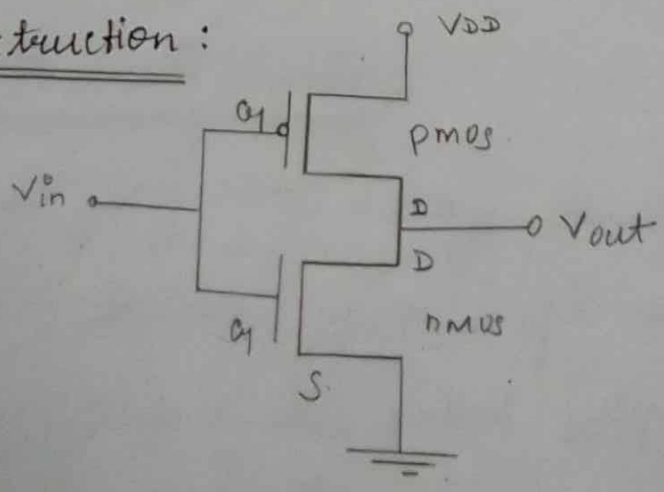
CMOS inverter

⇒ CMOS inverters are the most widely used inverter in chip design.

⇒ The CMOS inverter can be obtained by connecting PMOS and NMOS transistors in series.

⇒ CMOS operates with very little power and higher speed.

construction :



⇒ The PMOS and NMOS transistors are connected by the drain terminal

⇒ The supply voltage V_{DD} is given at the source of the PMOS transistors. and ground is connected at nMOS source

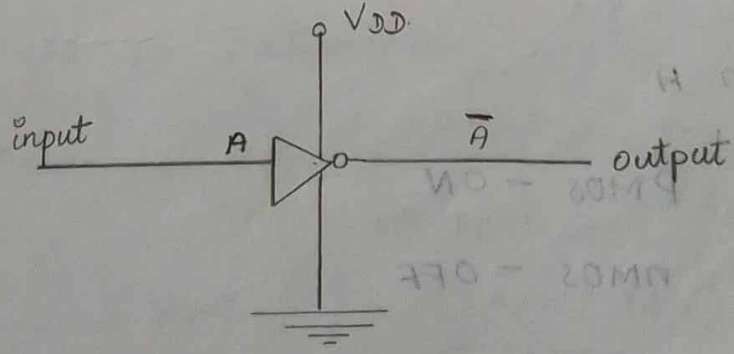
⇒ The input voltage is applied at the gate terminals of PMOS and nMOS transistor. and the output voltage is taken from the interconnected drain terminal.

Operation:

$V_{in} = 0$, nMOS = OFF state, PMOS => ON state => high output.

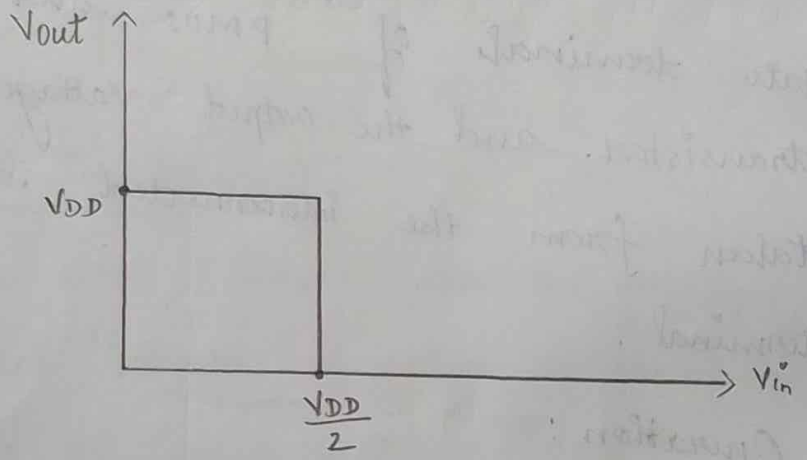
$V_{in} = 1$, nMOS = ON state, PMOS => OFF state => low output.

Logic Symbol:

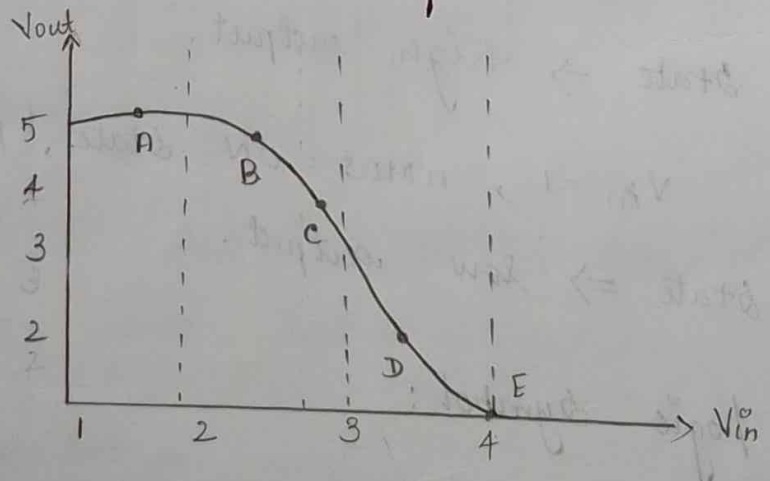


$V_{in}=0$	NMOS OFF	PMOS ON	$V_{out}=1$
$V_{in}=1$	NMOS ON	PMOS OFF	$V_{out}=0$

DC characteristics :



Actual characteristics of an inverter :



Region A

PMOS – ON

nMOS – OFF

nMOS → cut off Region

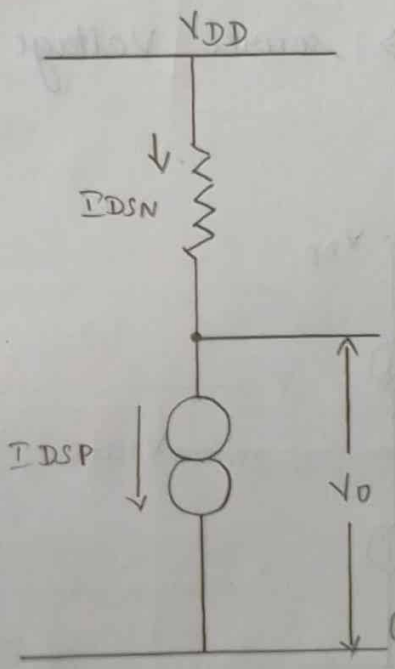
PMOS → Non saturated region

$I_{dsn} = 0$

$I_{dsp} = I_{dsn}$

$\boxed{V_{out} = V_{DD}}$

Region B



IDSN → source to drain current at nMOS

IDSP → source to drain current at PMOS

PMOS → ON

nMOS → ON

nMOS → Saturation region

PMOS → Non-Saturation Region

$$I_{DSN} = \beta_n \frac{(V_{gsn} - V_{tn})^2}{2}$$

$$I_{DSP} = -\beta_p \left[(V_{gsp} - V_{tp}) V_{dsp} - \frac{V_{dsp}^2}{2} \right]$$

V_{gsn} → Gate to source voltage at nMOS

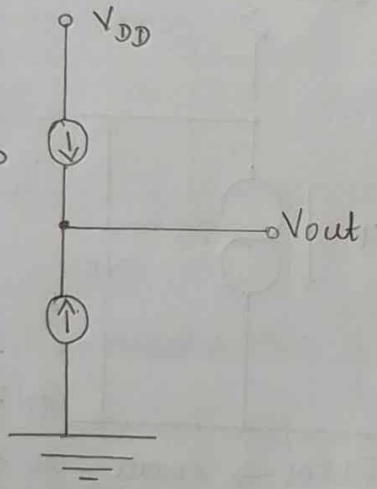
V_{tn} → Threshold voltage at nmos

V_{gsp} → gate to source voltage at PMOS

V_{tp} → Threshold voltage at PMOS

V_{dsp} → source voltage at PMOS

Region C :



I_{DP} → Drain current at PMOS

I_{Dn} → Drain current at nmos

PMOS → ON

nMOS → ON

Pmos → Saturation region

nmos → Saturation Region.

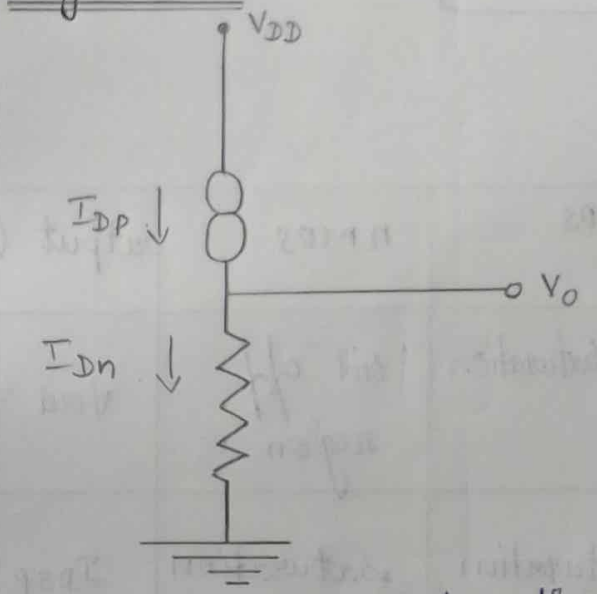
$$I_{Dsn} = \frac{\beta_n (V_{in} - V_{tn})^2}{2}$$

$$I_{DSP} = \frac{\beta_P (V_{in} - V_{DD} - V_{tp})^2}{2}$$

$\beta_n \rightarrow$ Gain of nMOS

$\beta_P \rightarrow$ Gain of PMOS

Region - D



nMOS $\rightarrow$ Non saturation Region

PMOS $\rightarrow$ saturation Region

PMOS $\rightarrow$ OFF

nMOS $\rightarrow$ ON

$$I_{DSP} = \frac{-\beta_P (V_{in} - V_{DD} - V_{tp})^2}{2}$$

$$I_{Dsn} = \beta_n \left[(V_{in} - V_{tn}) V_{out} - \frac{V_{out}}{2} \right]^2$$

Region E :

PMOS – OFF

nMOS – ON

nMOS – Non Saturation Region

PMOS – cut off Region

$I_{DSP} = 0$

$V_{out} = 0$

Region	PMOS	nMOS	output (V_o)
A	Non-saturation	cut off region	$V_{out} = V_{DD}$
B	Non saturation region	saturation region	$I_{DSP} = -\beta_P\left[(V_{gsp} - V_{tp})V_{dsp} - \frac{V_{dsp}^2}{2}\right]$ $I_{Dsn} = \frac{\beta_n (V_{in} - V_{tn})^2}{2}$
C	saturation region	saturation region	V_{out} is not the function.
D	saturation	non saturation	$V_{out} = \frac{(V_{in} - V_{tn}) - \sqrt{(V_{in} - V_{tn})^2 - \frac{\beta_P}{\beta_n}(V_{in} - V_{DD} - V_{tp})}}{2}$
E	cut off region	Non saturation region	$V_{out} = 0$