

STEP 3: RTL DESIGN

The output of HLS tool is called Register Transfer Level (RTL) circuit because data flow, date operations and control flow are captured between registers.

STEP 4: LOGIC SYNTHESIS

After HLS, RTL circuits are transformed into logic gate level implementation. This is called logic synthesis. Initially, we have to verify whether the RTL is, equivalent to the specifications, then logic synthesis is performed by CAD tools.

STEP 5: PHYSICAL LAYOUT

Once the logic level output of the circuit is obtained, we move to back end phase of design process. The placement of gates, flip-flops etc., in appropriate places in the software representation of the chip is called floor plan.

Exact locations in the die where the circuit components are placed is called placement.

The interconnections among the gates that are placed in exact positions in the die are called routing.

STEP 6: TEST PLANNING

In VLSI design, millions of transistors are packed into a single chip which may lead to manufacturing defects. So all the chips should be physically tested.

If the testing is based on structure of the circuit, then it is called structural testing.

STEP 7: FABRICATION, TEST AND MARKETING

Once all the steps are completed, verification is done after each level of transformation. Then the chips are fabricated, physically tested and fault free chips are sent for marketing.

5.3. APPLICATION SPECIFIC INTEGRATED CIRCUITS (ASICS)

An Application Specific Integrated Circuits (ASIC) is an integrated circuit designed for performing particular operation, instead of general-purpose operation.

- ❖ ASIC is not generally software programmable to perform a wide variety of different tasks.

- ❖ An ASIC will have an embedded CPU to manage suitable tasks. An ASIC may be implemented as an FPGA. It may be considered separately or implemented hybrid with programmable logic and application specific blocks.
- ❖ ASIC can also be implemented using platform such as system on chip.

Table 5.3. Comparison of General purpose IC & ASIC

S.NO.	General Purpose IC	ASIC
1.	Programmable microprocessors ❖ Intel Pentium series, Motorola	Video processor to decode or encode digital TU signals.
2.	PCs, Washing machines	Low power dedicated DSP controller, convergence device for mobiles
3.	Programmable DSPs	Encryption processor for security
4.	Multimedia, sensor processing, communications	Graphics chips
5.	Memory (DRAM, SRAM)	Network processor for packets, traffic management

Application Specific Standard Products (ASSPs) are intermediate between ASICs and standard products. The maximum complexity has grown from 5000 gates to over 100 million.

Modern ASICs often include 32-bit processors, memory blocks such as ROM, RAM, EEPROM, flash memory. Such an ASIC is called as System On Chip (SOC). Hardware Description Language (HDL) such as Verilog or VHDL is used for implementing ASICs.

5.3.1. TYPES OF ASICS

ICs are made on a thin silicon wafer, with each wafer having hundreds of dice. The transistors and wiring are made from many layers built on top of one another. Each successive mask layer has a pattern defined by a mask similar to a glass photographic slide.

The first layers defines the transistors and the last layers defines the metal wires between the transistors (Interconnect)

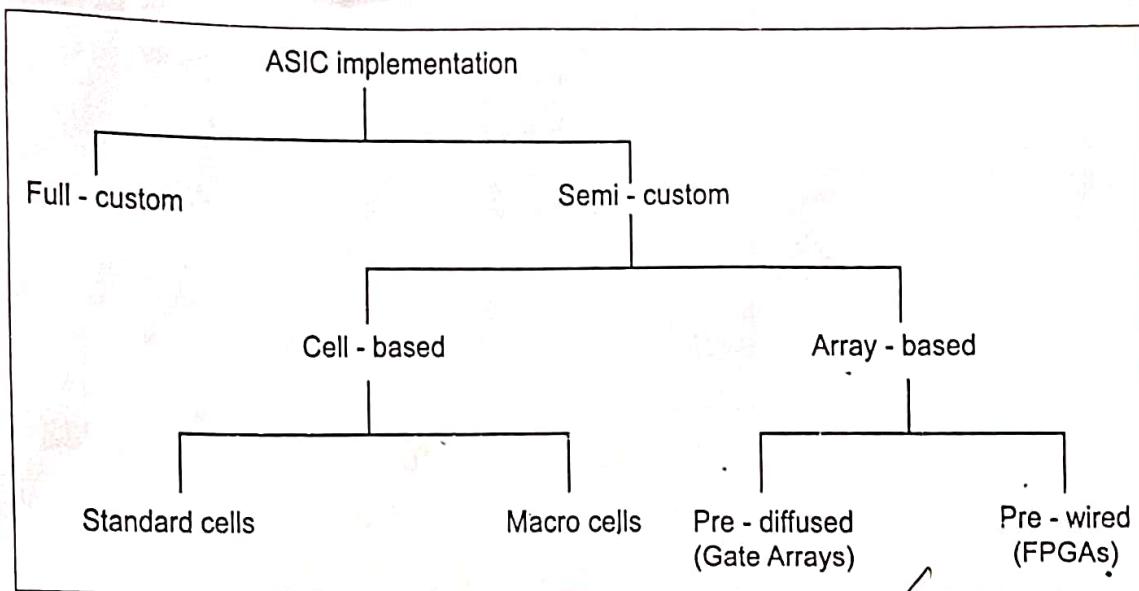


Fig. 5.4. Types of ASICS

5.3.2. FULL-CUSTOM ASICS

A full custom ASIC has logic cells and all mask layers customized.

Example: Microprocessor designers get the solutions for their problems by writing suitable codes by hand.

- ❖ The analog circuits, optimized memory cells, mechanical structures may be included in this design.
- ❖ The predesigned or pretested cells cannot be used in this design. i.e., If suitable existing cell libraries are not available, then we can use the full custom design. The existing cell libraries have less speed, and consume more power.
- ❖ Bipolar technology is used for precision analog function because of the following reasons.
 1. The matching of component characteristics between chips is very poor whereas the matching of characteristics between components on the same chip is excellent.
 2. ICs are made in batches called wafer lots. i.e., A wafer lot is a group of silicon wafers processed together. There are between 3 and 5 wafers in a lot with each wafer having 10s or 100s of chips depending on the size of the IC and wafer.

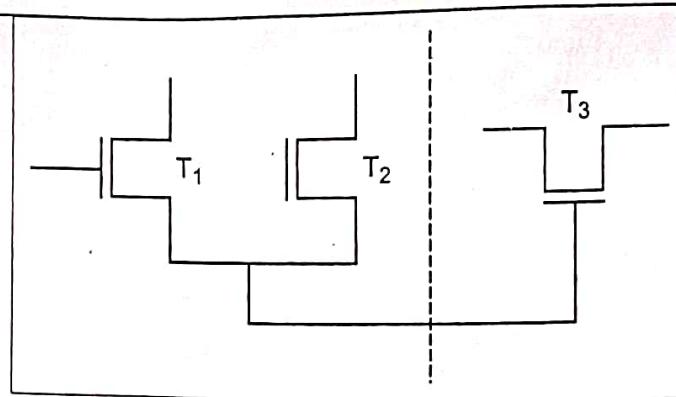


Fig. 5.5. Transistors in an IC

Consider the transistors T₁, T₂, T₃ as shown in Figure 5.5, T₁ and T₂ are adjacent to each other and have same orientation T₃ is also of same size as T₁ and T₂ but located on other side of chip with different orientation. The following observations are made during measurements.

- ❖ T₁ have virtually identical characteristics to T₂ on the same IC. T₁ and T₂ have excellent matching.
 - ❖ T₃ will match T₁ and T₂ on the same IC, but matching is less than the matching between T₁ and T₂
 - ❖ T₁, T₂, T₃ will match fairly with transistors T₁, T₂, T₃ on a different IC on the same wafer. The matching depends on the distance between 2ICs on the wafer.
 - ❖ Transistors on ICs from different wafer in the same lot will not match very well.
 - ❖ Transistors on ICs from different wafer lots will match very power.
2. Bipolar transistors will match more precisely than CMOS transistors.
- CMOS technology is preferred for analog functions. The main reasons are
1. CMOS is the most widely used technology.
 2. Increased level of integration to combine analog and digital functions in the same IC.

Advantages

- Custom design at the physical level
- Smallest, fastest, and lowest power circuit
- High performance

Disadvantages

- More design time
- Custom mask set is expensive
- Economical only for High volume.

❖ Examples

- Microprocessor data path, cache, IO cell

5.3.3. SEMICUSTOM DESIGN

All of the logic cells are predesigned and some of the mask layers are customized. The predesigned cells from a cell library are used by the designers. There are two types of semicustom ASICs.

1. Standard-cell based ASICs
2. Gate-Array based ASICs

Standard cell based ASICs

A cell based IC (CBIC) uses predesigned logic cells. The standard cells are custom designed and then inserted into a library. These cells are then used in the design by placing them in rows and wired together using 'place and route' tools. Standard cell area is the rows of standard cells. For example, AND gates, OR gates, flip-flops, multiplexers are known as standard cells.

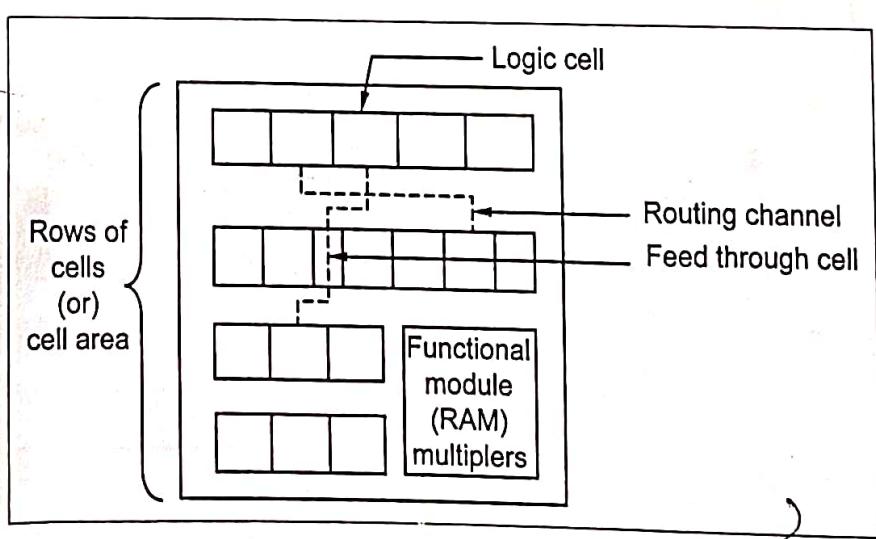


Fig. 5.6. Standard Cell Based ASIC

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The designer specifies the placement of standard cells and the interconnect on a CBIC. The standard cells can be placed anywhere on the silicon chip. i.e., all the mask layers of a CBIC are customized and are unique to a particular user.

The main features of standard all ASIC are

1. All mask layers such as transistors and interconnect are customized.
2. Custom blocks can be embedded.
3. Manufacturing lead time is about eight weeks.

Standard cells can fit together like bricks in a wall. The simple standard cell is shown in figure 5.6 power line (V_{DD}) and ground line (GND) run horizontally on metal lines inside the cells.

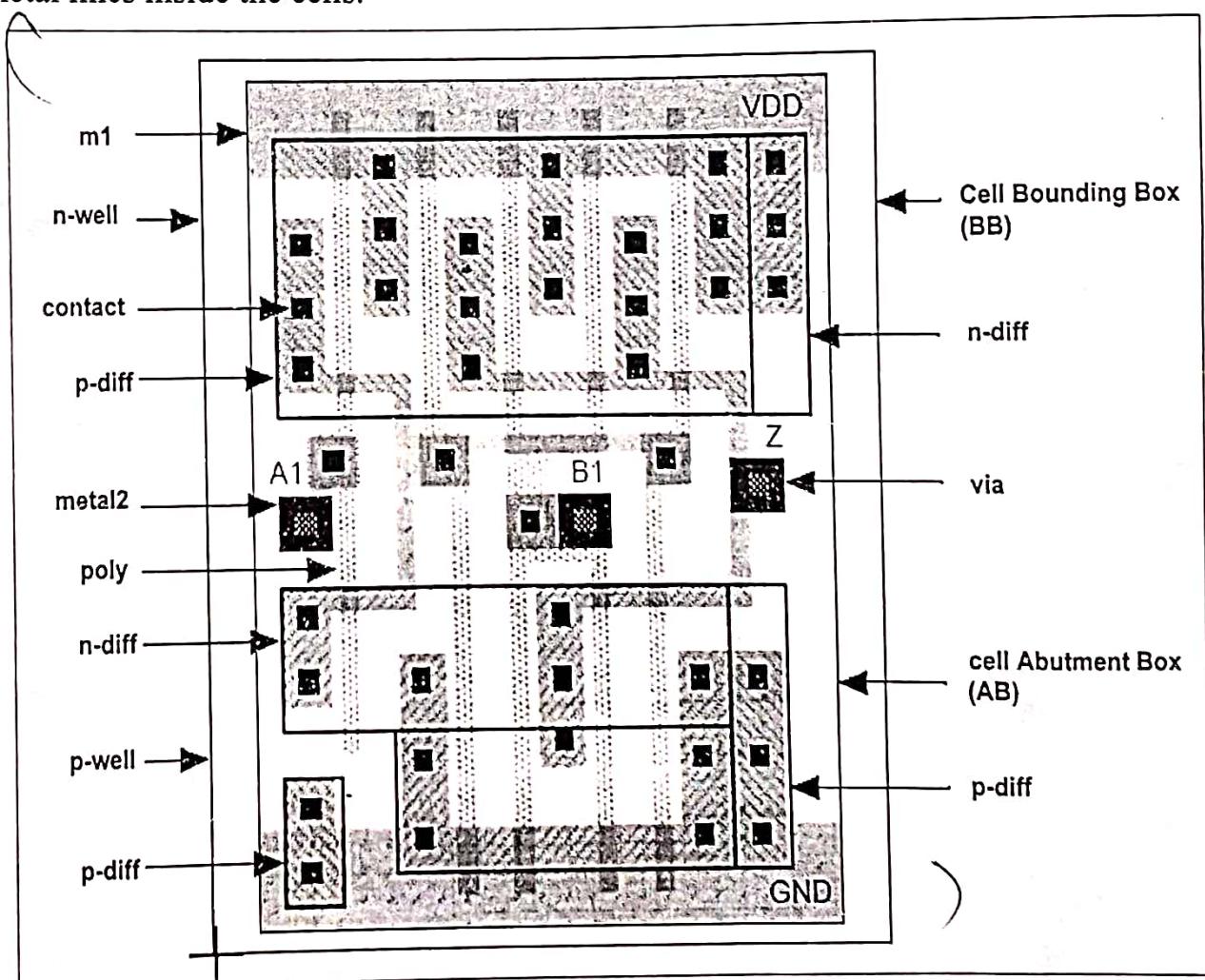


Fig. 5.7. Standard Cell with 25μ Wide

The assembling process of an ASIC can be automated using standard-cell design. A flexible block can be built from several rows of standard cells, which can also be connected to other standard cell blocks or full custom blocks.

When two or more layers of metal for interconnect are used, wires cross over different layers. Similar to copper traces in different layers of Printed Circuit Board (PCB).

In a two-level metal CMOS, connections to the standard cell inputs and outputs are made using second level or upper level of metal at the top and bottom of the cells. In a three-level metal CMOS, the connections may be internal to the logic cell and the extra metal layer can be used for routing interconnect.

A connection which crosses over a row of standard cells is achieved via feed through. Feed-through is nothing but a piece of metal which passes a signal through a cell or to a space in a cell.

The interconnections between logic cells use spaces between rows of cells called channels. The width of each row of standard cells is adjusted such that they are aligned with spacer cells.

ADVANTAGES

1. Cell based design has smaller, faster and lower power chips than gate arrays.
2. Higher productivity due to the use of predefined cells.
3. High performance and flexibility.
4. Less Design time.
5. Minimum Risk.

DISADVANTAGES

1. High expense of buying standard cell library
2. Requires more time for fabrication.

5.3.4. STANDARD CELL LIBRARY

Example

Typical Standard Cell library		
Gate Type	Variations	Options
Inverter / buffer / tristate buffers		Wide range of power options, IX, 2X, 4X, 8X, 16X, 32X, MX minimum size inverter
NAND/AND	2-8 inputs	High, normal, low power
NOR/OR	2-8 inputs	High, normal, low power
XOR/XNOR		High, normal, low power
AOI / OAI		High, normal, low power
Multiplexers	Inverting/noninverting	High, normal, low power
Schmitt trigger		High, normal, low power
Adder / half adder		High, normal, low power
Latches		High, normal, low power
Flip-flops	D, with and without synch/asynch set and reset, scan	High, normal, low power

Typical Standard Cell library		
Gate Type	Variations	Options
I/O pads	Input, output, tristate, bidirectional, boundary scan, slew rate limited, crystal oscillator	Various drive levels (1-16 mA) and logic levels

5.3.5. MACRO CELL DESIGN)

The standard cell areas may be used in combination with larger predesigned cells known as Macro Cell or Mega Cell.

Example: Standard cells such as RAM and ROM cells and some data path cells such as multiplier are tiled together to create macro cells.

Macro cell is also called mega functions; System Level Macros (SLM), fixed blocks, full-custom blocks or functional standard blocks.

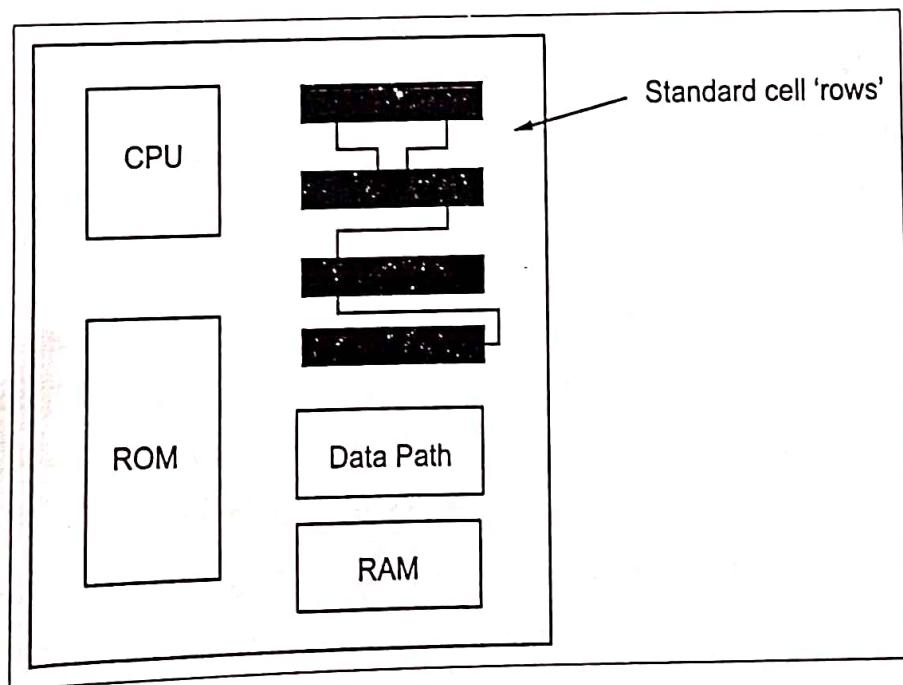


Fig. 5.8. Macro Cell

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When multiple signals are processed across a data bus such as data path, the standard cells will not be efficient. Some ASIC library provides a data path compiler which automatically generates data path logic.

A data path library may have cells such as adders, subtractors, multipliers, simple ALUs. The connectors of data path library cells are pitch-matched to each other i.e., fit together.

Standard-cell and gate-array libraries have hundreds of different logic cells such as NAND, NOR, AND, OR gates, latches, flip-flops.)

5.3.6. GATE-ARRAY BASED ASIC

The transistors masks are completely defined on the silicon wafer. The predefined pattern of transistors on a gate array is the base array.

The smallest element which is replicated to form the base array called base cell or primitive cell.

Designers define the interconnect between transistors using custom masks, to distinguish this array, it is called Masked Gate Array (MGA)

Macro

The designer selects the predesigned and pre-characterised logic cells from a gate-array library. The logic cells in a gate array library are called macros.

The base cell layout is same for each logic cell and only the interconnect is customized. Thus the gate-array macro is similar to a software macro. IBM calls the gate-array macros as books.

Both the cell-based and gate-array ASICs use predefined cells. In standard cell, the transistor sizes change to optimise speed and performance, whereas the gate array use fixed size of transistors. The tradeoff between areas and performance should be made in a standard cell ASIC. Hence gate array is called prediffused array.

The gate-array is classified into three types.

1. Channelled gate arrays
2. Channelless gate arrays
3. Structured gate arrays

5.3.6.1. CHANNELLED GATE ARRAY

In Channelled gate array architecture, the gate array is channelled i.e., the space between the rows of transistors are wired.

- ❖ Only the interconnect is customized
- ❖ The interconnect uses predefined spaces between rows of base cells.
- ❖ Manufacturing lead time is between 2 days and 2 weeks.

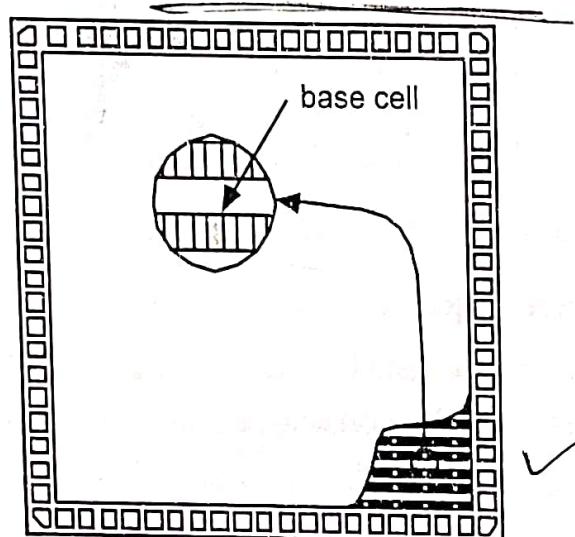


Fig. 5.9. Channelled gate array

Figure 5.8 shows a Channelled gate array. Rows of cells are separated using interconnect. This structure is similar to CBIC except that the space for interconnect between rows are fixed in height in a Channelled gate array, while the space between rows of cells can be adjusted in CBIC.

5.3.6.2. CHANNELLESS GATE ARRAY

The salient features of the channelless gate array are

- ❖ Only some mask layers are customized such as interconnect
- ❖ Manufacturing lead time is between 2 days and 2 weeks.

There is no predefined area for routing between cells on a channelless gate array. Routing is done over the top of the gate array devices as the first layer of metal defining connections between metal is customized.

When an area of transistors is used for routing, the transistors are left unused inspite of connecting the devices using contacts.

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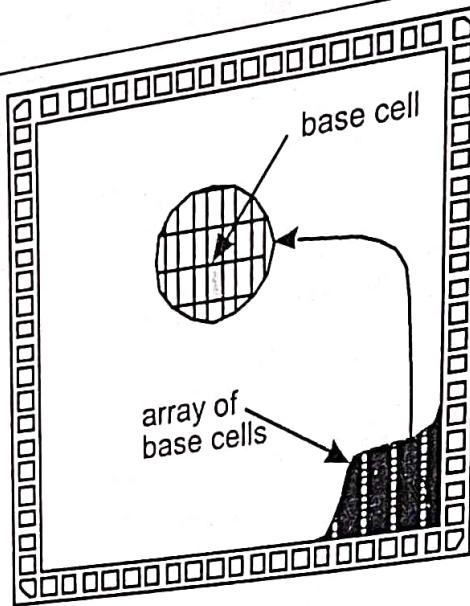


Fig. 5.10. Channelless gate-array (or) Sea of gates (SOG)

5.3.6.3. STRUCTURED GATE ARRAY

A structured gate array utilizes some of the features of cell-based ASICs (CBIC) and Masked Gate Array (MGA). It is otherwise known as an embedded gate array or master slice or master image.

We know that the MGA uses fixed gate-array base cell. This is the main disadvantage as it makes the memory implementation difficult and inefficient. So, some of the IC area is dedicated to a specific function in an embedded gate array. This embedded gate array may have

1. a different base cell for building memory cells (or)
2. complete circuit block. Example: Microcontroller

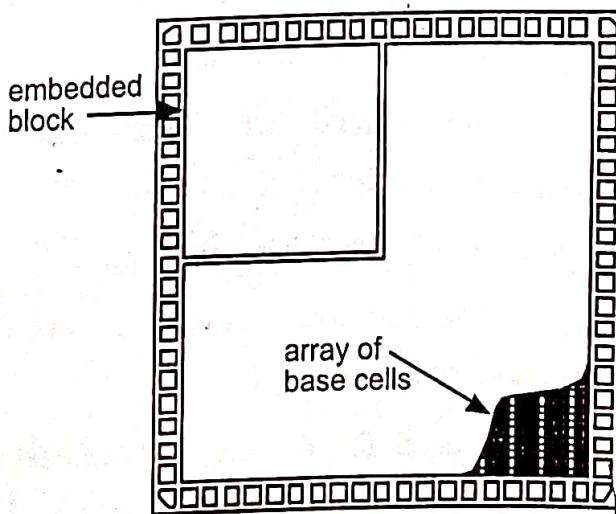


Fig. 5.11. Embedded gate array

The salient features of embedded gate array are

- ❖ only the interconnect is customized
- ❖ custom blocks can be embedded
- ❖ Manufacturing lead time is between 2 days and 2 weeks

ADVANTAGES

1. Improved area efficiency
2. High performance
3. Lower cost

DISADVANTAGES

1. Fixed embedded function
2. If the memory required is less than the memory in the embedded function, then some portion of the memory remain unused.

5.4. PROGRAMMABLE LOGIC DEVICES (PLD)

The programmable logic devices (PLDs) are standard ICs that are available in standard configuration. PLDs can be configured to create a customized part for specific application. A programmable logic device is shown in Figure 5.12.

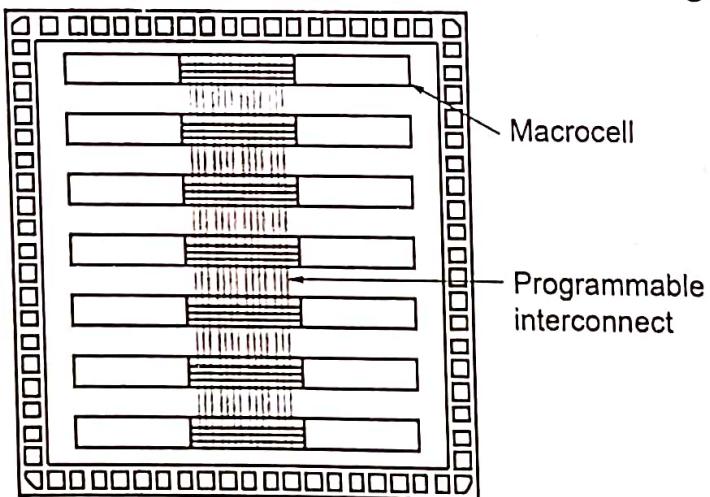


Fig. 5.12. Programmable Logic Device

The important features of PLD are

- No customized mask layers
- A single block of programmable interconnect

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- A matrix block of programmable array logic followed by a flip-flop or latch
- The programmable IC is classified as follows.

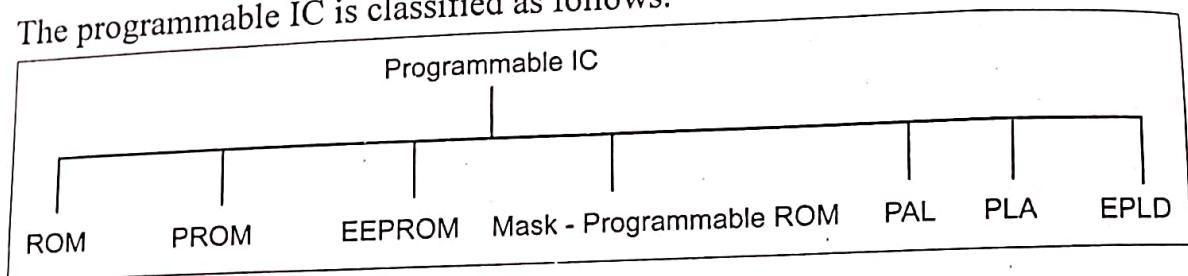


Fig. 5.13. Programmable IC Classification

ROM

The simple type of programmable IC is a Read-only Memory (ROM). It uses a metal fuse which is stored permanently.

PROM

Programmable ROM has programmable MOS transistors. When high voltage is applied, the characteristics of transistors can be varied.

EEPROM

In Electrically Erasable PROM (EEPROM), another high voltage is applied to erase the content of PROM. Ultra Violet rays (UV) can be applied to the device or the device is exposed to UV rays to erase the data.

Mask-programmable ROM

A masked ROM consists of a regular array of transistors permanently programmed using custom mask patterns. An embedded mask ROM is a large, specialized, logic cell.

Programmable Array Logic (PAL)

ROM can be made more flexible by using a large array of AND gates and OR gates. This programmable device is called logic array.

A PAL also consists registers or flip-flops to store the current state information. PAL has a programmable AND logic and fixed OR logic **Programmable Logic Array (PLA)**.

A logic array which is placed as a cell on a custom ASIC is called programmable logic array (PLA). PLA has a programmable AND logic and programmable OR logic.

Criterion	Standard Components	PLDs	Gate Arrays	Standard Cells	Full Custom
Time to market	Short to medium	Short	Medium	Medium	Long
Development lead time	Immediate	Immediate	Weeks to months	Weeks to months	Years
Development costs	None	Low	Medium to high	Medium to high	Very high
Availability	High	High	Medium	Medium	Low
Available sources	Many	Many	Few	Few	Few
Volume dependence	Low	Low	High	High	High
Application support	Much	Much	Some	Some	None
Architectural flexibility	Low	Medium to high	High	Higher	Highest
Design change ease	Medium	Medium to high	High	Higher	Highest
Performance	Low	High	High	High	Very high
Density	Low	Medium	Very high	Very high	Very high
Solution efficiency	Low to medium	Low	High	High	Very high
Design change cost	Low	Medium	High	High	Very high

Table 5.1.1 Comparison of standard components, plds, gate arrays, standard cells and full-custom ASICs

University Questions

1. Explain the programmable interconnects and I/O blocks used in FPGA.
2. With neat sketch explain the CLB, IOB and programmable interconnects of an FPGA device.

5/ Design for Testability : Ad Hoc Testing, Scan Design, BIST, IDDQ Testing, Design for Manufacturability, Boundary Scan

- Design for testability covers three important approaches :
1. Ad-hoc testing
 2. Scan based approaches
 3. Self-test and built in testing

Ad Hoc Testing

- Testability can be increased by making nodes more accessible at some cost by physically inserting more access circuits to the original design.
- Some of the ad hoc testable design techniques are :
 1. Partition-and-Mux Technique
 2. Initialize Sequential Circuit
 3. Disable Internal Oscillators and Clocks
 4. Avoid Asynchronous Logic and Redundant Logic
 5. Avoid Delay-Dependent Logic
- Ad hoc methods were the first DFT techniques introduced in the 1970s. The goal was to target only those portions of the circuit that would be difficult to test and to add circuitry to improve the controllability or observability.
- Ad hoc techniques typically use test point insertion to access internal nodes directly. An example of a test point is a multiplexer inserted to control or observe an internal node.

Scan Design

- The scan technique is a structured approach to designing sequential circuit for testability. The storage cells in registers are used as observation points, control points or both.
- The storage elements are connected to form a long, serial shift register therefore called scan path by using multiplexer and a mode control signal as shown in Fig. 5.2.1.

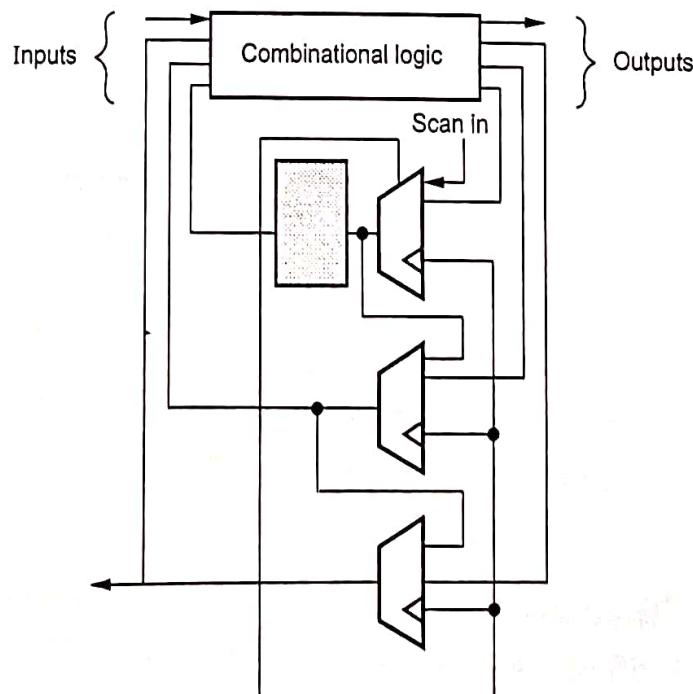


Fig. 5.2.1

- The scan based technique works in two modes :
 1. **Test mode** : The scan-in signal is clocked into scan path and output of last stage is scanned out.
 2. **Normal mode** : The scan-in path is disabled and the circuit functions as a sequential circuit.

Testing sequence

- The testing sequence is as follows :
 1. Set the mode to test mode and let latches accept data from scan-in input.
 2. Verify the scan path by shifting in and out the test data.
 3. Scan in (shift in) the desired state vector into the shift register.
 4. Apply the test pattern to primary input.
 5. Set mode to normal mode and observe the primary outputs of the circuit after sufficient time for propagation.
 6. Assert the circuit clock for one machine cycle to capture the outputs of the combinational logic into the registers.
 7. Return to test mode; scan out the contents of registers, and scan in the next pattern.
 8. Repeat testing steps 3 to 7 until all test patterns are applied.

Boundary Scan Check

- Boundary scan check is a test technique which uses scan methodology involving shift registers. The shift register control monitors signal at each input and output pins that are connected in serial fashion to form a chain of data register called Boundary Scan Registers.
- Printed circuit boards are becoming more dense and complex with use of surface mount devices (SMD). Hence most test system does not guarantee good fault coverage. Boundary scan check technique involves scan path and self tests which resolves above problems.

Merits of Boundary Scan Check

- Boundary scan check has following advantages over other testing methods.
 1. Increased fault coverage in system.
 2. The boundary scan check is much more time efficient. i.e. time required is much less than other systems.
 3. The process of boundary scan check is very simple.
 4. In built scan path and self test makes it more accurate and efficient.

Boundary Scan Standards

- Several standards are specified for boundary scan check testing. Their prime objective is to ensure testing and development less costly and efficient. Some boundary scan standards are mentioned -
 1. Joint Test Action Group [JTAG 1988]
 2. Element Test and Maintenance [ETM VHSIC]
 3. VHSIC Test and Maintenance [TM] Bus Standard.
 4. Testability Bus Standard [IEEE 1989J] / [IEEE 1149.1]

Boundary Scan Test Methodology

- The boundary scan shift register prevents output from rippling as data is shifted through the shift register during scan operation.

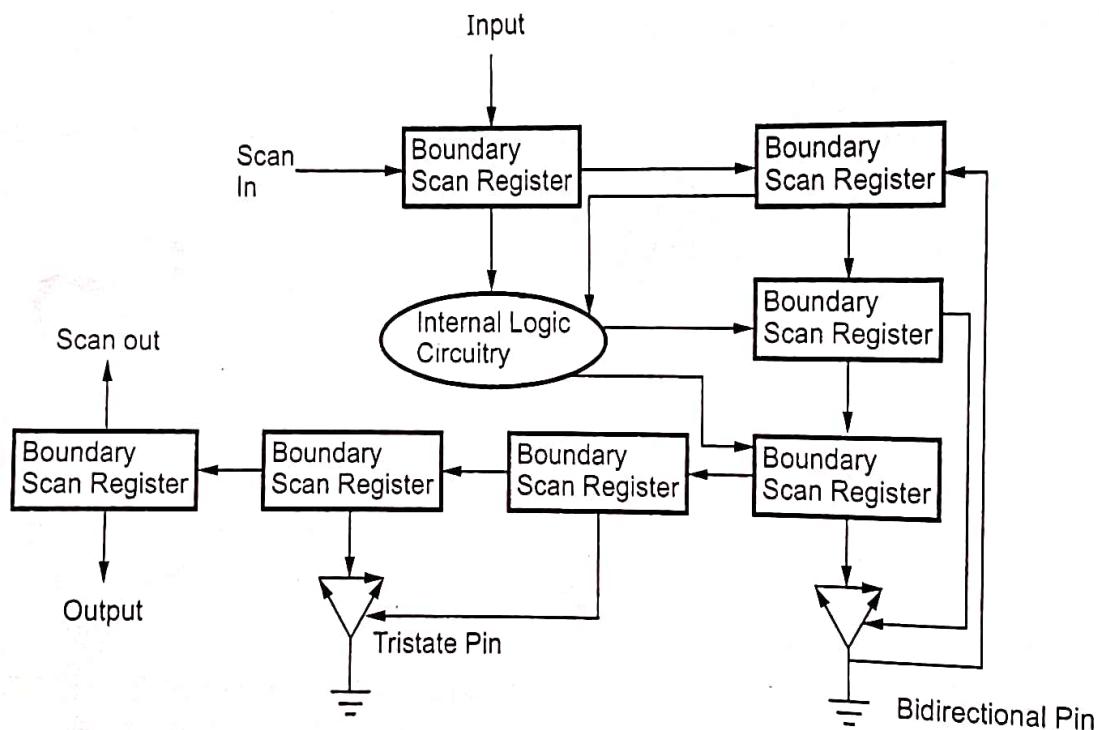


Fig. 5.2.2 Boundary scan test methodology

- The test set is scanned into boundary scan registers (BSR) by using a scan in port with test stimuli input. The response of the circuit is captured in parallel by BSRs in series and scanned out through scan out port.
- All the BSRs are interconnected to form a chain around the border of the circuit so as to form a single path as shown in Fig. 5.2.3 (See Fig. 5.2.3 on next page). It indicates the architecture of IEEE 1149 boundary scan.
- The boundary scan path is having serial input output cells/pads and has appropriate clock pads. The cells or pads are provided for -
 - a) Interconnections between chips
 - b) Internal self test

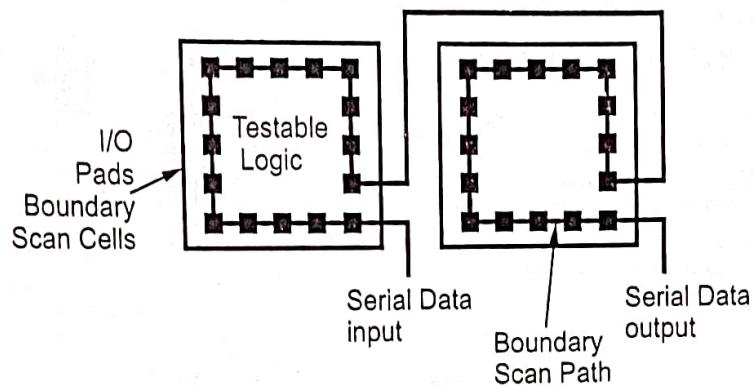


Fig. 5.2.3 Boundary scan architecture

- Various tests that carried out by the architecture IEEE 1149 are -
 - a) Sampling and setting chip Input/Outputs.
 - b) Connectivity test between components.
 - c) Distribution and collection of self test and built-in test results.

5.2.3 Built - In Self Test (BIST)

- With the increasing complexity of VLSI systems, test generation and application becomes an expensive and may not be an effective testing.
- Further the high speeds at which newer VLSI systems are designed to operate may not be possible to be simulated and this may create problems. These aspects can be well handled by incorporating BIST which is mainly focused at reducing -
 - a. The volume of test data.
 - b. Costs involved in test pattern generation.
 - c. Test time.
- All above points can be covered by integrating an automatic test system into the design of chip which is possible by different techniques.

These test include,

1. Linear Feedback Shift Register (LFSR)
2. Built-in Logic Block Observer (BILBO)
3. Signature Analysis

Advantages of BIST

1. Low cost.
2. High quality testing.
3. Faster fault detection.
4. Ease of diagnostics.
5. Reduced maintenance and repair costs.

- The essential circuit modules required for BIST are :

 - Pseudo Random Pattern Generator (PRPG)
 - Output Response Analyzer (ORA)

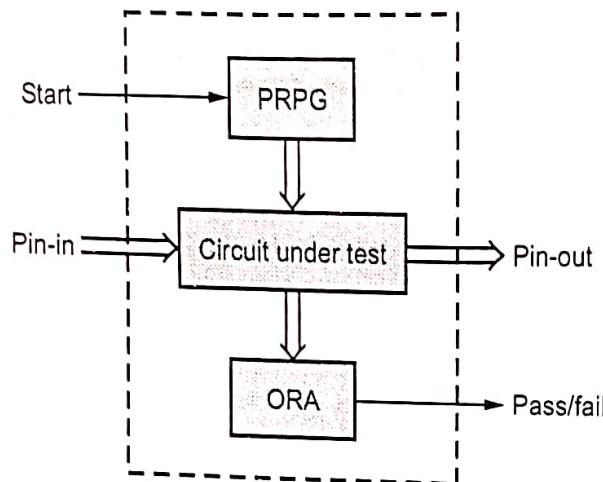


Fig. 5.2.4 BIST process

- Fig. 5.2.4 shows general procedure for BIST.

Pseudo Random Pattern Generator (PRPG)

- A Pseudo Random Bit Generator (PRBG) is defined as a deterministic algorithm which, given a truly random binary sequence of length k , outputs a binary sequence of length l_k that "appears" to be random.
- The input to the PRBG is called the seed, while the output of the PRBG is called a pseudo random bit sequence.
- A (pseudo) random bit sequence can be constructed by concatenation of (pseudo) random bits. A (pseudo) random number in interval $<0, n>$ can be converted from (pseudo) random bit sequence of length $[\log_2 n] + 1$ (if n is exceeded, new sequence should always be used).

IDDQ Testing

- The I_{DDQ} test is usually used for testing fabrication defects. In bridging fault CMOS circuit draws very high current from power supply.
- The I_{DDQ} test is performed by applying the test vector and then monitoring the current drawn from power supply. This test requires more time but fault detection capability is greatly improves.
- While stuck at tests requires both fault sensitization and fault effect propagation, the I_{DDQ} test requires only fault sensitization. The fault coverage is easy to obtain and offers a full chip coverage capability for large design.

Design guidelines for I_{DDQ} testability

1. Low static current states.
2. No active pull-ups or pull-downs.
3. No internal drive conflicts (drivers share a bus)
4. No floating nodes.
5. No degraded voltages.

Two Marks Questions with Answers

Q.1 What is a FPGA ?

Ans. : A Field Programmable Gate Array (FPGA) is a programmable logic device that supports implementation of relatively large logic circuits. FPGAs can be used to implement a logic circuit with more than 20,000 gates whereas a CPLD can implement circuits of upto about 20,000 equivalent gates..

Q.2 What are the different methods of programming of PALs ?

Ans. : The programming of PALs is done in three main ways :

- 1) Fusible links
- 2) UV - erasable EEPROM
- 3) EEPROM (E^2PROM) - Electrically Erasable Programmable ROM.

Q.3 What is an antifuse ?

Ans. : An antifuse is normally high resistance ($>100\text{ M}\Omega$). On application of appropriate programming voltages, the antifuse is changed permanently to a low-resistance structure ($200\text{-}500\ \Omega$).

Q.4 Explain different types of programmable devices.

Ans. : Types of Programmable Logic Devices (PLDs) : PROM, PAL, PLA, CPLDs, FPGAs, etc.

1. **PROM** : The PROM (Programmable Read Only Memory) has a fixed AND array (constructed as a decoder) and programmable connections for the output OR gates array. The PROM implements Boolean functions in sum-of-minterms form.
2. **PAL** : The PAL (Programmable Array Logic) device has a programmable AND array and fixed connections for the OR array.
3. **PLA** : The PLA (Programmable Logic Array) has programmable connections for both AND and OR arrays. So it is the most flexible type of PLD.

4. Complex Programmable Logic Devices (CPLDs) : A CPLD contains a bunch of PLD blocks whose inputs and outputs are connected together by a global interconnection matrix.

5. Field Programmable Gate Arrays (FPGAs) : The FPGA consists of three main structures :

- A] Programmable logic structure,
- B] Programmable routing structure, and
- C] Programmable Input/Output (I/O).

Q.5 State the three important blocks of FPGA architecture.

ANSWER

Ans. : The building blocks of FPGA are :

1. Logic Cells (LCs) grouped into Configurable Logic Blocks (CLBs)
2. I/O blocks
3. Programmable interconnects.

Q.6 What are the different chip-level test techniques ?

Ans. : Chip-level test techniques

1. Fault models : Stuck at faults, Stuck-open or Stuck-Shut-Fault
2. Scan Path : Full Scan, Partial Scan
3. Boundary Scan Check-JTAG, TAP Controller, BIST.

Q.7 Explain stuck-at-fault.

Ans. : Stuck-at-Fault

- The Stuck-at fault is a logical fault model in which faults are fixed (0 or 1) value to a net. A fault can exist at the input or at the output of a logic gate or a flip-flop in the circuit.
- If the net is stuck to 0, it is called stuck-at-0 (s-a-0) fault and if the net is stuck to 1, it is called stuck-at-1 (s-a-1) fault.

Q.8 Explain VLSI verification and testing.

Ans. : VLSI Verification is done before manufacturing. Before even tapeout. This is done for verifying if the chip design is working as expected.

Example : If we have a counter design in verilog, We can simulate the verilog file and verify if the sequence is correct. This is functionality check.

VLSI Testing is done after manufacturing. After the chips are made, we will look for any structural damages or mistakes in the chip. At this stage, we will check if the chip passes the test. If it does not, we throw away the chip. If it passes, we can use(sell) the chip. To do testing, we have to put some extra special logic into the chip before it is taped out. This is called Design For Testing (DFT).

