MIPs ISA Release 2

All 199 instructions from MIPs ISA Release 2 are summarized below. In this class, we implement only about 7 of them.

The full MIPS ISA reference documents are listed below.

Volume
Volume I: Introduction to the MIPS32 Architecture
Volume II: The MIPS32 Instruction Set
Volume III: The MIPS32 Privileged Resource Architecture

CPU Arithmetic Instructions

	Mnemonic	Instruction	Misc.
0	ADD	Add Word	
1	ADDI	Add Immediate Word	
2	ADDIU	Add Immediate Unsigned Word	
3	ADDU	Add Unsigned Word	
4	CLO	Count Leading Ones in Word	
5	CLZ	Count Leading Zeros in Word	
6	DIV	Divide Word	
7	DIVU	Divide Unsigned Word	
8	MADD	Multiply and Add Word to Hi, Lo	
9	MADDU	Multiply and Add Unsigned Word to Hi, Lo	
10	MSUB	Multiply and Subtract Word to Hi, Lo	
11	MSUBU	Multiply and Subtract Unsigned Word to Hi, Lo	
12	MUL	Multiply Word to GPR	
13	MULT	Multiply Word	
14	MULTU	Multiply Unsigned Word	
15	SEB	Sign-Extend Byte	Release 2 Only
16	SEH	Sign-Extend Halftword	Release 2 Only
17	SLT	Set on Less Than	
18	SLTI	Set on Less Than Immediate	
19	SLTIU	Set on Less Than Immediate Unsigned	
20	SLTU	Set on Less Than Unsigned	
21	SUB	Subtract Word	
22	SUBU	Subtract Unsigned Word	

CPU Branch and Jump Instructions

	Mnemonic	Instruction	Misc.
0	B	Unconditional Branch	
1	BAL	Branch and Link	
2	BEQ	Branch on Equal	
3	BGEZ	Branch on Greater Than or Equal to Zero	
4	BGEZAL	Branch on Greater Than or Equal to Zero and Link	
5	BGTZ	Branch on Greater Than Zero	
6	BLEZ	Branch on Less Than or Equal to Zero	
7	BLTZ	Branch on Less Than Zero	
8	BLTZAL	Branch on Less Than Zero and Link	
9	BNE	Branch on Not Equal	
10	J	Jump	
11	JAL	Jump and Link	
12	JALR	Jump and Link Register	
13	JALR.HB	Jump and Link Register with Hazard Barrier	Release 2 Only
14	JR	Jump Register	
15	JR.HB	Jump Register with Hazard Barrier	Release 2 Only

CPU Instruction Control Instruction

	Mnemonic	Instruction	Misc.
0	EHB	Execution Hazard Barrier	Release 2 Only
1	NOP	No Operation	
2	SSNOP	Superscalar No Operation	

CPU Load, Store, and Memory Control Instructions

	Mnemonic	Instruction	Misc.
0	LB	Load Byte	
1	LBU	Load Byte Unsigned	
2	LH	Load Halfword	
3	LHU	Load Halfword Unsigned	
4	LL	Load Linked Word	
5	LW	Load Word	
6	LWL	Load Word Left	
7	LWR	Load Word Right	
8	PREF	Prefetch	
9	SB	Store Byte	
10	SC	Store Conditional Word	

	Mnemonic	Instruction	Misc.
11	SH	Store Halfword	
12	SW	Store Word	
13	SWL	Store Word Left	
14	SWR	Store Word Right	
15	SYNC	Synchronize Shared Memory	
16	SYNCI	Synchronize Caches to Make Instruction Writes Effective	Release 2 Only

CPU Logical Instructions

	Mnemonic	Instruction
0	AND	And
1	ANDI	And Immediate
2	LUI	Load Upper Immediate
3	NOR	Not Or
4	OR	Or
5	ORI	Or Immediate
6	XOR	Exclusive Or
7	XORI	Exclusive Or Immediate

CPU InsertExtract Instructions

	Mnemonic	Instruction	Misc.
0	EXT	Extract Bit Field	Release 2 Only
1	INS	Insert Bit Field	Release 2 Only
2	WSBH	Word Swap Bytes Within Halfwords	Release 2 Only

CPU Move Instructions

	Mnemonic	Instruction	Misc.
0	MFHI	Move From HI Register	
1	MFLO	Move From LO Register	
2	MOVF	Move Conditional on Floating Point False	
3	MOVN	Move Conditional on Not Zero	
4	MOVT	Move Conditional on Floating Point True	
5	MOVZ	Move Conditional on Zero	
6	MTHI	Move To HI Register	

	Mnemonic	Instruction	Misc.
7	MTLO	Move To LO Register	
8	RDHWR	Read Hardware Register	Release 2 Only

CPU Shift Instructions

	Mnemonic	Instruction	Misc.
0	ROTR	Rotate Word Right	Release 2 Only
1	ROTRV	Rotate Word Right Variable	Release 2 Only
2	SLL	Shift Word Left Logical	
3	SLLV	Shift Word Left Logical Variable	
4	SRA	Shift Word Right Arithmetic	
5	SRAV	Shift Word Right Arithmetic Variable	
6	SRL	Shift Word Right Logical	
7	SRLV	Shift Word Right Logical Variable	

CPU Trap Instructions

	Mnemonic	Instruction	Misc.
0	BREAK	Breakpoint	
1	SYSCALL	System Call	
2	TEQ	Trap if Equal	
3	TEQI	Trap if Equal Immediate	
4	TGE	Trap if Greater or Equal	
5	TGEI	Trap if Greater of Equal Immediate	
6	TGEIU	Trap if Greater or Equal Immediate Unsigned	
7	TGEU	Trap if Greater or Equal Unsigned	
8	TLT	Trap if Less Than	
9	TLTI	Trap if Less Than Immediate	
10	TLTIU	Trap if Less Than Immediate Unsigned	
11	TLTU	Trap if Less Than Unsigned	
12	TNE	Trap if Not Equal	
13	TNEI	Trap if Not Equal Immediate	

Obsolete CPU Branch Instructions

	Mnemonic	Instruction
0	BEQL	Branch on Equal Likely

	Mnemonic	Instruction
1	BGEZALL	Branch on Greater Than or Equal to Zero and Link Likely
2	BGEZL	Branch on Greater Than or Equal to Zero Likely
3	BGTZL	Branch on Greater Than Zero Likely
4	BLEZL	Branch on Less Than or Equal to Zero Likely
5	BLTZALL	Branch on Less Than Zero and Link Likely
6	BLTZL	Branch on Less Than Zero Likely
7	BNEL	Branch on Not Equal Likely

FPU Arithmetic Instruction

	Mnemonic	Instruction
0	ABS.fmt	Floating Point Absolute Value
1	ADD.fmt	Floating Point Add
2	DIV.fmt	Floating Point Divide
3	MADD.fmt	Floating Point Multiply Add
4	MSUB.fmt	Floating Point Multiply Subtract
5	MUL.fmt	Floating Point Multiply
6	NEG.fmt	Floating Point Negate
7	NMADD.fmt	Floating Point Negative Multiply Add
8	NMSUB.fmt	Floating Point Negative Multiply Subtract
9	RECIP.fmt	Reciprocal Approximation
10	RSQRT.fmt	Reciprocal Square Root Approximation
11	SQRT.fmt	Floating Point Square Root
12	SUB.fmt	Floating Point Subtract

FPU Branch Instructions

	Mnemonic	Instruction
0	BC1F	Branch on FP False
1	BC1T	Branch on FP True
2	C.cond.fmt	Floating Point Compare

FPU Compare Instructions

	Mnemonic	Instruction
0	C.cond.fmt	Floating Point Compare

FPU Convert Instructions

	Mnemonic	Instruction	Misc.
0	ALNV.PS	Floating Point Align Variable	64-bit FPU Only
1	CEIL.L.fmt	Floating Point Ceiling Convert to Long Fixed Point	64-bit FPU Only
2	CEIL.W.fmt	Floating Point Ceiling Convert to Word Fixed Point	
3	CVT.D.fmt	Floating Point Convert to Double Floating Point	
4	CVT.L.fmt	Floating Point Convert to Long Fixed Point	64-bit FPU Only
5	CVT.PS.S	Floating Point Convert Pair to Paired Single	64-bit FPU Only
6	CVT.S.PL	Floating Point Convert Pair Lower to Single Floating Point	64-bit FPU Only
7	CVT.S.PU	Floating Point Convert Pair Upper to Single Floating Point	64-bit FPU Only
8	CVT.S.fmt	Floating Point Convert to Single Floating Point	
9	CVT.W.fmt	Floating Point Convert to Word Fixed Point	
10	FLOOR.L.fmt	Floating Point Floor Convert to Long Fixed Point	64-bit FPU Only
11	FLOOR.W.fmt	Floating Point Floor Convert to Word Fixed Point	
12	PLL.PS	Pair Lower Lower	64-bit FPU Only
13	PLU.PS	Pair Lower Upper	64-bit FPU Only
14	PUL.PS	Pair Upper Lower	64-bit FPU Only
15	PUU.PS	Pair Upper Upper	64-bit FPU Only
16	ROUND.L.fmt	Floating Point Round to Long Fixed Point	64-bit FPU Only
17	ROUND.W.fmt	Floating Point Round to Word Fixed Point	
18	TRUNC.L.fmt	Floating Point Truncate to Long Fixed Point	64-bit FPU Only
19	TRUNC.W.fmt	Floating Point Truncate to Word Fixed Point	

FPU Load, Store, and Memory Control Instructions

	Mnemonic	Instruction	Misc.
0	LDC1	Load Doubleword to Floating Point	
1	LDXC1	Load Doubleword Indexed to Floating Point	64-bit FPU Only
2	LUXC1	Load Doubleword Indexed Unaligned to Floating Point	64-bit FPU Only
3	LWC1	Load Word to Floating Point	
4	LWXC1	Load Word Indexed to Floating Point	64-bit FPU Only
5	PREFX	Prefetch Indexed	
6	SDC1	Store Doubleword from Floating Point	
7	SDXC1	Store Doubleword Indexed from Floating Point	64-bit FPU Only
8	SUXC1	Store Doubleword Indexed Unaligned from Floating Point	64-bit FPU Only
9	SWC1	Store Word from Floating Point	
10	SWXC1	Store Word Indexed from Floating Point	64-bit FPU Only

FPU Move Instructions

	Mnemonic	Instruction	Misc.
0	CFC1	Move Control Word from Floating Point	
1	CTC1	Move Control Word to Floating Point	
2	MFC1	Move Word from Floating Point	
3	MFHC1	Move Word from High Half of Floating Point Register	Release 2 Only
4	MOV.fmt	Floating Point Move	
5	MOVF.fmt	Floating Point Move Conditional on Floating Point False	
6	MOVN.fmt	Floating Point Move Conditional on Not Zero	
7	MOVT.fmt	Floating Point Move Conditional on Floating Point True	
8	MOVZ.fmt	Floating Point Move Conditional on Zero	
9	MTC1	Move Word to Floating Point	
10	MTHC1	Move Word to High Half of Floating Point Register	Release 2 Only

Obsolete FPU Branch Instructions

	Mnemonic	Instruction
0	BC1FL	Branch on FP False Likely
1	BC1TL	Branch on FP True Likely

Coprocessor Branch Instructions

	Mnemonic	Instruction
0	BC2F	Branch on COP2 False
1	BC2T	Branch on COP2 True

Coprocessor Execute Instructions

	Mnemonic	Instruction
0	COP2	Coprocessor Operation to Coprocessor 2

Coprocessor Load and Store Instructions

	Mnemonic	Instruction
0	LDC2	Load Doubleword to Coprocessor 2
1	LWC2	Load Word to Coprocessor 2
2	SDC2	Store Doubleword from Coprocessor 2
3	SWC2	Store Word from Coprocessor 2

Coprocessor Move Instructions

	Mnemonic	Instruction	Misc.
0	CFC2	Move Control Word from Coprocessor 2	
1	CTC2	Move Control Word to Coprocessor 2	
2	MFC2	Move Word from Coprocessor 2	
3	MFHC2	Move Word from High Half of Coprocessor 2 Register	Release 2 Only
4	MTC2	Move Word to Coprocessor 2	
5	MTHC2	Move Word to High Half of Coprocessor 2 Register	Release 2 Only

Obsolete Coprocessor Branch Instructions

	Mnemonic	Instruction
0	BC2FL	Branch on COP2 False Likely
1	BC2TL	Branch on COP2 True Likely

Privileged Instructions

	Mnemonic	Instruction	Misc.
0	CACHE	Perform Cache Operation	
1	DI	Disable Interrupts	Release 2 Only
2	EI	Enable Interrupts	Release 2 Only
3	ERET	Exception Return	
4	MFC0	Move from Coprocessor 0	
5	MTC0	Move to Coprocessor 0	
6	RDPGPR	Read GPR from Previous Shadow Set	Release 2 Only
7	TLBP	Probe TLB for Matching Entry	
8	TLBR	Read Indexed TLB Entry	
9	TLBWI	Write Indexed TLB Entry	
10	TLBWR	Write Random TLB Entry	
11	WAIT	Enter Standby Mode	
12	WRPGPR	Write GPR to Previous Shadow Set	Release 2 Only

EJTAG Instructions

	Mnemonic	Instruction
0	DERET	Debug Exception Return
1	SDBBP	Software Debug Breakpoint