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BMS College of Engineering, Bangalore-560019

(Autonomous Institute, Affiliated to VTU, Belgaum)

December 2016 Semester End Main Examinations

Course: Computer Organization and Architecture — Duration: **3 hrs**
Course Code: 15CS3DCCOA — Max Marks: **100**

Date: 22.12.2016

Instructions: **1.Answer any five full questions choosing one from each unit.**
2. Assume missing data (if any) suitably

UNIT 1

1	a)	Explain auto increment and decrement addressing modes with an example for each and write an assembly language program to add N numbers using immediate and indirect addressing modes.	08
	b)	Discuss the parameters on which the performance of a processor depends.	04
	c)	Show how the operation Z=(P x (Q/R-(S x T))) – (U x V) can be implemented in a single accumulator computer by (i) Three address (ii) Two address and (iii) single address instructions	08

UNIT 2

2	a)	Define bus master. Explain centralized and distributed bus arbitration with block diagram.	10
	b)	Outline the advantage of using direct memory access. Explain with block diagram.	06
	c)	Describe the use of PCI bus in a computer system	04

OR

3	a)	With a timing diagram explain the read operation on the PCI bus.	08
	b)	Illustrate the significance of using tree structure in USB architecture.	08
	c)	Describe target controllers with respect to SCSI Bus, explain their working in brief.	04

UNIT 3

4	a)	Define logical address. Explain virtual memory working with a block diagram.	08
	b)	Explain the cache associative and set associative mapping techniques with an example.	08
	c)	Is static random access memory faster than dynamic memory? Justify with a diagram.	04

OR

5	a)	Explain the organization and access of data on hard disk.	06
	b)	Describe the advantage of dynamic memory. Explain the design of 16 Mb DRAM chip.	08
	c)	A block set-associative cache consists of a total of 64 blocks divided into four block sets. The main memory contains 4096 blocks, each consisting of 128 words. Identify the following: a) How many bits are there in a main memory? b) How many bits are there in each of the TAG, SET, and WORD fields? c) What is the size of the cache memory?	06

UNIT 4

6	a)	Multiply 12x8 using add and shift method and write the register configuration required for the same.	08
	b)	Write the algorithm of non-restoring division method and perform the division 0011/0010 using the same.	08
	c)	Represent 571.25 in IEEE single precision floating point format.	04

UNIT 5

7	a)	Explain the single bus organization of CPU with a neat diagram and write the control steps required for executing the instruction Add #2, R2.	10
	b)	Is micro-programmed control unit faster than Hardwired? Justify. Explain the working of micro-programmed control unit with a block diagram	06
	c)	Describe thread level parallelism. List its applications.	04

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