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BMS College of Engineering, Bengaluru-560019

(Autonomous Institute, Affiliated to VTU, Belgaum)

July / August 2016 Supplementary Examination

Course: Computer Organization & Architecture **Duration: 3 Hours**
Course Code: 15CS3DCCOA **Max Marks: 100**
Date:29.07.2016

Instruction: Answer any five full questions choosing one from each unit.

UNIT-I

1. a) Explain the four generic instruction types. Also mention assembly instructions to compute C = A+B for each example case. **10**
   b) Explain the factors on which the performance of a system is evaluated. **05**
   c) Registers R1 and R2 of a computer contain the decimal values 1200 and 4600. What is the effective address of the memory operand in each of the following instructions? **05**
   i) Load 20(R1), R5
   ii) Move #3000, R5
   iii) Store R5, 30(R1, R2)
   iv) Add –(R2), R5
   v) Sub (R1)+, R5

UNIT-II

2. a) What is bus arbitration? Explain centralized and distributed bus arbitration. **10**
   b) What do you mean by interrupt nesting? Explain interrupt priority scheme with a neat diagram. **10**

OR

3. a) With a neat diagram explain the concept of Handshake control of data transfer during input operation. **08**
   b) What are the different modes of data transfer? Explain DMA controller with a block diagram. **08**
   c) What are the differences between PCI and SCSI buses? **04**

UNIT-III

4. a) With a diagram explain structure of a DRAM cell. **04**
   b) Explain memory hierarchy used in a computer. **06**
   c) With a neat diagram explain design of 1K X 1 memory module. **10**

OR

5.	a)	Explain different mapping techniques used in cache memories.	**10**
	b)	Explain with necessary diagram how virtual address is translated in to physical address. Also explain the use of TLB.	**10**

UNIT-IV

6.	a)	Explain the IEEE Floating Point Formats, Represent (0.0625)10 in IEEE Floating point Formats.	**10**
	b)	Multiply (+22)(Multiplicand) x Multiplier(-6) using Booth's Algorithm Method	**05**
	c)	Multiply 110101 (Multiplicand) x 011011 (Multiplier) using Bit-Pair Recoding Method	**05**

UNIT - V

7.	a)	With a neat diagram, explain multiple bus organization of a processor.	**06**
	b)	Explain with the block diagram the basic organization of a microprogrammed control unit.	**08**
	c)	Explain Flynn's classification of computers.	**06**

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