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BMS College of Engineering, Bangalore-560019

(Autonomous Institute, Affiliated to VTU, Belgaum)

July / August 2017 Supplementary Semester Examinations

Course: Computer Organization and Architecture — Duration: **3 hrs**
Course Code: 15CS3DCCOA — Max Marks: **100**

Date: 31.07.2017

Instructions: **1.Answer any five full questions choosing one from each unit.**
2. Assume missing data (if any) suitably

UNIT 1

1 a) Describe basic performance equation for processor. Explain SPEC method for Performance measurement. 06

b) Write a program to evaluate the expression A X B + C X D in a Single-accumulator processor. Assume the processor has Load, Store, Multiply and Add instructions. 04

c) Consider a computer that has 32-bit big-endian arranged byte-addressable memory. A program reads the name "Johnson" and stores them in successive byte locations starting at location 1000. Show the contents of memory words at location 1000 and 1004. 04

d) Register R5 is used in a program to point to top of the stack. Write a sequence of instructions using index, Auto increment and Auto decrement addressing modes to perform each of the following tasks. 06

i) Pop the top two items off the stack, add them, and then push the result onto the stack

ii) Copy the 5^{th} item from the top into register R3 Remove top 10 items from the stack

UNIT 2

2 a) Identify the arbitration technique which uses daisy chain and demonstrate distributed Arbitration technique with example. 07

b) Devise a mechanism to handle interrupts which allows the interrupt to the processor, when another interrupt is being serviced. 06

c) Point out the limitations of synchronous bus transfer and manipulate it to overcome the limitations. 07

OR

3 a) With a diagram of serial interface circuit, Discuss the connection of processor to I/O devices using serial port. 08

b) Discuss handshaking scheme for controlling data transfers on the bus between the master and the slave, with timing diagram for input data transfer. 06

c) Explain the main phases involved in the operation of SCSI Bus. 06

UNIT 3

4 a) Devise the implementation details in designing a 16-M DRAM chip, configured using 2M x 8 dynamic memory chip. 08

b) Illustrate different types of Read Only Memories. 08

c) A block-set-associative cache consists of total 64 blocks divided into 4-block sets. The main memory contains 4096 blocks, each consisting of 128 words. 04

i) Find the number of bits in main memory address.

ii) Calculate the number of bits in TAG, SET and WORD fields

OR

5 a) Explain Direct Cache memory mapping technique with block diagram. 06

b) Demonstrate the translation of Virtual address to physical address with diagram. 08

c) A disk has 24 recording sufaces and total of 14,000 cylinders. There is an average of 400 sectors per track. Each sector contains 512 bytes of data. 06

i) Calculate the maximum number of bytes that can be stored in this unit.

ii) Find the data transfer rate in bytes per second at a rotational speed of 7200rpm

iii) Using 32-bit word, suggest a suitable scheme for specifying the disk address assuming there are 512 bytes per sector

UNIT 4

6 a) Design a 16 bit Carry lookahead adder by cascading 4-bit carry lookahead adders and compute the gate delays to produce s_{15} and c_{16}. Compare the gate delays needed when 16-bit carry lookahead adder is built using high level generate and propagate functions of 4-bit CLA. 08

b) Compute the multiplication of given signed 2's complement number using Bit-pair recoding. Assume A is Multiplicand and B as Multiplier. 06

A=110011 B=101100

c) Formulate the values represented by the following single precision IEEE standard Floating point format and perform addition on the numbers and represent the result back in IEEE standard format 06

A = 0 100001 111111110

B = 0 011111 001010101

UNIT 5

7 a) With a neat diagram, explain Multiple bus organization and write control sequence for Add (R_4), R_5. 08

b) Illustrate with a neat block diagram the microprogrammed control unit for branching and breakdown the instruction branch<0 into sequence of microinstructions. 06

c) Describe the Flynn's taxonomy for classification of parallel computers. 06

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