USN | | | | | | | | | | |

BMS College of Engineering, Bangalore-560019

(Autonomous Institute, Affiliated to VTU, Belgaum)

July / August 2016 Supplementary Examination

Course: Computer Organization & Architecture **Duration: 3 hours**
Course code: 09CI3GCCOA **Max Marks: 100**
Date: 29.07.2016

Instructions: Answer any FIVE full questions, choosing one full question from each unit.

UNIT – I

1	a	Explain with a diagram, connections between processor and memory.	8
	b	Explain with an example, the stack structure and its operations.	12

UNIT – II

2	a	Write control sequence for execution of instruction, Add (R3),R1 in single bus architecture. Provide explanation for each step.	8
	b	Explain Hardwired control unit. Give an example for generation of control signal.	6
	c	Describe the generation of microinstructions with next-address field.	6

OR

3	a	Explain asynchronous and synchronous models in linear pipeline processors.	6
	b	Provide reservation and latency analysis in nonlinear pipeline processors.	6
	c	Explain Three-bus organization of the data path.	8

UNIT - III

4	a	Represent 571.25 in IEEE single and double precision format.	6
	b	Perform division operation on 010010÷000110 using nonrestoring method.	10
	c	Construct an example to show that three guard bits are needed to produce the correct answer when two positive numbers are subtracted.	4

UNIT - IV

5	a	What is Bus Arbitration ? Explain the different Bus Arbitration Methods	10
	b	Explain the mechanism of Interrupts used in synchronizing the data transfers between the processor and memory.	10

UNIT – V

6	a	Explain any two mapping methods used in cache memory.	8
	b	Explain virtual memory concept and address translation.	7
	c	Describe asynchronous DRAMs.	5

OR

7	a	Explain the controller's major functions on the disk drive.	4
	b	What are replacement algorithms? Briefly explain the LRU replacement algorithm.	8
	c	Give the organization of a 2M x 32 memory module using 512K x 8 static memory chips.	8

******