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BMS College of Engineering, Bangalore-560019

(Autonomous Institute, Affiliated to VTU, Belgaum)

July / August 2016 Supplementary Examination

Course: Logic Design **Duration: 3 hours**

Course code: 09CI3GCLDL **Max Marks: 100**

Date:04.08.2016

Instructions:

Answer any **FIVE** full questions, choosing one full question from each unit.

UNIT – I

1	a	Using the Boolean Algebra postulates and theorems, simplify the following expression as disjunctive normal form formula with fewest number of literals. (i) $\overline{w}\ \overline{x}\ \overline{y}\,z + w\ \overline{x}\ \overline{y}\,z + xy\,\overline{z}$ (ii) $(x+z)(w+x)(\overline{y}+z)(w+\overline{y})$	4
	b	Determine minimal sum & minimal product for the given Boolean function using VEM technique. Take 'z' as MEV. $f(w,x,y,z) = \sum m(0,1,4,6,9,11) + dc(3,15)$	8
	c	Define Boolean algebra with 6-postulates and state the principle of duality.	8

UNIT – II

2	a	Simplify the following Boolean function by using Quine-McClusky method and prime implicant table reduction: $F(A,B,C,D) = \sum(1,3,6,8,9,10,12,14) + \sum dc(7,13)$	10
	b	Define a decoder. Construct a 4:16 decoder using 2:4 decoders.	4
	c	Realize a full adder and a full subtractor using a 4:1 Multiplexer.	6

OR

3	a	Design a 2-bit Comparator using basic gates.	6
	b	Write the condensed truth table for 4 to 2 line priority encoder with a valid output where the highest priority is given to the highest bit position and obtain the minimal sum expressions for the outputs.	6
	c	Explain 4-bit carry look ahead adder, with the help of a logic diagram.	8

UNIT – III

4	a	Using a PROM of appropriate size, draw the logic diagram in PLD notation for a PROM realization to convert 3 bit binary numbers into gray code.	5
	b	Show how a D flip flop can be converted to SR flip flop.	4
	c	What is 0's and 1's catching? Give the function table and characteristic equation for JK flip flop.	8
	d	Explain the following: i) Minimum pulse width ii) Setup time.	3

UNIT – IV

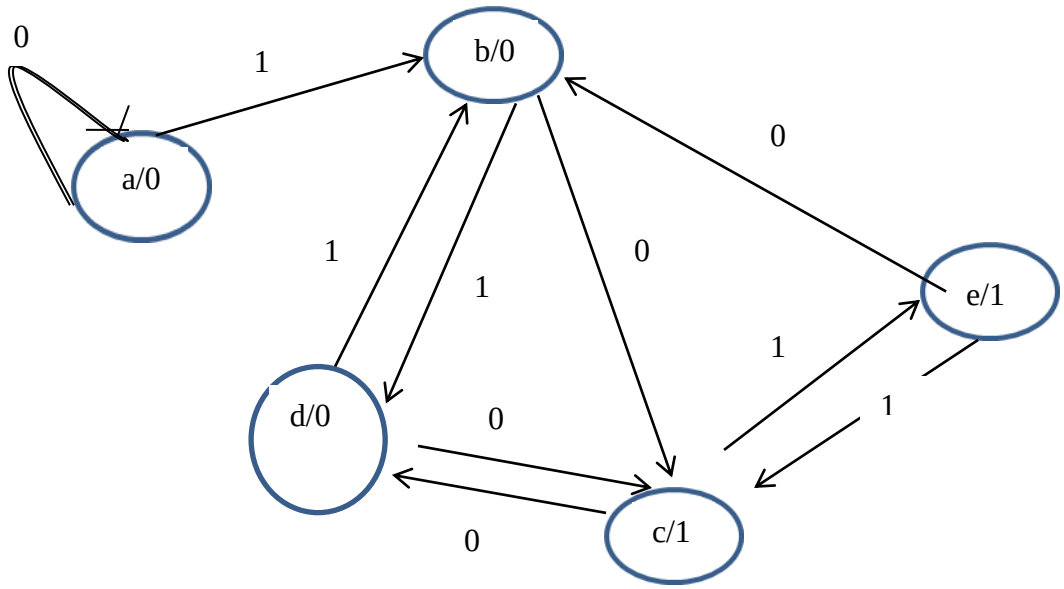
5	a	Explain the Universal shift register with logic diagram, mode control and symbol.	10
	b	Design a Mod-6 synchronous counter whose counting sequence consists of 000, 001, 010, 011, 100 101 using 'JK' flip-flop.	10

OR

6	a	Design a Mod-6 synchronous counter whose counting sequence consists of 000, 001, 010, 011, 100, 101 using 'D' flip-flop.	10
	b	Discuss the two drawbacks of resistive divider used in converting digital input to analog output. Draw the schematic for a 4-bit binary ladder and explain how the digital to analog conversion is achieved using it.	10

UNIT – V

7	a	Design a Mealy Model for the binary data stream 011 with design equations and neat circuit diagram.	8
	b	Analyze AND gate and NAND gate as asynchronous sequential circuit.	6
	c	Reduce the given state transition diagram by row elimination method.	6



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