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BMS College of Engineering, Bangalore-560019

(Autonomous Institute, Affiliated to VTU, Belgaum)

July / August 2017 Supplementary Semester Examinations

Course: **Computer Organization and Embedded System** Duration: **3 hrs**
Course Code: **15IS3DCCOE** Max Marks: **100**
Date: 25.07.2017

Instructions: **1.Answer any five full questions choosing one from each unit.**
2. Assume missing data (if any) suitably

UNIT 1

1.	a)	Explain Subroutine linkage with an example.	**06**
	b)	Describe a RISC-style program that computes the expression SUM = 100 + 200 + 300.	**07**
	c)	Explain the components involved in connection between the processor and the main memory with a neat diagram	**07**

UNIT 2

2.	a)	Explain the process of control signal generation in hardwired control and microprogramming with neat diagrams.	**10**
	b)	Outline the sequence of actions produced by a processor to fetch and execute a conditional and an unconditional branch instruction in terms of the specific control signals produced at each clock during the whole process.	**10**

UNIT 3

3.	a)	Develop a program that displays the contents of ten bytes of the main memory in hexadecimal format on a line of a display device. The ten bytes start at location LOC in the memory and there are two hex characters per byte. The contents of successive bytes should be separated by a space when displayed.	**08**
	b)	Interpret the following at each level in the memory hierarchy i) Finding a block ii) Write Policy	**08**
	c)	Differentiate between a subroutine and an interrupt-service routine.	**04**

OR

4.	a)	Explain the timing diagram for modified synchronous input data transfer with multiple clock cycles with a neat diagram	**06**
	b)	Develop and explain a RISC-style program for Program-controlled I/O implemented with a wait loop involving a keyboard and a display device, that reads one line from the keyboard, stores it in memory buffer and echoes it back to the display.	**08**
	c)	Explain the process of address translation in virtual memory.	**06**

UNIT 4

5.	a)	Apply Booth's algorithm to multiply two 4-bit numbers 1011 and 0101 using Booth's algorithm. Verify the result obtained.	**06**
	b)	Design a binary addition/subtraction logic circuit. Illustrate how the process of binary addition and subtraction takes place with an example.	**08**

c) Explain the logic circuit arrangement that implements the restoring division algorithm. **06**

UNIT 5

6. a) Assume that the I/O device is capable of sending 8-bit data in a bit-serial manner. Consider now a similar device that uses eight lines to send the data in parallel. Thus, one of the parallel ports in the microcontroller has to be used to receive the data. This leaves only one parallel port to display two hexadecimal digits that represent the data. Hence, only one 7-segment display device can be used. To convey the received information, a single device can be used to display the digits one after another. Let the most-significant digit be displayed for one second, followed by a one-second blank period, and then the second digit is displayed for one second. After displaying the second digit, the display should show a "dash" for two seconds. This sequence is to be repeated continuously, reflecting the latest data received. Assume that it is driven by a 100-MHz clock. Show the necessary hardware connections and write a program to implement the required task. Use polling to check the timer status. **10**

b) Illustrate how double buffering is used on transmit and receive paths of the serial interface with a neat diagram. Show the addressable registers of the serial interface. **10**

OR

7. a) Illustrate the working of a sensor using a voltage divider. **05**

b) With a neat block diagram of a microcontroller, explain the working of typical microcontroller chip components. **07**

c) Explain with a neat block diagram of a microwave oven, how it uses computer control to govern their operation. **08**

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