U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

December 2018 / January 2019 Semester End Main Examinations

Programme: B.E. **Semester : III**
Branch : Computer Science and Engineering **Duration: 3 hrs.**
Course Code : 15CS3DCCOA **Max Marks: 100**
Course Title : Computer Organization and Architecture **Date: 05.01.2019**

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any may suitably assumed.

UNIT - I

1	a)	With neat diagram explain different functional units of a computer.	**08**
	b)	For the following processor, calculate the performance (or time required to execute). Clock rate = 800 MHz Number of instructions executed = 1000 Average number of steps needed per machine instruction = 20	**04**
	c)	With example, explain any four addressing modes.	**08**

UNIT - II

2	a)	Design *Input interface* circuit. Show your design with neat diagram and describe.	**08**
	b)	Define bus arbitration. Explain the centralized arbitration with a neat diagram.	**06**
	c)	With neat diagram explain Universal Serial Bus (USB) architecture.	**06**

OR

3	a)	Considering Asynchronous (or Handshake Control) Bus, write timing diagram for the following and explain **i.** For Input data Transfer or Read Operation **ii.** For Output data Transfer or Write Operation	**10**
	b)	Discuss the main phases involved in the operation of SCSI bus.	**06**
	c)	Differentiate between serial and parallel port.	**04**

UNIT - III

4	a)	A a cache is organized in the direct-mapped manner with the following parameters: Main Memory size 64K words. Cache size 1K words Block size 128 words i. How many bits are there in main memory address? ii. How many bits are there in each of the TAG, BLOCK and WORD fields?	**06**

b) Design memory module of 2Mx32 using 512K x 8 memory chips. Show your design with neat diagram. **10**

c) Describe the memory hierarchy with respect to speed, size and cost with a neat diagram. **04**

OR

5 a) Explain any two mapping functions used in cache Memory. **08**

b) With a neat diagram explain how virtual memory translation takes place. **06**

c) A disk unit has 24 recording surfaces and has a total of 14,000 Cylinders. There is an average of 400 sectors per track, each sector contains 512 bytes of data. **06**

i. What is the maximum number of bytes that can be stored in this disk unit?

ii. What is the data transfer rate in bytes per second at a rotational speed of 7200 rpm?

(Note: rpm=Revolutions per minute.)

UNIT - IV

6 a) Perform multiplication for +13(Multiplicand) and -06(Multiplier) using Booth's Algorithm. Consider 5-bit number representation. **06**

b) Design 32-bit adder using 4-bit carry look ahead adders(CLA). Calculate the number of gate delays for carry (C_{32}) and Sum(S_{31}). Note: Show your design with neat diagram. **08**

c) Using restoring division algorithm, perform the division of 00011 (+3 Divisor) with 1000 (+8 Dividend). Show the solving steps completely and clearly. **06**

UNIT - V

7 a) List and explain different classifications of parallel computer according Flynn's Taxonomy. **08**

b) Using single bus organization, write complete control sequence for execution of the instruction Add (R3), R1 ; $R1 \longleftarrow [[R3]] + [R1]$ **08**

c) With a neat block diagram, explain hardwired control unit. **04**

****