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BMS College of Engineering, Bangalore-560019

(Autonomous Institute, Affiliated to VTU, Belgaum)

January 2017 Semester End Make Up Examinations

Course: Computer Organization and Architecture — Duration: **3 hrs**
Course Code: 15CS3DCCOA — Max Marks: **100**

Date: 17.01.2017

Instructions: **1.Answer any five full questions choosing one from each unit.**
2. Assume missing data (if any) suitably

UNIT 1

1	a)	With the help of a neat diagram, explain the instruction execution process of the following instructions : i. Load MEML, RO ii. Add RO, RI	08
	b)	Write a complete ALP to compute the factorial of a given number using subroutine concept.	06
	c)	Discuss Auto-increment and program relative addressing modes. Give Examples for each.	06

UNIT 2

2	a)	With a neat timing diagram, illustrate the read and write operation of input data transfer on a Synchronous bus using multiple clock cycles.	08
	b)	Differentiate between Subroutine and Interrupt Service routine.	04
	c)	Show a circuit arrangement and explain how interrupt request from several I/O devices can be communicated to a processor through a single INTR Line.	08

OR

3	a)	With a neat timing diagram, explain the read operation on the PCI bus.	08
	b)	With the help of suitable diagram, discuss the split bus operation in USB.	06
	c)	Describe the output interface circuit for connecting a printer to the processor with a neat diagram.	06

UNIT 3

4	a)	Design and explain a 4MB X 32 memory module using 512KB X 8 memory chips. Show the address lines and control signals required.	08
	b)	Outline the differences between SRAM and DRAM.	06
	c)	Explain the read/write operation of an SRAM cell designed using CMOS. Illustrate the same with the aid of a diagram.	06

OR

5	a)	Illustrate with a neat block diagram the cache mapping functions along with its merits and demerits.	10
	b)	Discuss replacement algorithm and explain LRU replacement algorithm.	05
	c)	Illustrate with a neat diagram the method for translating virtual address to physical address	05

UNIT 4

6	a)	Apply Booth algorithm to perform the multiplication on +9 and +15. Summarize the relative merits of Bit-Pair recoding method of Booth's Algorithm.	08
	b)	Subtract -12 from -40 Applying 7 bit 2's complement representation, including the sign bit.	04
	c)	Represent $(+1259.125)_{10}$ using IEEE Single and Double precision floating point notation. List the steps used to perform floating point addition and subtraction.	08

UNIT 5

7	a)	Describe with a neat diagram the basic organization of a CPU in terms of registers and other units for a single datapath CPU. Show the complete action of the CPU in fetching and executing the instruction.	08
	b)	Describe the taxonomy of Flynn's classification. Discuss in detail with a neat diagram.	08
	c)	Illustrate the differences between Hardwired and Microprogrammed control.	04

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