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BMS College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

January 2018 Semester End Make Up Examinations

Course: Computer Organization and Architecture **Duration: 3 hrs.**
Course Code: 15CS3DCCOA **Max Marks: 100**
Date:12.01.2018

Instructions: **Answer any FIVE full questions, choosing one from each Unit.**

UNIT 1

1.	a)	Explain the basic operational concept between memory and processor when the instruction Add LOCA, R0 is executed with relevant diagram.	08
	b)	Write an assembly program to perform=(A+B)*(C+D) using i. Three address instructions ii. Two address instructions iii. One address instructions iv. Zero address instructions	08
	c)	Write an assembly program to add N numbers.	04

UNIT 2

2.	a)	Describe sequence of events that occur when an interrupt arrives.	05
	b)	Explain centralized and distributed bus arbitration with necessary diagrams.	10
	c)	Explain Daisy chain arrangement for connecting multiple devices to a common interrupt line.	05

UNIT 3

3.	a)	Design 2M X 32 memory module using 512K X 8 static memory chips.	10
	b)	Explain virtual memory address translation with necessary diagram.	06
	c)	Explain why address and data lines are multiplexed on to same lines. On multiplexing what is the additional requirement in circuits.	04

OR

4.	a)	Explain different mapping techniques used in cache memories with an example.	12
	b)	Give a typical internal organization of a 2Mx8 dynamic memory chip with necessary diagram.	08

UNIT 4

5.	a)	Multiply -13(multiplicand) and -20(Multiplier) using Booth's algorithm.	08

	b)	Divide 10 by 2 using non restoring division algorithm.	08
	c)	Convert 34.890625 to IEEE 32bit floating point format.	04

UNIT 5

6.	a)	Describe taxonomy of Flynn's classification.	08
	b)	With a block diagram explain the structure of hardwired control unit.	12

OR

7.	a)	With a block diagram explain the structure of micro programmed control unit.	10
	b)	Design control sequence for the execution of the instruction Add (R3), R1.	06
	c)	Is micro programmed control unit faster than hardwired control unit? Justify.	04

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