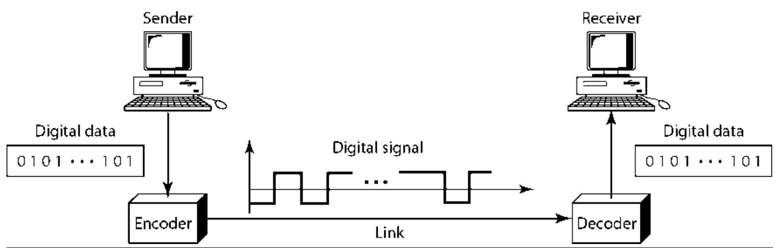
Chapter 4
Digital Transmission I
Digital to Digital Conversion

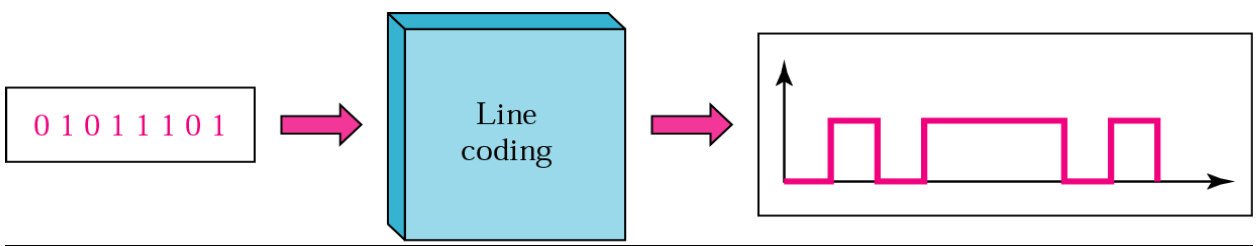
In this we see how we can represent digital data by using digital signals. The conversion of digital data to digital signals involves three techniques: **line coding, block coding, and scrambling**. Line coding is always needed; block coding and scrambling may or may not be needed.

Line Coding

Line coding is the process of converting binary data to a digital signal.

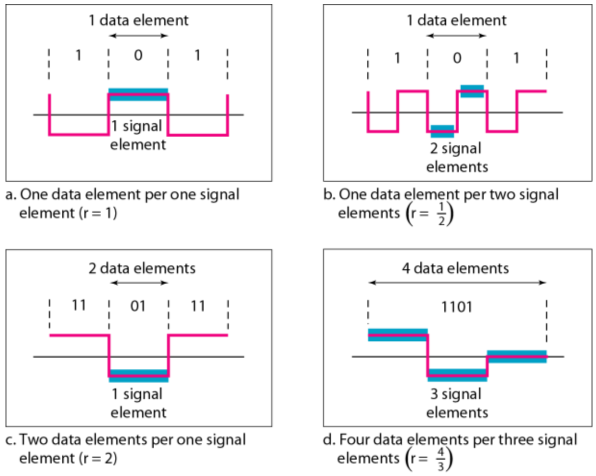
At the sender digital data are encoded into a digital signal, at the receiver digital signal is decoded to digital data.





Characteristics

Signal Element versus Data Element: A **data element** is the smallest entity representing a piece of information (bit).
A **signal element** is the shortest unit (timewise) of a digital signal.
A signal element carries data elements.
Ratio r defines the number of data elements carried by each signal element



Signal element VS data element

When r=1 means one data element is carried by one signal element.
When r= ½ means we need 2 sihnal elements to carry one data element.
When r= 2 means one signal element carrying 2 data elements.
When r= 4/3 means 4 bits are carried by 3 signal elements.

Suppose each data element is a person who needs to be carried from one place to another.we can think of signal element as a vehicle that can carry people.when r=1 , it means each person is driving a vehicle. When r > 1 , it means more than one person is travelling in a vehicle**.**

Data Rate versus Signal Rate :

The data rate is the number of data elements sent in 1s. The unit is bps.
The signal rate is the number of signal elements sent in 1s. The unit is baud.
The data rate is sometimes called the **bit rate**.
The signal rate is sometimes called the **pulse rate**, the **modulation rate** or the **baud rate**.

One goal in data communications is to increase the data rate while decreasing the signal rate.

Increasing the data rate increases the speed of transmission, Decreasing the signal rate decreases the bandwidth requirement

Ex: Carry more people in fewer vehicles to prevent traffic jams

Relationship between data rate and signal rate

The relationship between bit rate and baud rate depends on the value of *r* and the data pattern.
Three cases (Worst – max signal rate, best – min signal rate and average) need to be defined to derive a formula for the relationship.

$$S = c*N*1/r \quad \text{baud}$$

Where N is the data rate (bps), C is the case factor, S is the number of signal elements, r is the ratio of number of data elements carried by each signal element

A signal is carrying data in which one data element is encoded as one signal element (r = 1). If the bit rate is 100 kbps, what is the average value of the baud rate if c is between 0 and 1?

Solution

We assume that the average value of c is 1/2 . The baud rate is then

$$S = c \times N \times \frac{1}{r} = \frac{1}{2} \times 100{,}000 \times \frac{1}{1} = 50{,}000 = 50 \text{ kbaud}$$

Bandwidth

Baud rate determines the required bandwidth, means bandwidth is proportional to the signal rate (Baud Rate)

The formula for minimum bandwidth can be given as

Bmin = C*N*(1/r)

The maximum data rate can be given as

Nmax = B*r*(1/c)

A signal with L levels actually can carry log2L bits per level. If each level corresponds to one signal element and we assume the average case (c = 1/2), then we have

$$N_{\max} = \frac{1}{c} \times B \times r = 2 \times B \times \log_2 L$$

Baseline Wandering

In decoding a digital signal, the receiver calculates a running average of the received signal power. This average is called the baseline.

The incoming signal power is evaluated against this baseline to determine the value of the data element.

A long string of 0s or 1s can cause a drift in the baseline called baseline wandering thereby making it difficult for the receiver to decode correctly.

Note: A good line coding scheme needs to prevent baseline wandering

DC Components

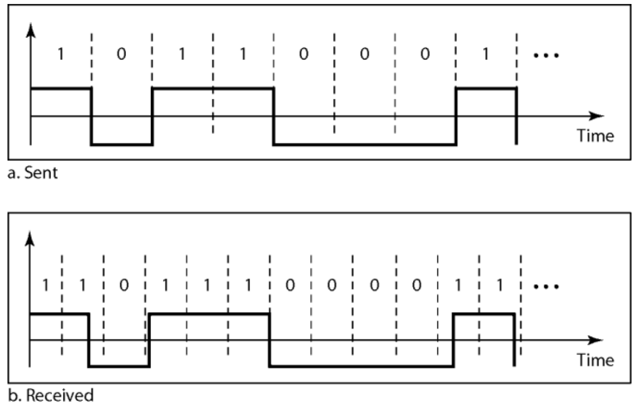
When the voltage level in a digital signal is constant for a while, the spectrum creates very low frequencies. These frequencies are called DC components

DC components present problems for a system that cannot pass low frequencies or a system that uses electrical coupling

Self-synchronization

The receiver's bit intervals must correspond exactly to the sender's bit intervals otherwise the receiver might misinterpret the signals.

A self-synchronizing digital signal includes timing information in the data being transmitted



Effect of lack of synchronization

In a digital transmission, the receiver clock is 0.1 percent faster than the sender clock. How many extra bits per second does the receiver receive if the data rate is
1 kbps? How many if the data rate is 1 Mbps?

Solution
At 1 kbps, the receiver receives 1001 bps instead of 1000 bps.

$$\frac{1000 \text{ bits sent} \quad 1001 \text{ bits received} \quad 1 \text{ extra bps}}{}$$

At 1 Mbps, the receiver receives 1,001,000 bps instead of 1,000,000 bps.

1,000,000 bits sent 1,001,000 bits received 1000 extra bps

Built-in error detection

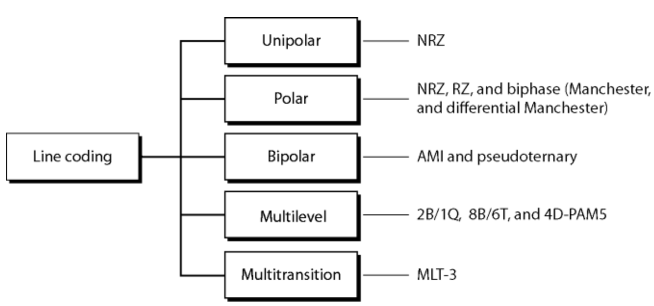
It is desirable to have a built-in error-detecting capability in the generated code to detect errors that occurred during transmission.

Immunity to Noise and Interference

Another desirable code characteristic is that the code is immune to noise and other interferences.

Complexity

A complex scheme is more costly to implement than a simple one. A scheme that uses four signal levels is more difficult to interpret that one that uses two levels.



Line Encoding schemes

Unipolar scheme,

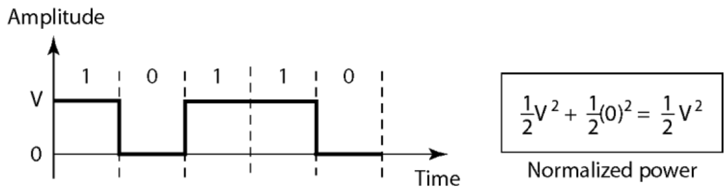
all the signal levels are on one side of the time axis.

NRZ: A unipolar scheme was designed as a NRZ (non-return-to-zero) scheme means the signal does not return to zero at the middle of the bit.

In Unipolar scheme **positive voltage defines bit 1 and zero voltage defines bit 0.**

This scheme is normally not used in data communications today as it is very costly.

Unipolar encoding uses only one voltage level.



polar schemes

In **polar schemes** voltages are on both sides of the time axis.

+ve voltage defines 0 and –ve voltage defines 1

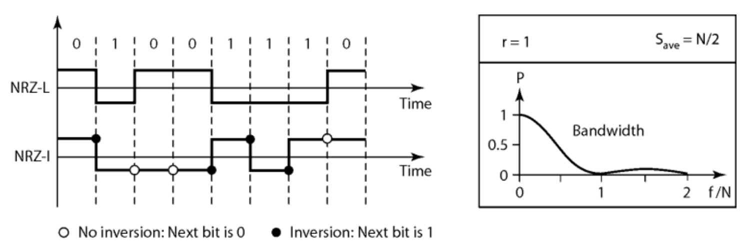
Polar schemes can be NRZ or RZ

NRZ: There can be two versions of polar NRZ: **NRZ-L and NRZ-I**

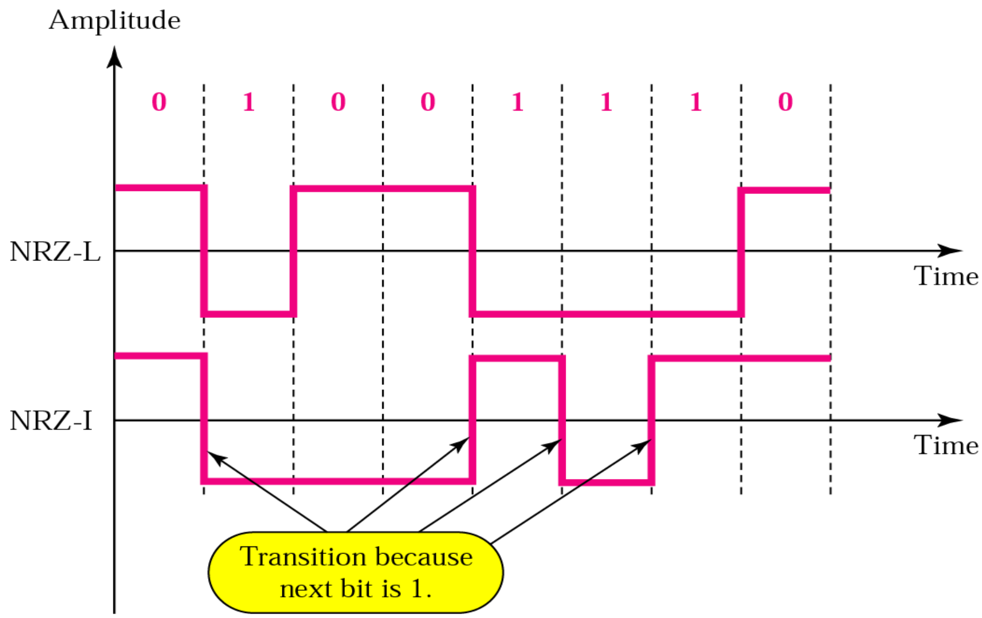
In **NRZ-L,** the level of voltage determines the value of the bit.

In **NRZ-I,** the change or no change in the level of voltage determines the value of the bit

If there is no change the bit is 0; if there is a change the bit is 1



NOTE: In NRZ-L the level of the voltage determines the value of the bit. In NRZ-I the inversion or the lack of inversion determines the value of the bit.



Comparison of NRZ-L and NRZ-I

NRZ-L :

Baseline wandering occurs for a long sequence of 0s or 1s
A long sequence of zeros or 1s can cause synchronization problem
Change in polarity of the wire results in all 0s interpreted as 1s & vice-versa

NRZ-I :

Baseline wandering occurs only for long sequence of 0s
A long sequence of zeros can cause synchronization problem
No such problem

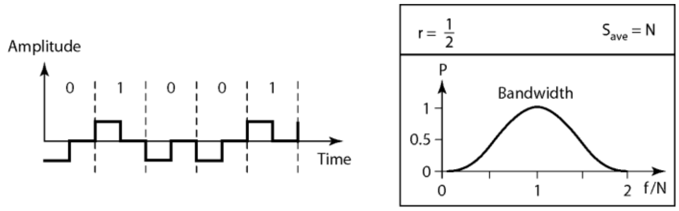
NOTE: NRZ-L and NRZ-I both have an average signal rate of N/2 Bd. NRZ-L and NRZ-I both have a DC component problem.

The main problem with NRZ encoding occurs when the sender and receiver clocks are not synchronized. One solution is the **return-to-zero (RZ)** scheme, in which the signal changes during the bit.

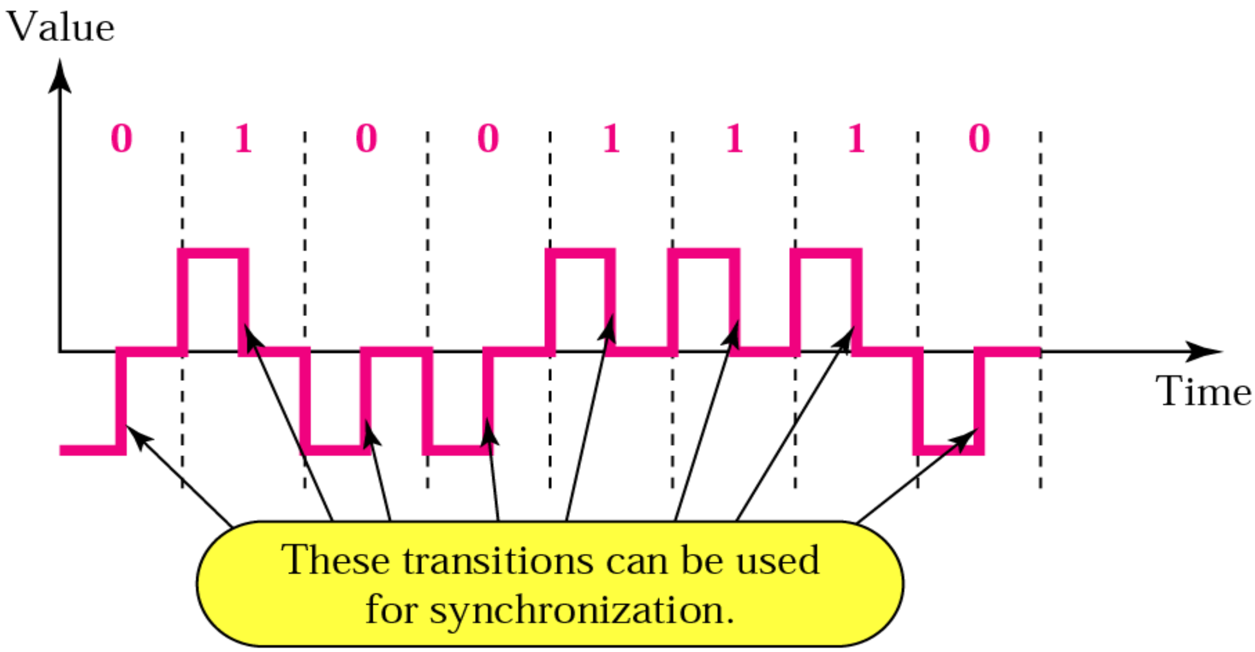
RETURN TO ZERO(RZ)

RZ scheme uses three values**: positive negative and zero**, which is more complex to create and discern.
The signal changes not between the bits but during bits.
In fig we can see that signal goes to 0 in the middle of each bit.
The disadvantage of this scheme is that it requires two signal changes to encode a bit and therefore occupies greater bandwidth.

Problem of polarity exists here also.
No DC component problem.



Polar RZ scheme



Biphase : Manchester and Differential Manchester

The idea of RZ and NRZ-L are combined into Manchester scheme

The duration of the bit is divided into two halves.

The voltage remains at one level during the first half and moves to the other level in the second half

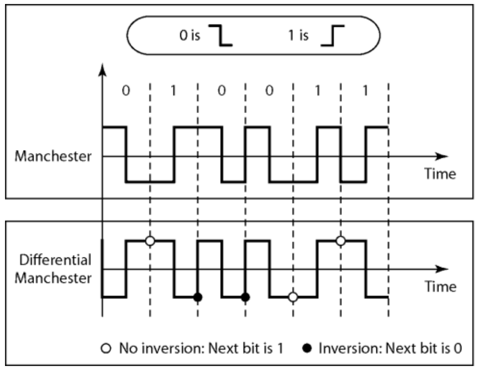
In Manchester encoding, the transition at the middle of the bit is used for both synchronization and bit representation.

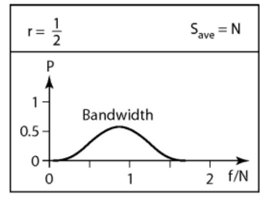
Differential Manchester combines the ideas of RZ and NRZ-I

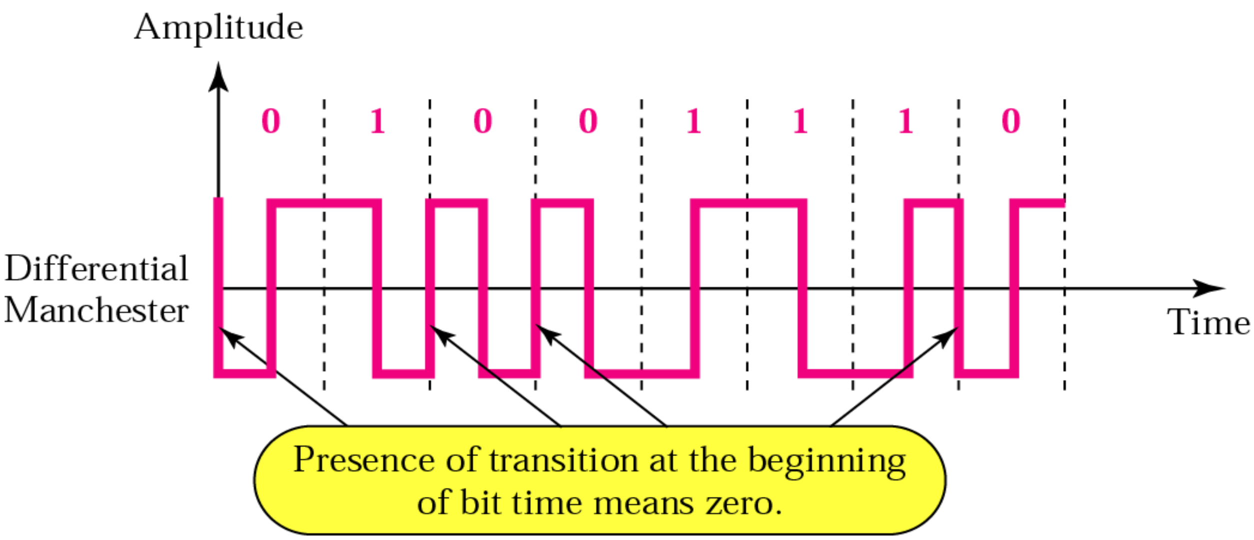
There is a transition at the middle of the bit, but the bit values are determined at the beginning of the bit.

If the next bit is zero there is a transition, if 1 no transition.

In differential Manchester encoding, the transition at the middle of the bit is used only for synchronization.
The bit representation is defined by the inversion or noninversion at the beginning of the bit.







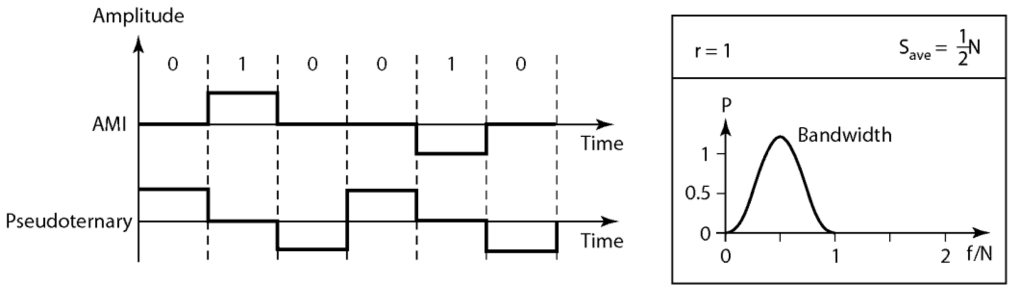
Manchester scheme overcomes problems associated with NRZ-L
Differential Manchester overcomes problems associated with NRZ-I.
No Baseline wandering, No DC Component.
The only drawback is the signal rate, which is double that for NRZ
Manchester and Differential-Manchester schemes are also called biphase schemes

NOTE: In Manchester and differential Manchester encoding, the transition at the middle of the bit is used for synchronization. The minimum bandwidth of Manchester and differential Manchester is 2 times that of NRZ.

Bipolar Schemes

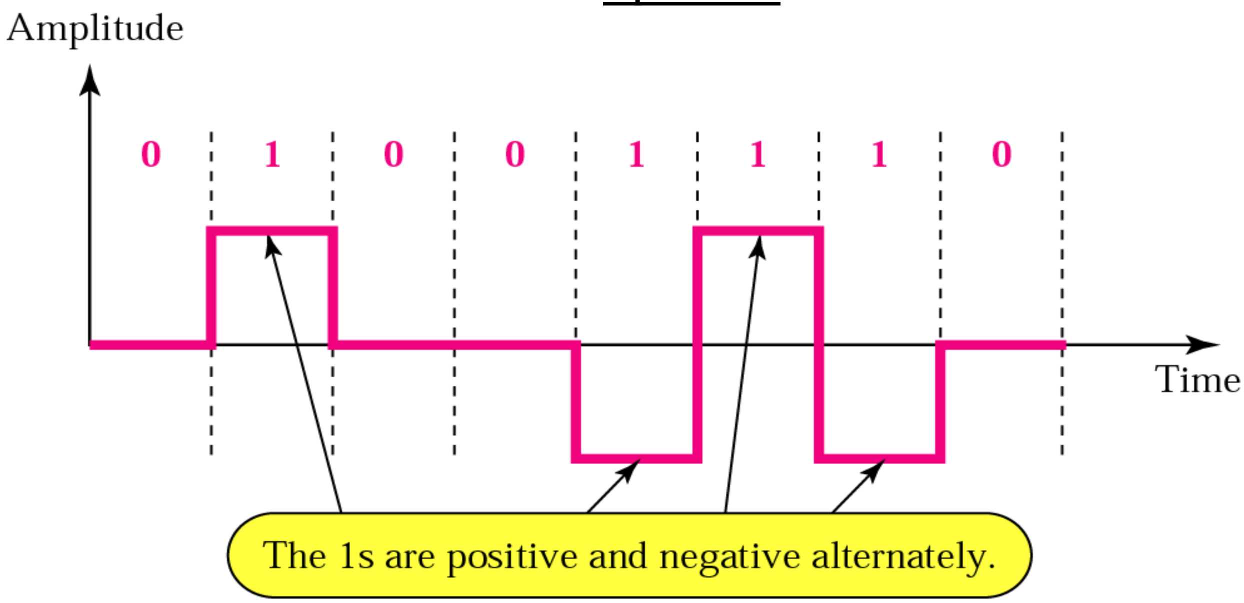
In bipolar encoding, we use three levels: positive, zero, and negative.

AMI (Alternate Mark Inversion) and **Pseudoternary** are two variations of bipolar encoding.
AMI means alternate 1 inversion. 0 voltage represents 0, alternating +ve and –ve voltages represent 1.
A variation of AMI is **pseudoternary** in which, zero voltage represents 1 and alternating +ve and –ve voltages represent 0



<u>Bipolar schemes : AMI and Pseudoternary</u>

<u>Bipolar AMI</u>



No DC component in bipolar encoding, for a long sequence of zeros voltage remains constant but amplitude is zero.

A sequence that creates a constant zero voltage does not have a DC component.

AMI commonly used for long distance communication, but has synchronization problem

<u>Multilevel Schemes</u>

The desire to increase the data speed or decrease the required bandwidth resulted in **mBnL** coding where m is the number of data elements, n is the number of signal elements, B means binary data and L is the number of signal levels.

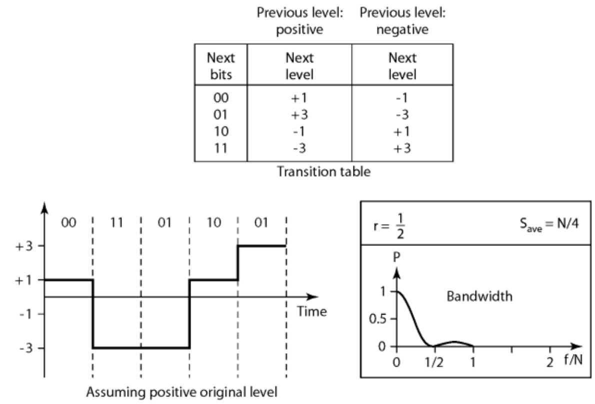
To prevent baseline wandering, to provide synchronization and to detect errors ; each data pattern is encoded into one signal pattern or less than one signal pattern

NOTE: In mBnL schemes, a pattern of m data elements is encoded as a pattern of n signal elements in which $2m \leq Ln$.

2B1Q **– two binary, one quarternary :** A mBnL scheme that uses data patterns of size 2 and encodes the 2-bit patterns as one signal element belonging to a four level signal.
In this type of encoding m=2, n=1 and L=4

2B1Q is used in DSL technology to provide a high speed connection to the Internet using subscriber telephone lines.
No self synchronization for long same double bits.

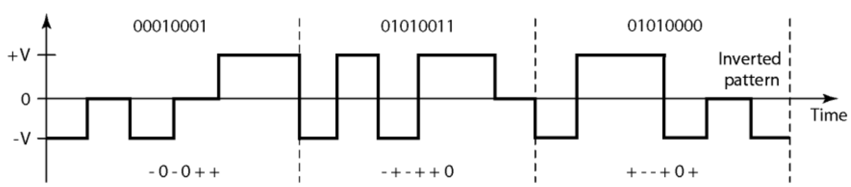
Average signal rate is *S= N/4*



2B1Q scheme

***8B6T* - eight binary, six ternary :** Encode a pattern of 8 bits as a pattern of 6 signal elements.
In this scheme, we can have 2^8= 256 different data patterns and 3^6= 476 different signal patterns.
The three possible signal levels are represented as **-, 0 and +**
For Ex: The 8-bit pattern 00010001 is encoded as signal pattern -0-0++, the pattern 01010011 is encoded as -+-++0 .
Each signal pattern has a weight of 0 or +1 DC values.
To make the whole stream DC-balanced,the sender keeps track of the weight.
If two groups of weight 1 are encountered one after another, the first one is sent as it is,while the next one is sent totally inverted to give a weight of -1.

Average signal rate is 6N/8

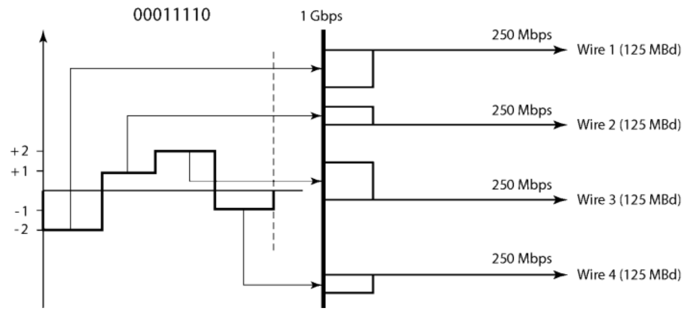


8B6T scheme

4D-PAM5 : Four-dimensional five-level pulse amplitude modulation

4D means 4 signal elements comprising one signal group is sent over four wires at the same time.
Uses five voltage levels such as -2, -1, 0, 1, 2 level 0 is used for forward error detection
On assuming code as 1 dimensional, 4 levels create something similar to 8B4Q.

Average signal rate is N/8.

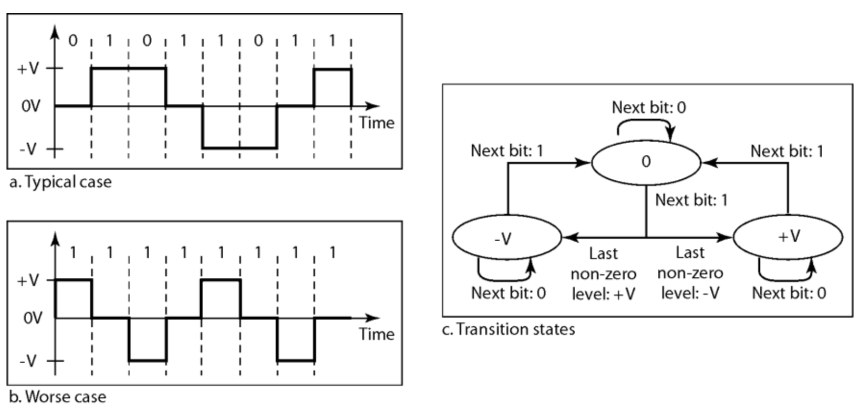


4D-PAM5 scheme

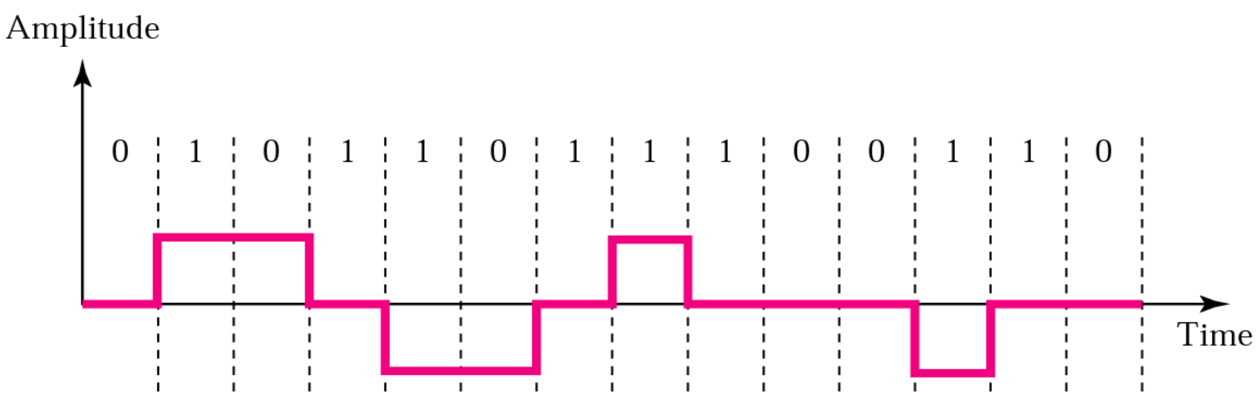
Multiline Transmission 3 Level: MLT-3

A differential encoding scheme with more than two transition rules can be designed for a signal having more than two levels.
MLT-3 uses three levels (+V, 0, -V) and 3 transition rules as below

If the next bit is 0, there is no transition
If the next bit is 1 and current level is not 0, the next level is 0.
If the next bit is 1 and the current level is 0, the next level is the opposite of the last nonzero level



MLT-3 scheme



Why MLT-3, a scheme that maps one bit to one signal element, same as that for NRZ-I, but with greater complexity?

At the worst case the signal element pattern +V0-V0 is repeated every 4 bits.

Means a non periodic signal has changed to a periodic signal with period equal to 4 times the bit duration.

This is equivalent to saying that the signal rate for MLT-3 is one-fourth the bit rate.

MLT-3 a suitable choice for sending 100Mbps on a copper wire that cannot support more than 32 MHz.

Category	*Scheme*	*Bandwidth (average)*	*Characteristics*
Unipolar	NRZ	$B = N/2$	Costly, no self-synchronization if long 0s or 1s, DC
Unipolar	NRZ-L	$B = N/2$	No self-synchronization if long 0s or 1s, DC
	NRZ-I	$B = N/2$	No self-synchronization for long 0s, DC
	Biphase	$B = N$	Self-synchronization, no DC, high bandwidth
Bipolar	AMI	$B = N/2$	No self-synchronization for long 0s, DC
Multilevel	2B1Q	$B = N/4$	No self-synchronization for long same double bits
	8B6T	$B = 3N/4$	Self-synchronization, no DC
	4D-PAM5	$B = N/8$	Self-synchronization, no DC
Multiline	MLT-3	$B = N/3$	No self-synchronization for long 0s

Block Coding

Block Coding improves the performance of line coding by providing redundancy

Block coding changes a block of m bits into a block of n bits, where n is larger than m, known as ***mB/nB encoding*** technique.

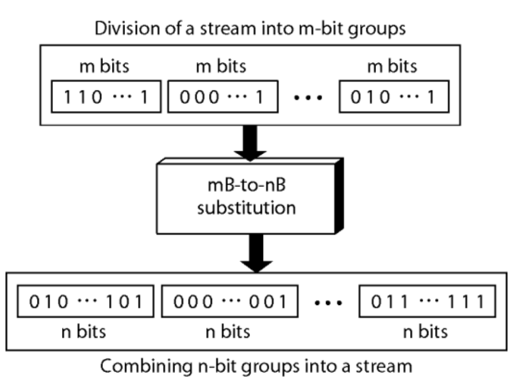
Block coding involves three steps: *Division, substitution and combination.*

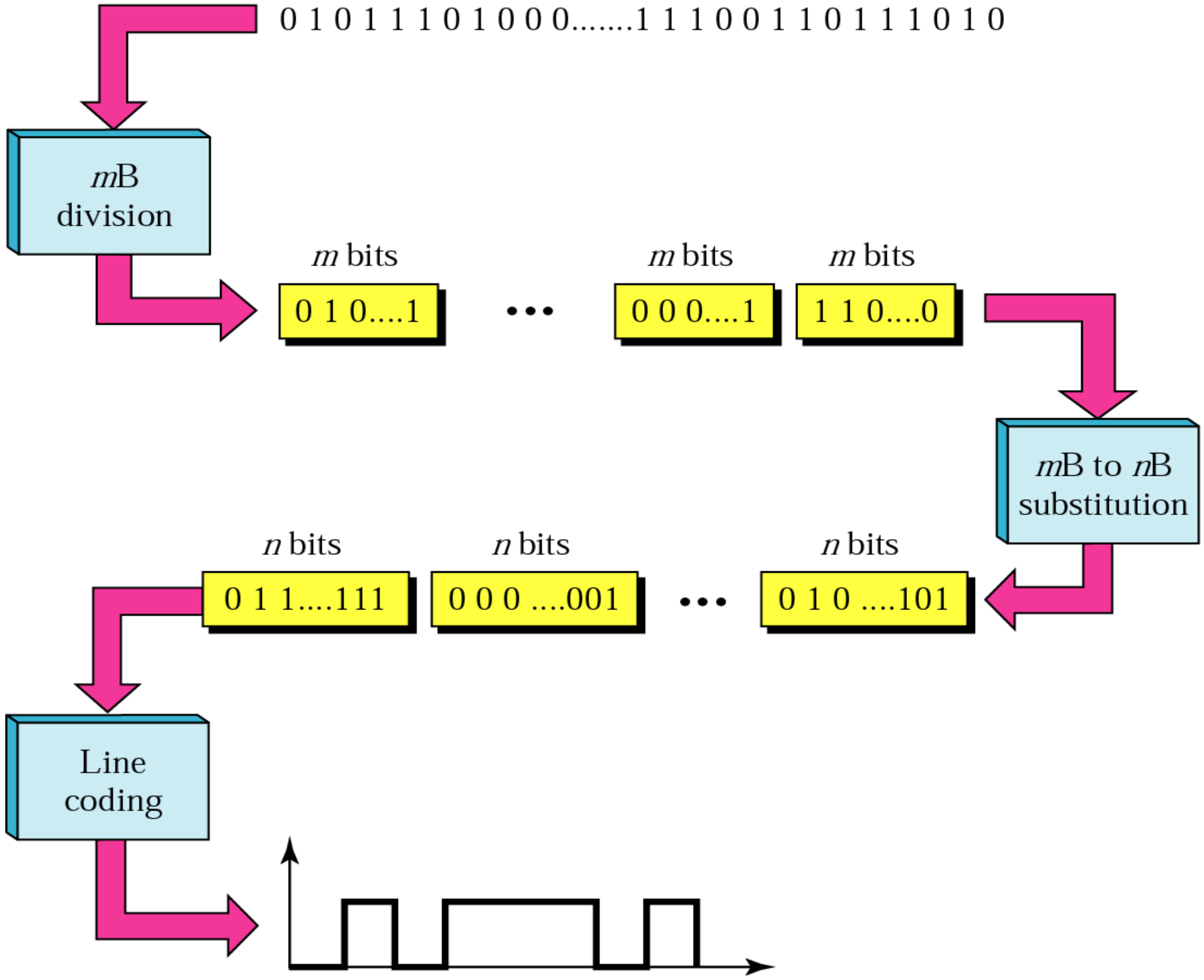
In division step, a sequence of bits is divided into groups of m bits.

In substitution step, an m-bit group is substituted for an n-bit group

In combination step, the n-bit groups are combined to form a stream

NOTE: Block coding is normally referred to as mB/nB coding it replaces each m-bit group with an n-bit group.



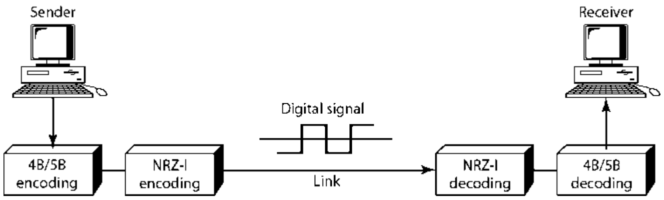


4B/5B: The four binary/five binary scheme is used in combination with NRZ-I.

Recall that NRZ-I has a synchronization problem with long sequence of 0s.

Solution to this is to change the bit stream prior to encoding with NRZ-I, so that it does not have long sequence of zeros.

At the receiver, the NRZ-I encoded signal is first decoded into stream of bits and then decoded to remove the redundancy.



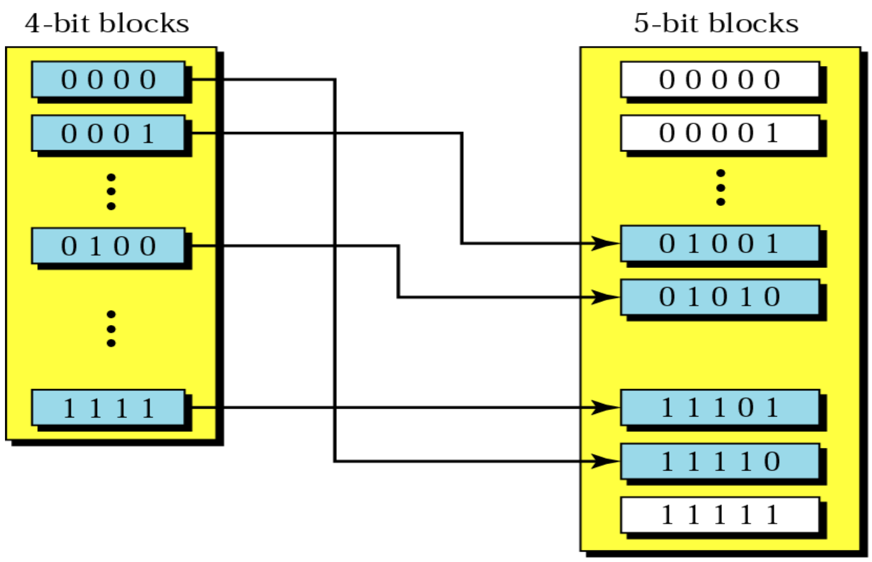
The 5-bit output that replaces 4-bit input has no more than 1 leading zero, and no more than 2 trailing 0s.

So when different groups are combined, there are never more than 3 consecutive zeros.

A group of 4 bits can have only 16 combinations, while a group of five bits can have 32 different combinations, this means 16 groups are not used for 4B/5B encoding.

Some of these 16 groups are used for control purposes and some are not used at all.

If a 5-bit group that belongs to unused portion arrives, the receiver knows that there is an error in the transmission.



4B/5B encoding solves the problem of synchronization, However the redundant bits add 20% more baud.

4B/5B block encoding does not solve the DC component problem.
If DC is unacceptable biphase or bipolar encoding need to be used.

Data	*Code*	*Data*	*code*
0000	***11110***	*1000*	***10010***
0001	***01001***	*1001*	***10011***
0010	***10100***	*1010*	***10110***
0011	***10101***	*1011*	***10111***
0100	***01010***	*1100*	***11010***
0101	***01011***	*1101*	***11011***
0110	***01110***	*1110*	***11100***
0111	***01111***	*1111*	***11101***

Control sequence	***Unused Code***
Q (Quiet)	***00000***
I (Idle)	***11111***
H (Halt)	***00100***
J (start delimiter)	***11000***
K (start delimiter)	***10001***
T (end delimiter)	***01101***
S (Set)	***11001***
R (Reset)	***00111***

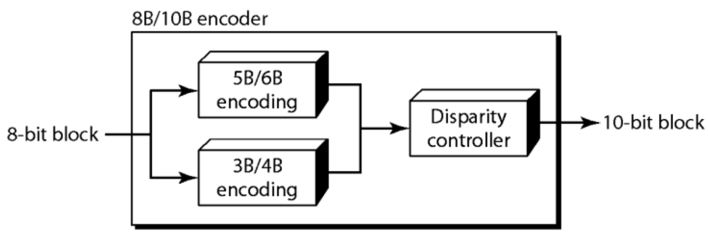
We need to send data at a 1-Mbps rate. What is the minimum required bandwidth, using a combination of 4B/5B and NRZ-I or Manchester coding?

Solution

First 4B/5B block coding increases the bit rate to 1.25 Mbps. The minimum bandwidth using NRZ-I is N/2 or 625 kHz. The Manchester scheme needs a minimum bandwidth of 1 MHz. The first choice needs a lower bandwidth, but has a DC component problem; the second choice needs a higher bandwidth, but does not have a DC component problem.

8B/10B – eight binary / ten binary

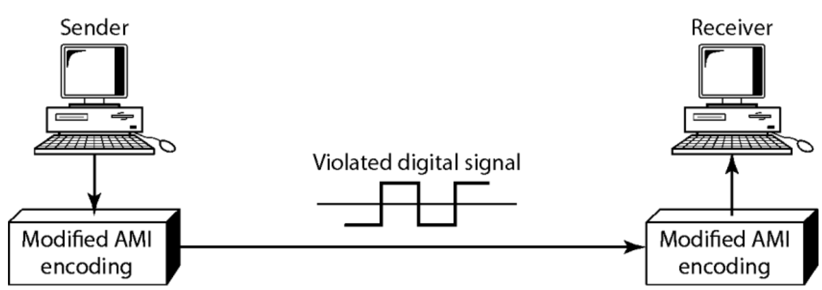
Here 8-bit code is substituted by a 10-bit code, thereby provides greater error detection capability.
8B/10B block coding is actually a combination of 5B/6B and 3B/4B.
The most 5 significant bits is fed into 5B/6B encoder and the least 3 significant bits is fed into 3B/4B encoder.
To prevent long run of consecutive 0s or 1s , the code uses a disparity controller which keeps track of excess 0s over 1s



Scrambling

Biphase schemes are not suitable for long distance communication b’coz of their wide bandwidth requirement.
The combination of block coding and NRZ line coding is not suitable for long distance encoding b’coz of DC component.
Bipolar AMI encoding has a narrow bandwidth and does not create DC component. However long sequence of zeros upsets synchronization.

Scrambling is one solution that substitutes long zero-level pulses with a combination of other levels thus making Bipolar AMI suitable for long distances
Scrambling as opposed to block coding, is done at same time as encoding
Two common scrambling techniques are B8ZS and HDB3

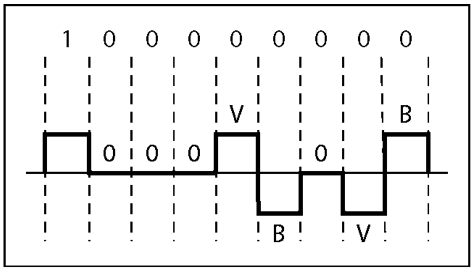


B8ZS – Bipolar with 8-zero substitution

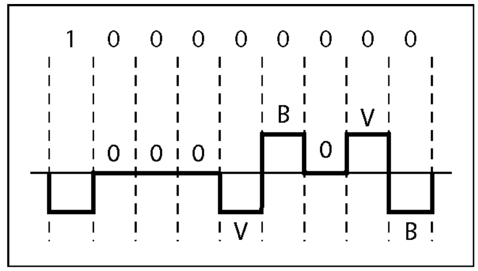
Eight consecutive zero level voltages are replaced by the sequence **000VB0VB**.

V denotes **violation;** non-zero voltage that breaks AMI rule (V means same polarity from the previous).

B denotes ***bipolar*;** non-zero voltage in accordance with AMI rule (B means opposite polarity from the previous).



a. Previous level is positive.



b. Previous level is negative.

This technique balances the positive and negative voltage levels,means DC balance is maintained.
After substitution AMI needs to follow its rules.
V means same polarity as the polarity of the previous nonzero pulse;
B means the polarity of the previous nonzero pulse.

HDB3 – High-density bipolar 3-zero

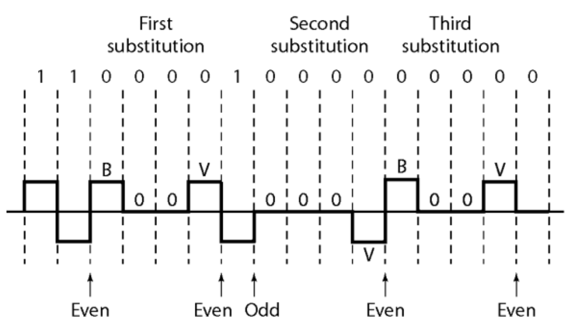
Four consecutive zero-level voltages are replaced with a sequence of 000V or B00V.

Two different substitutions is to maintain even number of non zero pulses.

If the number of non-zero pulses after the last substitution is odd, the substitution pattern will be **000V.**

If the number of non-zero pulses after the last substitution is even, the substitution pattern will be **B00V**.

Note: After each substitution must follow its own rule.



Before first substitution, the number of nonzero pulses is even, substitution is B00V.

Analog to digital conversion

Convertion of Analog signals to digital data:

Two techniques are used,

- Pulse Code modulation.
- Delta Modulation.

Once analog signals are converted to digital data ,then it is converted as digital signals and transmitted.

Pulse Code Modulation (PCM)

The most common technique to change an Anolog signal to digital data is called PCM.
A PCM encoder has 3 processes .
* Sampling
* Quantizing
* Encoding

Components of PCM encoder

- The Analog signal is Sampled
-
- The Sampled Signal is Quantised.
-
- The Quantised values are encoded as stream of bits.

SAMPLING

The analog signals is sampled every T_s S, where T_s is sampled interval or period.

Inverse of the Sampling interval is called the Sampling rate or sampling frequency denoted by F_s.

$F_s = 1/ T_s$.

Three sampling methods are available

Ideal
Natural
Flat-Top

In Ideal sampling pulses from the analog signal are sampled.It cannot be easily implemented In Natural Sampling ,a high speed switch is turned on for only the small period of time when sampling occurs.Here samples retain shape of analog signals.

- **Sample and Hold**:it creats Flat-Top Samples by using a circuit.
- **Sampling process** is also called as pulse amplitude modulation(PAM).
- **Sampling Rate** :According to Nyquist therom to reproduce original analog signal ,one codition is sampling rate be at least twice the highest frequency in the original signal.

We can sample a signal only if it is baud limited .A signal with an infinite bandwidth cannot be sampled. Sampling rate must be atleast 2 times the highest freq,not the between.

Quantization:

The result of sampling is a series of pulses with amplitude values between the max and min amplitude of the signal.

The set of amp can be infinite with nou integral values b/w the two limits.

The values cannot be used in encoding

We assume that the original analog signal has instantanious amp b/w Vmin & Vmax.

We divide the range into L zone,each of height ∂ .

∂=Vmax-Vmin/L
=20-(-20)/8=5.

We assugn quation values of 0 to L-1 to on the point of each zone.

We approximate the values of the sample amp to the quantized valueas.

Normalized PAM values	-1.22	1.50	3.24	3.94	2.20	-1.10	-2.26	-1.88	-1.2.
Normalized quantized values	-1.50	1.50	3.50	3.50	2.50	-1.50	-2.50	-1.50	-1.50
Normalized error	-.38	0	0.26	-0.44	0.30	-0.40	-0.24	0.38	-0.30

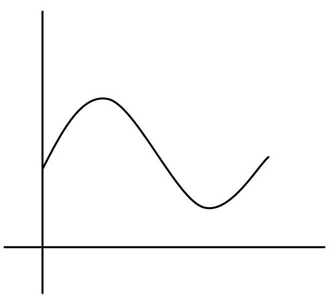
Quantization code 2 5 7 7 6 2 1 2 2

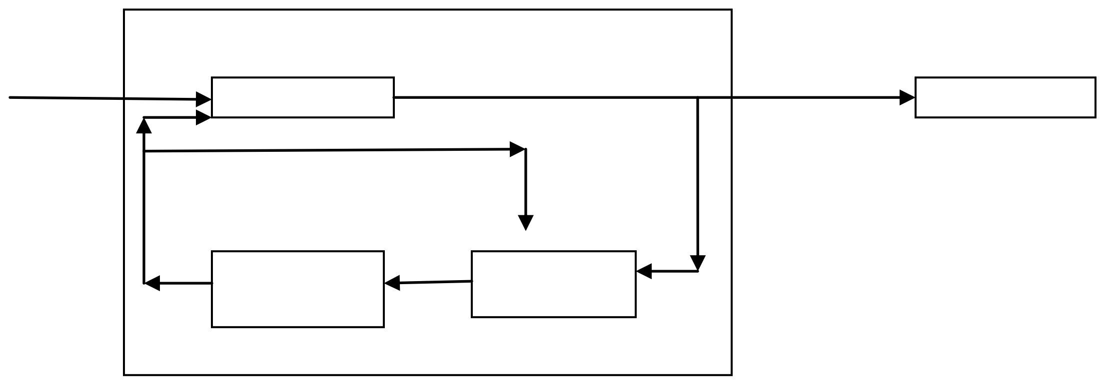
Encoded words 010 101 111 111 110 010 001 010 010

Modulator: Is used at the sender file to

1 Create a stream of bits from an analog signal.
2 The process records the small positive or negative changes, called ∂.
3 If ∂ is positive, the process records 1, if ∂ is negative the process records 0.

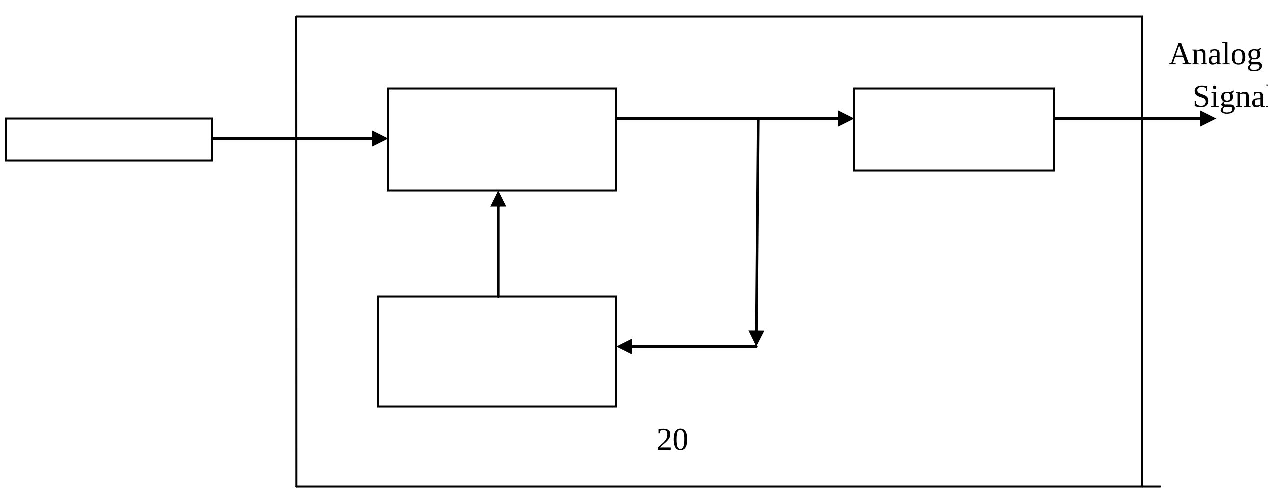
Delta modulation component





4. The modulator at each sampling interval compares the value of the analog signal with the last value of the staircase signal.
5. Amplitude of the analog signal is larger, the next bit in digital data is 1, otherwise it is 0.
6. The output of the comparator, makes staircase itself, if the next bit is 1, the staircase maker moves to last point of staircase signal ∂ up, if the next bit is 0, ∂ down.
7. We need a delay unit to hold the ∂ function for a period between two components.

Demodulator

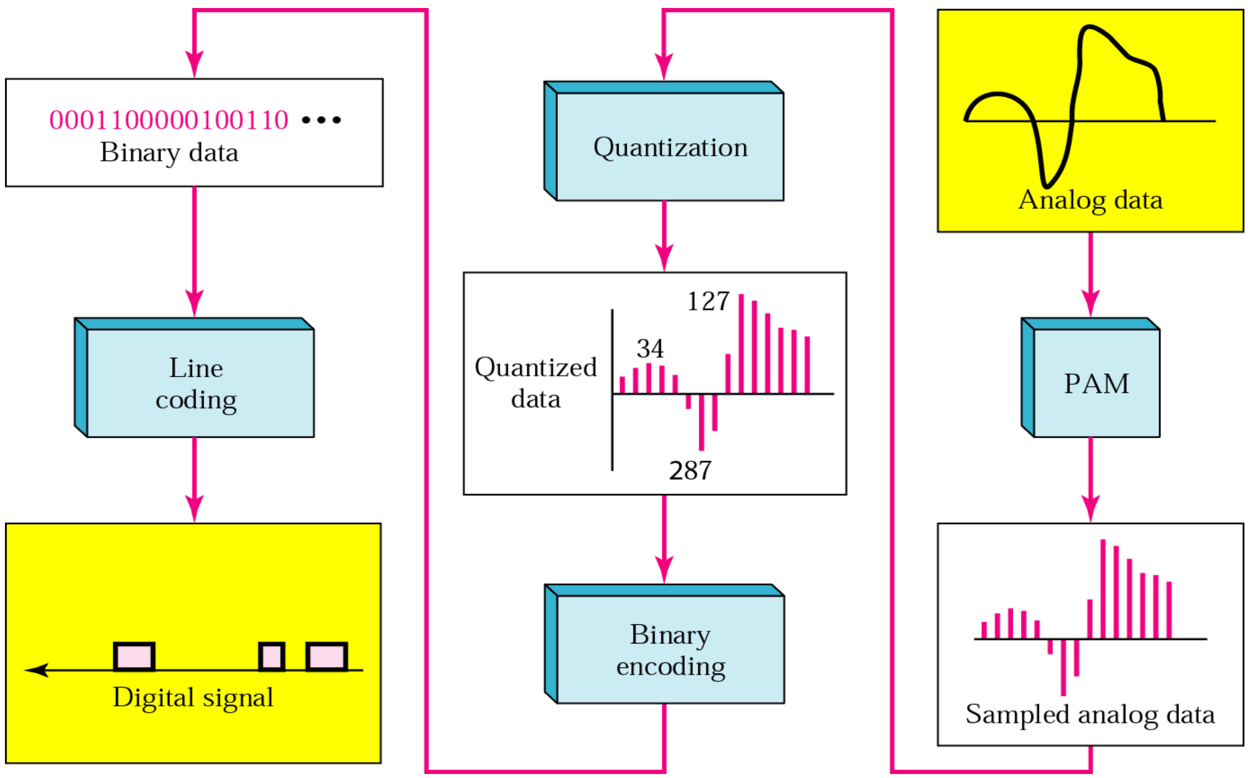


Adaptive delta modulation

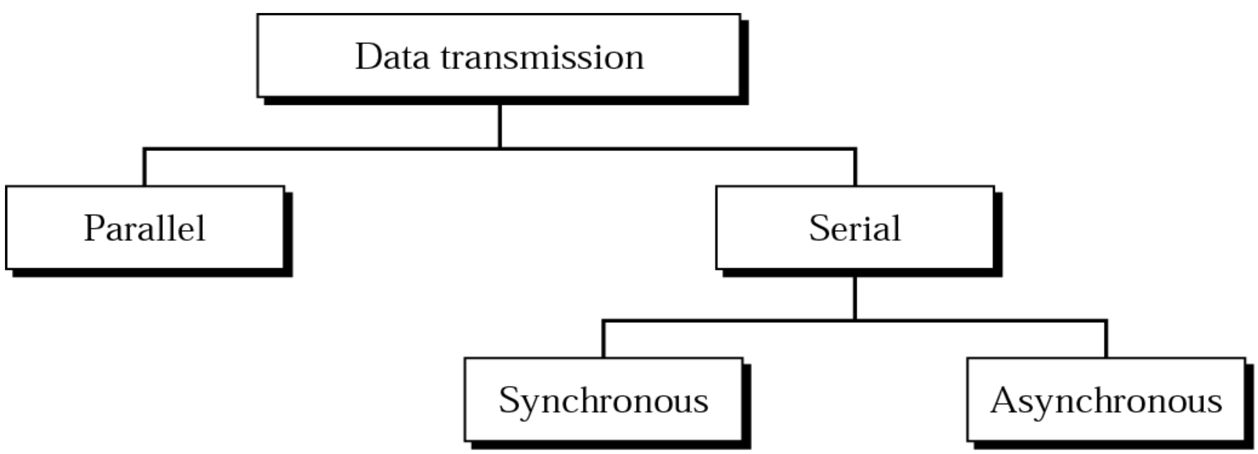
1. Better performance can be achieved if the value of ∂ is not fixed.
2. In adaptive delta modulation the value of ∂ changes according to the amplitude of analog signal.

Quantization Error

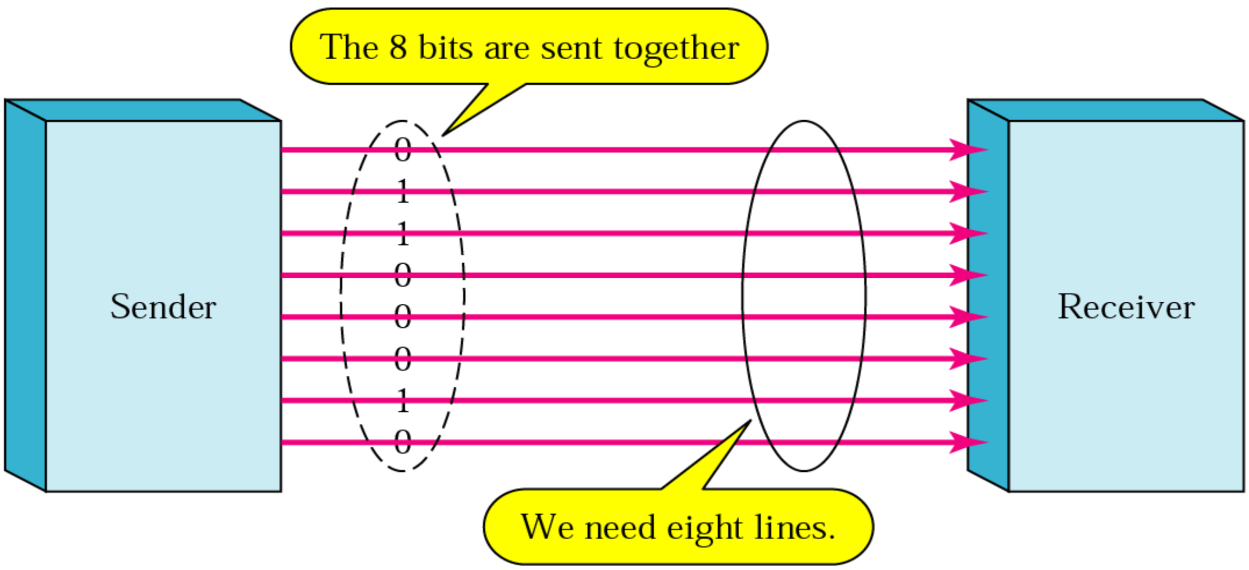
1. Delta modulation is not perfect; quantization error is introduced in process.
2. Quantization of DM is much less than that for PCM.



The transmission of binary data across a link can be accomplished in either parallel or series mode. In parallel mode, multiple bits are sent with each clock tick. In serial mode, 1 bit is sent with each clock tick. While there is only one way to send parallel data, there are 3 subclasses of serial transmission: asynchronous, synchronous, and isochronous (see figure 4.31)



Parallel transmission
Binary data, consisting of 0's and 1's,may be organized into groups of n bits each .by grouping ,we can send data n bits at a time instead of 1.this is called parallel transmission.
The mechanism for parallel transmission is a conceptually simple



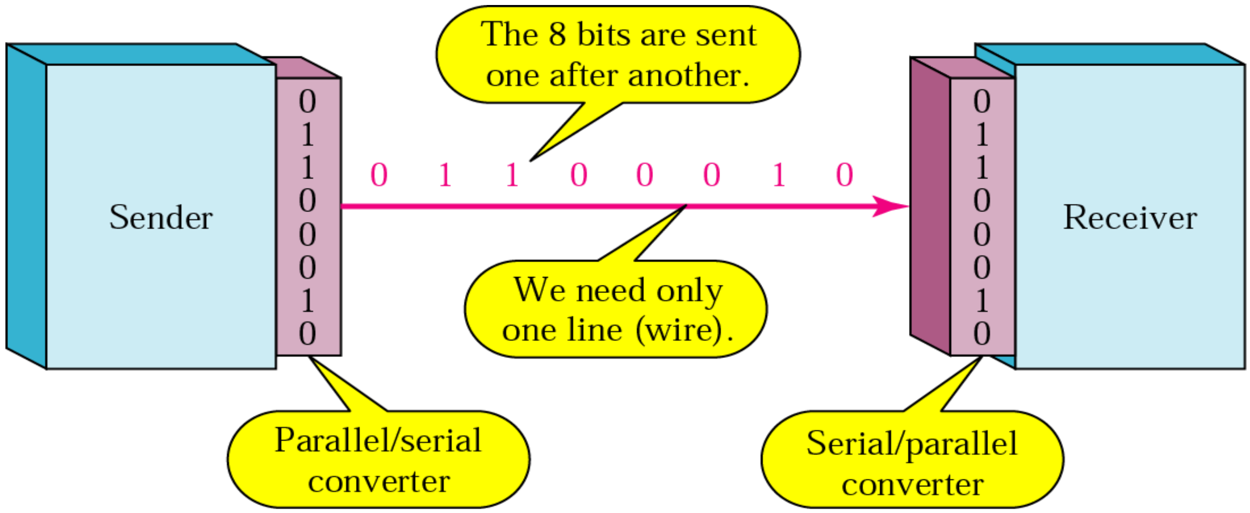
Parallel transmission
The mechanism for parallel is a conceptually simple one: Use n wires to send n bytes at one time. That way each bit has its own wire, and all n bytes of one group can be transmitted with each clock tick from one device to another. Figure4.32 shows how parallel transmission works for n=8. Typically, the 8 bundles are bundled in a cable with a connector at each end.

The advantage of parallel transmission is speed. All else being equal, parallel transmission can increase the transfer speed by a factor of n over serial transmission.

But there is a significant advantage: cost. Parallel transmission requires communication lines (wires in the example) just to transmit the data stream. Because this is expensive, parallel transmission is usually limited to short distances.

Serial transmission
In serial transmission one bit follows another, so we need only one communication channel rather than n to transmit data between two communicating devices (see figure 4.33).
The advantage of serial over parallel transmission is that with only one communication channel, serial transmission reduces the cost of transmission over parallel by roughly a factor of n.

Since communication within devices is parallel, conversion devices are required at the interface between the sender and the line (parallel-to-serial) and between the line and the receiver (serial-to-parallel).



Serial transmission occurs in one of three ways: asynchronous, synchronous, and isochronous.

Asynchronous Transmission

Asynchronous transmission is so named because the timing of a signal is important. Instead, information is received and translated by agreed upon patterns. As long as those patterns are followed, the receiving device can retrieve the information without regard to the rhythm in which it is sent. Patterns are based on grouping the bit stream into bytes. Each group, usually 8 bits, is sent along the link as a unit. The sending system handles each group independently, relaying it to the link whenever ready, without regard to a timer.

To alert the receiver to the arrival of a new group, therefore, an extra bit is added to the beginning of each byte. This bit, usually a 0, is called the start bit. To let the receiver know that the byte is finished, 1 or more additional bits are appended to the end of the byte. These bits, usually 1s, are called stop bits.

In asynchronous transmission, we send 1 start bit (0) at the beginning and 1 or more stop bits (1s) at the end of each byte. There may be a gap between each byte.

The start and stop bits and the gap alert the receiver to the beginning and end of each byte and allow it to synchronize with the data stream. This mechanism is called asynchronous because, at the byte level, the sender and receiver do not have to be synchronized.

The receiving device resynchronizes at the onset of each new byte. When the receiver detects a start bit, it sets a timer and begins counting bits as they come in. After n bits, the receiver looks for a stop bit. As soon as it detects the stop bit, it waits until it detects the next start bit.

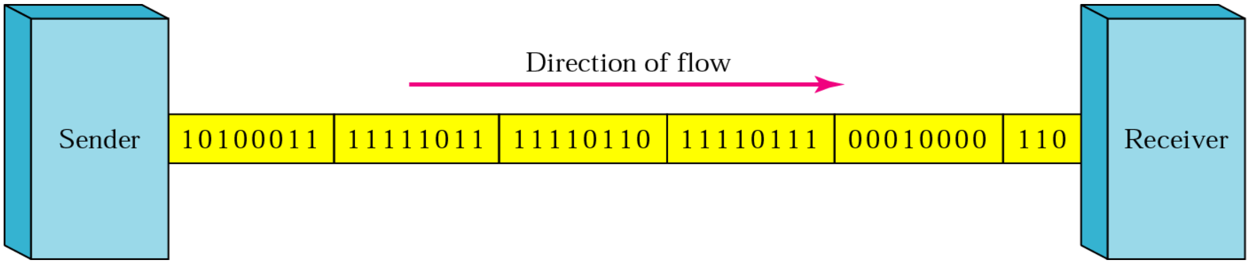
Asynchronous here means “asynchronous at the byte level,” but the bits are still synchronized; their durations are the same.

For example, the connection of a keyboard to a computer is a natural application for asynchronous transmission.

Synchronous Transmission

In synchronous transmission, the bit stream is combined into longer “frames,” which may contain multiple bytes. Each byte, however, is introduced onto the transmission link without a gap between it and next one. It is left to the receiver to separate the bit stream into bytes for decoding purposes. In other words, data are transmitted as an unbroken string of 1s and 0s, and the receiver separates that string into the bytes, or characters, it needs to reconstruct the information.

In synchronous transmission, we send bits one after another without start/stop bits or gaps. It is the responsibility of the receiver to group the bits.



In synchronous transmission, we send bits one after another without start or stop bits or gaps. It is the responsibility of the receiver to group the bits.

Figure 4.35 gives a schematic illustration of synchronous transmission. The advantage of synchronous transmission is speed.

We need to emphasize one point here. Although there is no gap between characters in synchronous serial transmission, there may be uneven gaps between frames.

Isochronous Transmission

The isochronous transmission guarantees that the data arrive at a fixed rate.