ZHEYUAN CHEN

+1 2017797262
sephirotheca17@gmail.com

EDUCATION

University of California, Santa Cruz *Sept 2024 - Present*
PhD, Computer Science and Engineering

RESEARCH & WORK EXPERIENCE

Microsoft Research Jun 2025 – Sep 2025
Research Intern, RiSE Group *Redmond, WA*

- Applied SIMT-Step semantics to shader development, focusing on warp execution correctness in HLSL.
- Built a Clang-AST–based interpreter and fuzzing framework for HLSL to automatically generate warp execution tests.
- Implemented a reducer to minimize failing tests into conformance test suites, enabling systematic validation across GPU vendors.
- Identified and reported warp execution bugs under non-uniform control flow across NVIDIA, Intel, and AMD GPUs.
- Extended HLSL testing infrastructure with more flexible test definitions, increasing coverage and long-term maintainability.

Mercedes-Benz Research & Development North America Jun 2024 – Dec 2024
Software Engineering Intern *Sunnyvale, CA*

- Contributed to building middleware for automated driving systems (ADS) to ensure reliable communication, data flow, and resource sharing across safety-critical components.
- Developed an automated toolchain to migrate a large Bazel project (CUDA/C++) to SYCL, reducing manual effort by 90% and improving portability across heterogeneous hardware.

Languages, Systems, and Data (LSD) Lab Jan 2023 – Present
Research Assistant *University of California, Santa Cruz*

- Developed **SIMT-Step**, a formal operational semantics for GPU warp execution, addressing the lack of rigorous semantic models in existing GPU programming languages.
- Introduced **dynamic blocks**, a novel semantic construct for precisely modeling converged execution of warps under collective, synchronous, and independent instruction variants.
- Conducted a large-scale GPU fuzzing campaign (700+ hours across 9 GPUs from 7 vendors), utilizing GraphicsFuzz, fuzzing framework for GLSL, revealing weak behaviors on several devices that are absent from official specifications.

PUBLICATIONS

Yanwen Xu, Rithik Sharma, **Zheyuan Chen**, Shaan Mistry, and Tyler Sorensen. "BetterTogether: An Interference-Aware Framework for Fine-grained Software Pipelining on Heterogeneous SoCs." *IEEE International Symposium on Workload Characterization (IISWC)*, Accepted, 2025.

SKILL

- **Language**: Rust, C/C++, Python, Go, HLSL, GLSL, SPIR-V, TLA+
- **Framework**: CUDA, SYCL, Vulkan, HIP, OpenCL, LLVM, MLIR