

Programmable Analog-to-Digital Converter Array Supporting Architecture Restructuring and Mode Concurrency

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Abstract—This work presents a new analog-to-digital converter (ADC) architecture named programmable converter array (PCA) for multi-standard signal acquisition. Unlike prior reconfigurable ADCs that are mainly configured at the circuit level, PCA is highly flexible at the architecture level and can process multiple input signals simultaneously for mode concurrency. The elemental units in the converter array are Conversion Blocks (CBs) based on successive approximation register (SAR) ADCs. Multiple CBs can interleave or run synergically through a bus system to form sophisticated architectures. Fabricated in 28nm CMOS, the prototype converter array can be configured as over 16 modes, with an SNDR range from 30dB to 82dB and an aggregate bandwidth from sub-MHz to 1000MHz. The prototype achieves a peak Schreier figure of merit (FoMs) of 176dB while maintaining FoMs over 165dB in most configurations, and occupies only 0.1mm² of silicon area.

Index Terms—Analog-to-digital converter (ADC), reconfigurable, programmable, array, architecture-level, concurrency.

I. INTRODUCTION

ANALOG-TO-DIGITAL converters (ADCs) have made significant progress in speed, accuracy, and energy efficiency, yet their multi-functionality remains limited. To meet the requirements for multi-specification signal acquisition, the conventional solution is to deploy multiple dedicated ADCs, each tailored for specific requirements, ensuring optimal performance, power and area (Fig. 1(a)). However, this strategy becomes inflexible as the number of modes in a signal chain grows. In modern mobile transceivers [1], [2], the number of ADCs can exceed dozens, occupying substantial silicon area and incurring considerable R&D costs. This challenge

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is expected to escalate as wireless standards continue to evolve. In addition to using multiple dedicated ADCs and using a power-hungry wideband ADC (Fig. 1(b)) [3], [4], [5], [6] to implement software-defined radios, multi-mode or reconfigurable ADC (Fig. 1(c)) provides an alternative solution and has received widespread attention [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30]. However, most existing multi-mode or reconfigurable ADCs fail to demonstrate substantial cost advantages in addressing multiple A/D requirements.

Reported multi-mode or reconfigurable ADCs primarily fall into two categories. The first category focuses on parameter tuning on a specific ADC architecture. This approach is common in reconfigurable Delta-Sigma Modulators (DSM) [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], where the sampling rate, oversampling ratio (OSR), loop filter, and quantizer are tunable to adjust the bandwidth, accuracy, and power consumption. Similar strategies can also be utilized in other architectures, such as pipelined [20], [21], successive approximation register (SAR) [22], [23], flash [24], counting [25] and zoom [26], [27]. Although some reconfigurability has been achieved, performance coverage is limited since each ADC architecture operates optimally within a specific range. For example, DSM-based ADCs struggle with wideband inputs, while flash-based ADCs are hard to support high-resolution.

The second category emphasizes architecture-level reconfiguring to leverage distinct architectural advantages. Examples include [28], [29], [30] that switches between two or three architectures (typically DSM for high accuracy and pipeline/flash for high speed), enabling broader performance coverage. Although this strategy offers greater reconfigurability, it still faces two significant limitations similar to the first category, resulting in a lack of competitive performance and cost advantage:

(1) Inferior performance and efficiency compared to the single-mode counterparts, as shown in Fig. 2. A key reason for the performance loss is the challenge of optimizing circuit

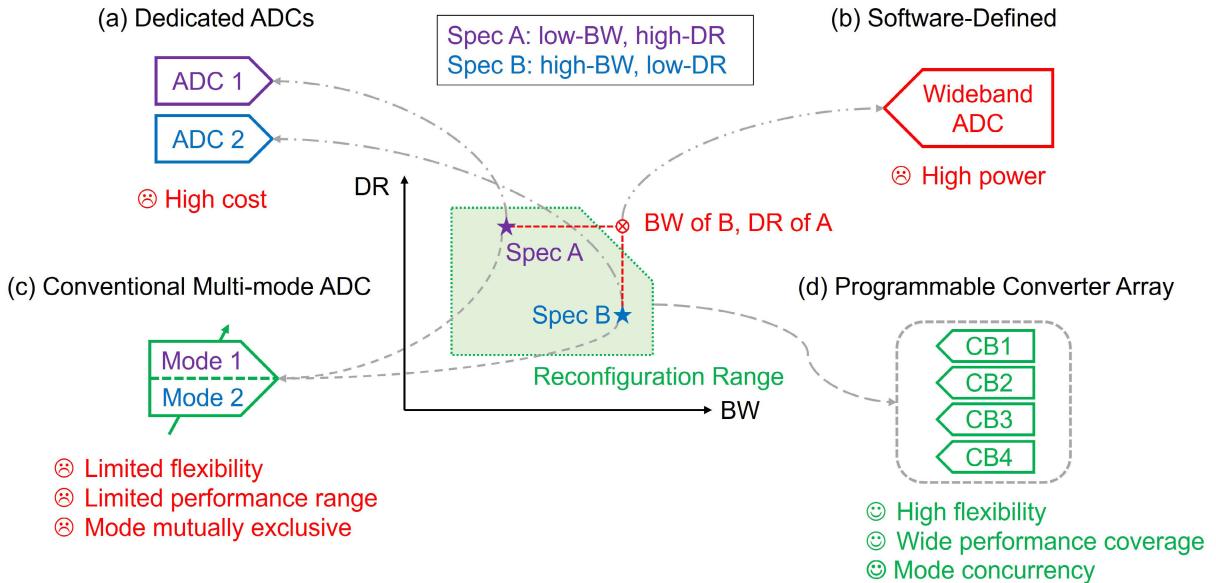
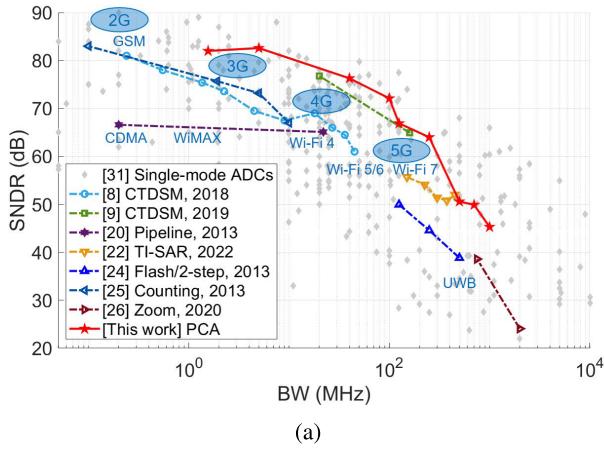
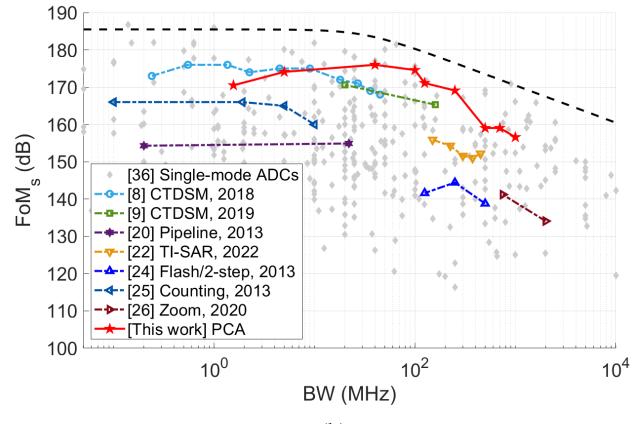


Fig. 1. ADC solutions for multi-specification signal acquisition.



(a)



(b)

Fig. 2. Performance survey of various multi-mode and single-mode ADCs [31]. (a) SNDR vs BW (b) FoM_s vs BW.

design for reconfigurability, alongside the non-negligible hardware overhead for adjustable components and switchable analog interconnects.

(2) The different modes are mutually exclusive. A multi-mode ADC can only substitute multiple single-mode ADCs that do not operate concurrently. In many practical applications, multiple signals must be captured simultaneously. Examples include processing different wireless standards, quadrature signals, carrier aggregation, beamforming, and MIMO. In these scenarios, multiple ADCs (even if reconfigurable) must be integrated onto silicon to meet concurrency requirements, undermining the area-saving benefits of using multi-mode ADCs.

To achieve multi-specification signal acquisition, we propose a novel macro-architecture named *Programmable Converter Array* (PCA), as shown in Fig. 1(d). Unlike previous reconfigurable ADCs that are largely fixed at the architecture and switched at the circuit level, PCA acts as a hardware resource pool, where reconfigurability is achieved by configuring elemental units and changing interconnections.

PCA can also support mode concurrency by dynamically decomposing into multiple sub-arrays. The homogeneity of PCA units allows for easy scalability by adding or removing elemental units. And redundant units can compensate for failures to enhance robustness. The prototype PCA can be configured into over 16 modes, covering a wide dynamic range from 30dB to 80dB, with an aggregate bandwidth range from sub-MHz to 1000MHz, which is a significant improvement over previously published reconfigurable ADCs.

This paper is an extension of [32], providing more detailed analysis and measurement results on an improved new tape-out. The rest of this paper is organized as follows. Section II presents the proposed PCA architecture. Section III illustrates the prototype implementations. Section IV presents the ADC measurement results. Finally, section V concludes the paper.

II. PROGRAMMABLE CONVERTER ARRAY

A. Basic Ideas

The elemental unit in PCA is named *Conversion Block* (CB), as shown in Fig. 3 (a). Besides an array of CBs,

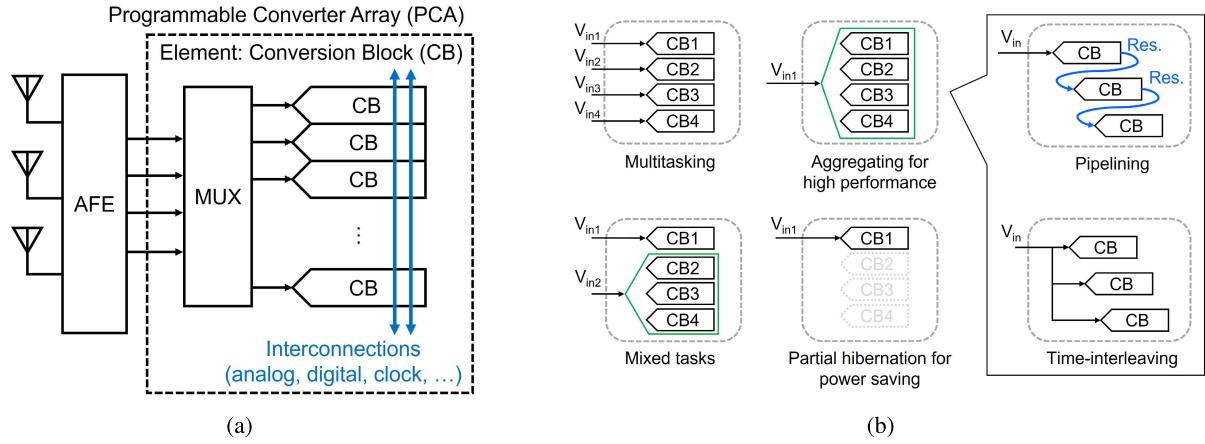


Fig. 3. (a) A general diagram of PCA. (b) Typical operation patterns of PCA.

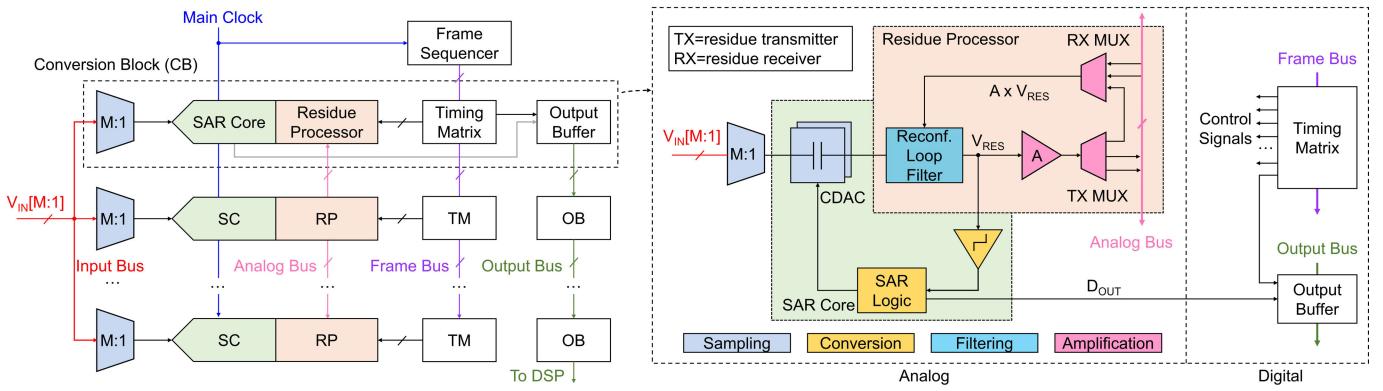


Fig. 4. Conceptual diagram of the proposed PCA architecture.

a PCA also consists of interconnection mechanisms to transmit analog, digital signals, and clocks.

Typical patterns for organizing CBs in a PCA are shown in Fig. 3 (b). Each CB can operate independently as a low-performance ADC. Multiple CBs can be combined in various ways: time-interleaved, pipelined, or parallel, to form different ADC configurations that meet diverse requirements. Upon these patterns, the CBs can be further fine-tuned to implement different performances within a specific architecture.

Effective implementation of PCA requires proper design of CB to achieve maximum architectural coverage. Among various ADCs architectures, the family of SAR ADCs stands out as a promising choice. The state-of-the-art (SoTA) SAR-based ADCs, including pipelined-SAR, time-interleaved-SAR (TI-SAR), noise-shaping-SAR (NS-SAR) [33] and further hybrid designs [34], [35], [36], [37], [38], [39], [40], [41], [42], have demonstrated high power efficiency, low area cost, and broad application range. These SAR-based ADCs fundamentally revolve around three operations: sampling, conversion, and residue processing. Different architectures are combinations and sequences of these three basic operations.

This inspires the fundamental programming mechanism behind the proposed PCA architecture: integrating necessary hardware for the three basic operations into a CB, and using a unified frame-based timetable to program the control signals for different operations. Different CBs can then operate synergically to achieve diverse A/D functions.

B. Architecture Details

The proposed PCA architecture is an array composed of multiple CBs interconnected by four bus systems, as depicted in Fig. 4. Each CB can work independently, serving as a low-power low-performance SAR ADC, while different CBs can be interleaved or collaborate synergically to form various architectures.

An *Input Bus* feeds analog inputs from different sources. Each CB can select one of the multiple input signals. Multitasking can be realized by allocating CBs to accept different inputs simultaneously. Since the CBs are always loading on the input bus whether activated or not, the input driver should be designed with sufficient driving strength to mitigate the input driving loss.

An *Analog Bus* allows the transmission of residues signals between CBs. The residue can be sent to or received from any CB, including the transmitting CB itself. The received residue is then added to the CDAC voltage, either directly or after loop filtering. This enables architectures such as pipelined-SAR and time-interleaved noise-shaping-SAR (TI-NS-SAR) [43].

A *Frame Bus* carries a set of multi-phase clocks generated from a global *Frame Sequencer*. These clocks drive a *Timing Matrix* in CBs to produce globally synchronized control signals based on a unified timetable, where the minimum time unit is named a *frame*. The Timing Matrix is essentially a crossbar array that stores the timetable of control signals, which will be detailed in Section III-E.

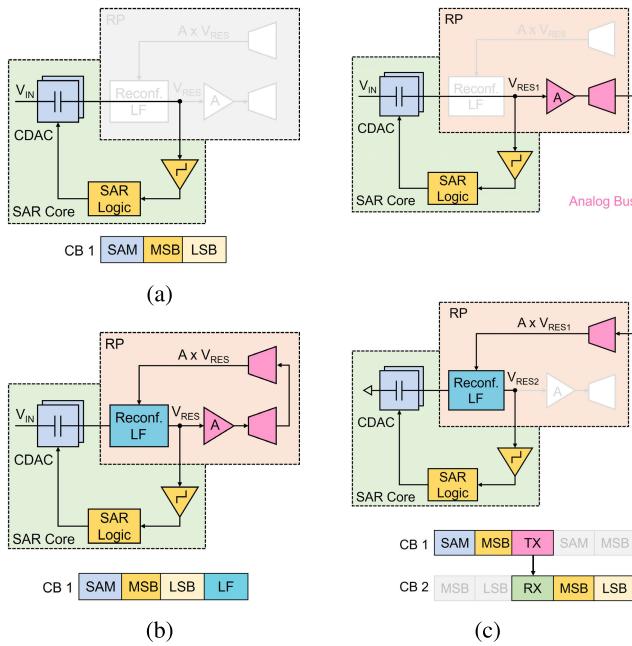


Fig. 5. Mode examples of (a) SAR, (b) NS-SAR, (c) Pipe-SAR.

In addition to the Frame Bus, there is also a main clock path running through all the CBs to provide low-jitter retiming for the timing-critical operations (i.e., sampling).

An *Output Bus* collects the data packages from CBs and sends them to the backend digital signal processor (DSP). Instead of using direct connections between CBs and the DSP, data from each CB is transferred over a shared bus (i.e., the Output Bus), and an unique address is assigned to each data package for identification. This approach significantly reduces the number of output wires, simplifies routing complexity, and minimizes silicon area.

The block diagram of each CB is illustrated in Fig. 4. Each CB contains a *SAR Core* with a front-end multiplexer for input selection. To increase flexibility, the SAR conversion is partitioned into the MSB and the LSB segments, which can be executed either solely or successively. In other words, the MSB parts of SAR conversion can be skipped to handle small input signals. A *Residue Processor*, including a reconfigurable amplifier and loop filter, handles residue amplification, filtering, and transferring. Key challenges in the PCA architecture lie in designing these high-performance, low-cost, and energy-efficient SAR Cores, Residue Processors, as well as Timing Matrixes.

C. Mode Examples

This section demonstrates the high reconfigurability of PCA using simple examples. Assume that the SAR Core in a CB is of 10-bit resolution, divided into two segments: 5-bit MSB and 5-bit LSB. By allocating one frame (assume 1ns, i.e., frame rate = 1GHz) for sampling and two frames for SAR conversion, a 330Msps 10-bit single-channel SAR ADC can be implemented (Fig. 5(a)). Additionally, enabling the loop filter (LF) after LSB conversion transforms the ADC into a NS-SAR with lower quantization noise (Fig. 5(b)).

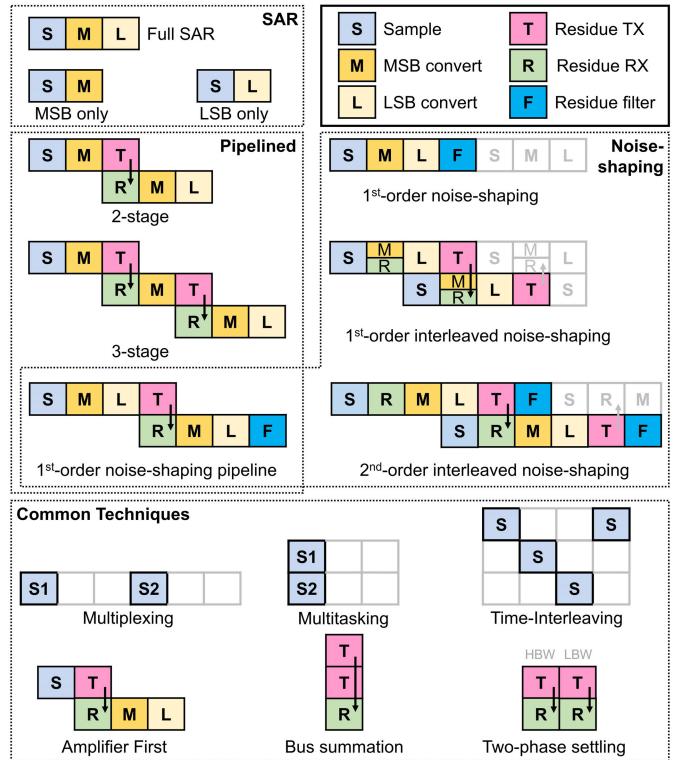


Fig. 6. Frame configuration templates for different architectures and variants.

To achieve higher performance, a single CB is insufficient. By utilizing two CBs, a 2-stage pipelined-SAR ADC can be implemented (Fig. 5(c)). The first CB performs a 5-bit SAR conversion, followed by residue amplification and transfer to the second CB for further 10-bit conversion. Under 8x interstage gain, the pipelined-SAR mode offers a resolution of 13 bits.

Beyond these simple examples, Fig. 6 showcases PCA's versatility through a broader range of configurations. This includes SAR ADCs with various resolutions, pipelined-SAR ADCs with different number of stages, and noise-shaping (NS) SAR ADCs with diverse orders for improved performance. Some hybrid architectures can also be supported, like TI-NS-SAR, pipe-NS-SAR.

Furthermore, various common techniques can be integrated, such as multitasking and time division multiplexing through configuring the input multiplexer, pre-amplification for small magnitude input signals, residue current summation on the analog bus, and multi-phase amplification with two-phase settling [44] for noise reduction. Additionally, PCA is fully dynamic and can adapt to a wide range of frame rates (clock frequency). This further enriches its applications as its sampling rate can be arbitrarily scaled. Therefore, the proposed PCA architecture demonstrates remarkable flexibility and adaptability, making it a promising candidate for multi-mode applications.

III. PROTOTYPE IMPLEMENTATIONS

A. Overview

We implement a PCA prototype consisted of six CBs, two Input Buses, two Analog Buses, 16 Frame Buses, and one

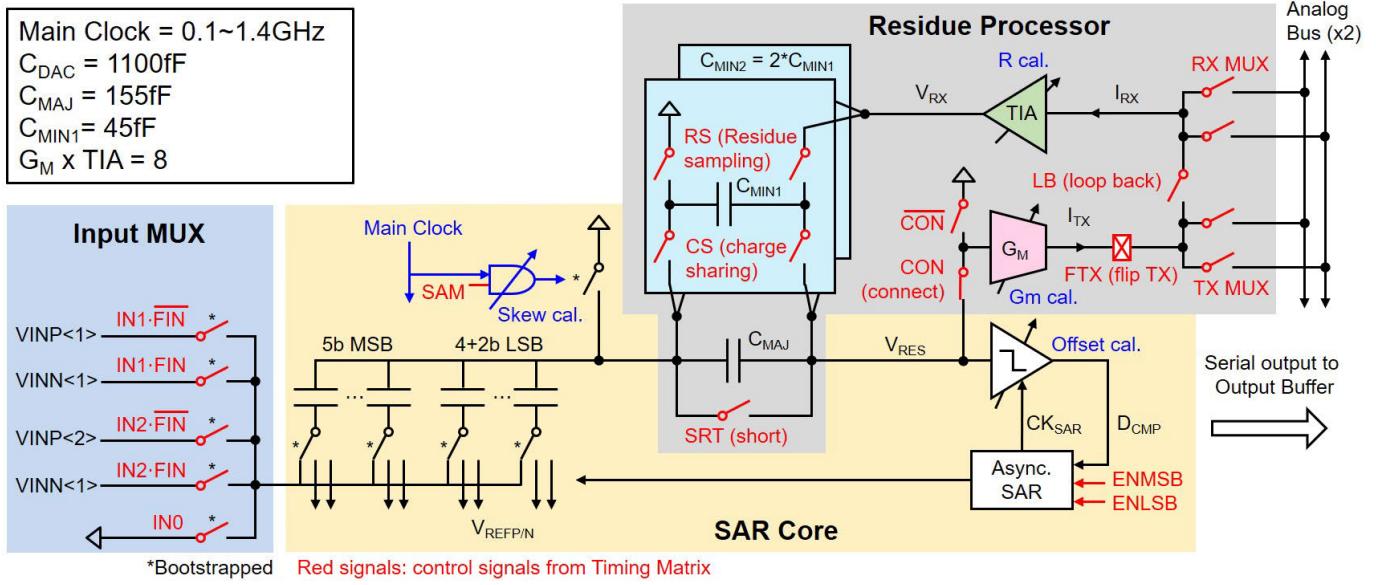


Fig. 7. Circuit implementation details of the CB.

Output Bus. The detailed implementation of a CB is shown in Fig. 7. The SAR Core is composed of a 9-bit SAR with 2-bit redundancy, divided into 5-bit MSB and 6-bit LSB. While the whole array runs synchronously, the SAR logic inside CBs is asynchronous for speed and efficiency reasons. Each CDAC is designed with a fixed total capacitance of 1100fF to suppress sampling noise in high-precision modes. However, this fixed capacitance may lead to inefficiencies in low-resolution configurations. Future designs may incorporate CDACs with variable capacitance values to address this issue. Bottom-plate sampling is adopted and a clock booster [45] is used to drive the top-plate switch to enhance linearity. The Residue Processor contains a transconductor(G_M)-transimpedance(TIA) pair and a reconfigurable 2nd-order switch-capacitor FIR filter. To handle PVT variations and mismatches, trimmers are added to fine tune the sampler's delay, comparator's offset and amplifier's gain. The sampling switch on the top plate is re-timed by the main clock to achieve low sampling jitter and skew.

B. Input Bus

To support mode concurrency, the prototype PCA equips two Input Buses to accept two sets of differential inputs. Each CB has a set of bootstrapped switches that form an input MUX in front of the bottom-plate sampling switches. The MUX selection signals are directly controlled by the Timing Matrix. As shown in Fig. 8, each CB can sample from either $VIN<1>$ or $VIN<2>$, and in either normal or inverted polarity. The polarity inversion, reserved for system chopping (detailed in Section III-D), is implemented by reusing the dummy switches for feedthrough cancellation. This approach introduces only one additional layer of switches in the input path. An input-shorting option is also embedded in the MUX for the scenarios that the SAR core receives signal from the Analog Bus only (i.e., the second stage in a pipeline). All the input MUX switches are bootstrapped using a bootstrap circuit similar to that in [46].

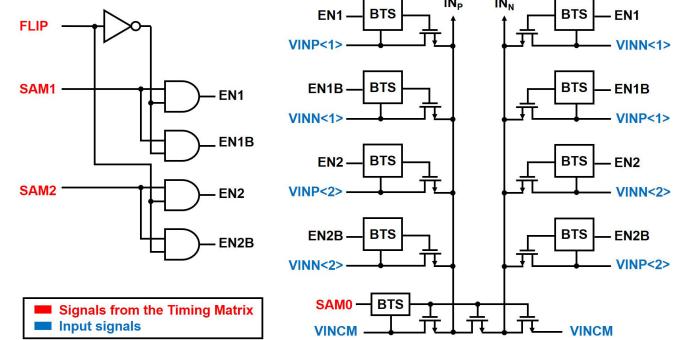


Fig. 8. Schematic of the input MUX.

Since the input signals pass through two layers of switches, the on-resistances of the MUX and the total resistance of bottom-plate sampling switches are kept below 20Ω to ensure adequate sampling bandwidth. According to simulations, the input MUX increases the sampling network's RC time constant from 22ps to 52.8ps, which is acceptable within the 800ps sampling window under 1GHz frame rate.

C. Residue Transmission

One of the key challenges in implementing the PCA is transmitting residual signals between CBs through the Analog Bus accurately and efficiently. The CB generating a residual signal may be far apart from the CB that receives this signal. PCA also need routing switches to transmit the signal flexibly. Therefore, the parasitics from the long routing and numerous switches are non-negligible for transmitting a voltage-mode signal, as they heavy load on the bus driver and significantly slow down its settling. To mitigate this problem, current-mode signals are adopted in the PCA's Analog Bus system to replace the conventional voltage-mode one, as the current-domain transmission is less sensitive to the parasitic R and C in the signal path.

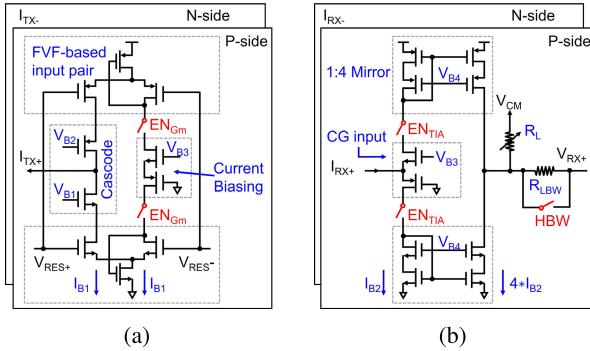


Fig. 9. Circuit implementation (single-ended) of (a) the G_M cell, (b) the TIA.

The Residue Processor contains a pair of current-mode transceivers: the transmitter is a trans-conductor (G_M cell) that converts the residue voltage (V_{res}) from SAR Core into a current (I_{TX}), and the receiver is a trans-impedance amplifier (TIA) that captures the current signals (I_{RX}) from the analog bus and converts the current back to a voltage (V_{RX}).

The cascading of G_M and TIA provides a voltage gain of $A = 8$. Both the G_M and TIA are connected to the analog bus through a MUX, by which they can send/receive the residue current signals to/from any CB. Alternatively, the output current from the G_M can also be looped back to the TIA in the same CB without occupying an Analog Bus. In addition to mitigating parasitic effects, this current-mode scheme has two additional benefits: (1) it decouples the TX's bandwidth from the RX's loading, and prevents the TX from burning extra power for load driving; (2) it supports on-bus signal summation in the current domain by Kirchhoff Current Law (KCL), which enables some performance-enhanced ADC architectures (e.g., conf. E-G in Fig. 15).

Fig. 9(a) shows the single-ended transistor-level implementation of the proposed trans-conductor. A Flipped-Voltage-Follower (FVF)-assisted pseudo-differential structure [47] is adopted for improved linearity, which produces a transconductance of 8mS. A total harmonic distortion (THD) of 40dB was achieved with a sine-wave input of 5-bit-residue magnitude. For better power efficiency, it is complementary and power gated. To prevent the gate capacitor of the input transistors from affecting the linearity of SAR core, a switch (CON in Fig. 7) is added to the input of the G_M to isolate the amplifier when it is disabled.

Fig. 9(b) shows the single-ended schematic of the proposed TIA, which is based on a common gate input stage and a current mirror gain stage. It is also complementary and power gated for efficiency consideration. The overall trans-impedance is the current mirror gain (4x) times the R_L (250Ω). Two-phase settling [44] is also adopted in the TIA as a low-noise option.

Additionally, gain trimming is achieved by adjusting the bias current of the G_M and the output resistance of the TIA. They both have 4 bits of configuration and cover a range of $\pm 10\%$. The total gain configuration range by $G_M + TIA$ is $\pm 21\%$.

D. Residue Injection and Filtering

The residue received by TIA is processed by a switched-capacitor system consisting of a major capacitor

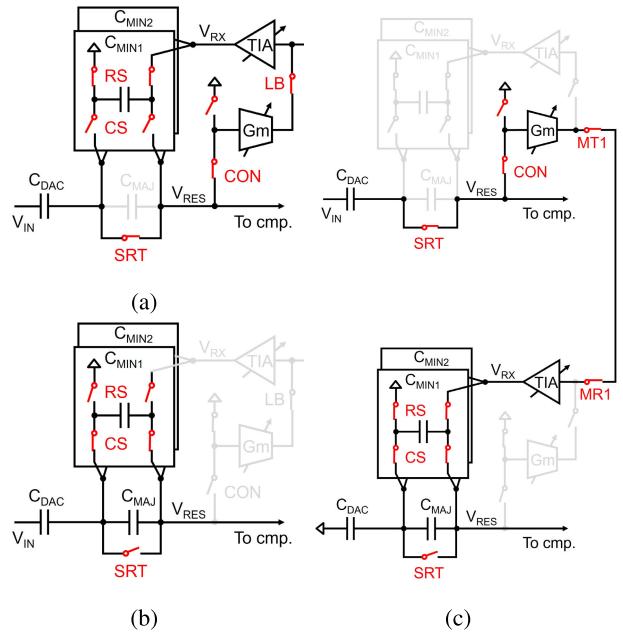


Fig. 10. Illustration of the EF operation in (a) residue sampling phase, (b) charge sharing phase. (c) The residue injection operation in pipe-SAR amplification phase.

(C_{MAJ}) and two minor capacitors (C_{MIN1}, C_{MIN2}). The two minor capacitors sample the TIA output (V_{RX}) through switch RS, and then share charge with C_{MAJ} through switch CS to perform signal transferring or IIR filtering. The signal on C_{MAJ} is injected into the SAR Core by being stacked between the CDAC and comparator. Programmed with proper timing, this capacitor system can support pipeline, noise-shaping, and other advanced architectures. Fig. 10(a) and (b) depict the error feedback (EF) operation in the 1st-order NS mode, serving as an illustrative example.

Fig. 11 (a) presents the corresponding signal model. Flicker noise generated by the G_M cell can degrade noise performance in NS modes, as illustrated by the D_{OUT} spectrum in Fig. 11 (c). To mitigate this issue, system chopping is employed by controlling both the input signal and the polarity of the residue feedback, as depicted in Fig. 11 (b). This is achieved by programming the FIN and FTX signals (shown in Fig. 7). It modifies the NTF from $1 - H_{EF}$ to $1 + H_{EF}$ and shifts the input signal to $F_s/2$, as illustrated in the $D_{OUT,F}$ spectrum in Fig. 11 (c). Finally, chopping the digital output restores a low-pass characteristic in $D_{OUT,CHOP}$. This process is equivalent to chopping at $F_s/2$, shifting the flicker noise and offset to out of band.

The achievable noise transfer function (NTF) for 1st-order NS is

$$1 - A \frac{C_{MIN1}}{C_{total}} z^{-1} \quad (1)$$

for 2nd order NS is

$$1 - A \frac{C_{MIN2}}{C_{total}} z^{-1} + A \frac{C_{MIN1}}{C_{total}} z^{-2} \quad (2)$$

where $C_{total} = C_{MAJ} + C_{MIN1} + C_{MIN2}$. By trimming the amplifier gain A, the optimal NTFs for 1st-order and 2nd-order noise-shaping can be achieved.

For pipe-SAR modes, the loop filter of the first stage is bypassed by a short switch (SRT), while the TIA output of

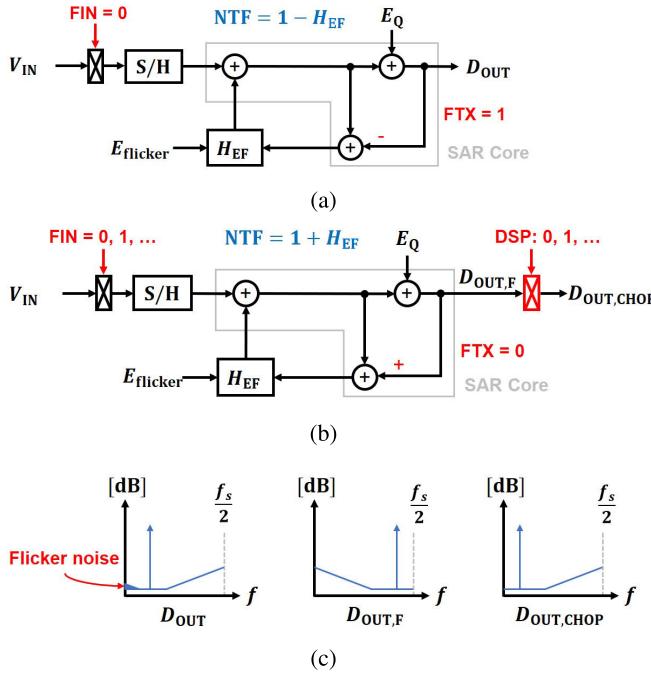


Fig. 11. Signal model of the 1st-order noise-shaping mode (a) without chopping, (b) with system chopping, and (c) the corresponding spectra.

the second stage can be directly sampled onto C_{MAJ} through RS and CS, as illustrated in Fig. 10(c).

E. Timing Matrix

The Timing Matrix is the foundation of PCA's programmability. It is essentially a crossbar switch array that maps the Frame Bus to the control signals. As illustrated in Fig. 12, the rows and columns represent control signals and frames, respectively, and the matrix size determines the available programming space.

In the prototype PCA, there are 24 control signals for each CB and the maximum frame period is 16, thus the programming space of each Timing Matrix is 384 bits. A global Frame Sequencer drives the Frame Bus at the main clock frequency (i.e., frame rate), and therefore drives all Timing Matrices to generate the programmed control signals. Each Timing Matrix can be disabled by freezing the column drivers when the corresponding CB is not in use.

Each element in the Timing Matrix consists of a 1-bit memory (DFF) and a line-NOR driver. The line-NOR gate is essentially a modified open-drain driver, it pulls down the row line when the corresponding frame bus and DFF are activated. To output a logic-high signal, the line-NOR gate has a PMOS branch for pull-up as well, but it is only activated when the current frame ($D[i,j]$) is 0 while the previous frame ($D[i, j-1]$) is 1. This design minimizes the logic flipping in the Timing Matrix and significantly saves power. The row lines are then buffered by a non-overlap (NOL) driver to generate the actual control signals. This ensures that there is no overlap between different frames of different control signals, while a multi-frame high level is uninterrupted, allowing some key operations, such as residue amplification, to be extended in time for better performance.

TABLE I
DESCRIPTION AND TYPICAL VALUES OF TIMING MATRIX

Name	Description	Typical Value
V_{DD}	Supply voltage	0.9 V
f_{frame}	Frame frequency	0.1 ~ 1.4 GHz
$Q_{clk,col}$	Charge to drive column line	45 fC
Q_{trans}	Charge to change output status	50 fC
N_{trans}	Average transitions per frame	3 ~ 4
I_{leak}	Leak current	20 μ A

The power consumption of the Timing Matrix can be estimated by

$$P_{TM} = V_{DD} ((Q_{clk,col} + Q_{trans}N_{trans}) f_{frame} + I_{leak}) \quad (3)$$

Table I gives the definitions and typical values of the terms in Eq. (3). For a configuration averaging 3 transitions per frame, the power consumption of a Timing Matrix is calculated to be approximately 200 μ W at a 1GHz frame rate, which matches the measurement results.

F. Output Bus

To efficiently transmit the output data from the CB arrays, each CB embeds an Output Buffer mounted on the Output Bus. As shown in Fig. 13, this buffer deserializes the data from the SAR Core, and wraps debugging information and the CB address (index) into the output data. In the prototype implementation, each 16-bit data package consists of 11 bits of conversion data, 3 bits of CB address, and 2 bits of debugging information. The debugging bits indicate whether the two SAR segments' conversions are completed within a clock cycle.

Upon receiving a *DISPATCH* signal from the Timing Matrix, it takes over the Output Bus and uploads the packaged output data. For simplicity, the output bus in the prototype chip is fully passive with no latch, allowing a minimum bus transferring delay and zero data latency. To enable data parsing and processing in various modes and implement different decimation filters, a reconfigurable backend digital signal processor (DSP), such as FPGAs or other programmable fabrics, is necessary. In this work, these post-processing tasks are performed off-chip using MATLAB for simplicity.

IV. MEASUREMENT RESULTS

The prototype PCA is fabricated in a 28nm CMOS process. Fig. 14 shows the die photograph. The total area of the six CBs is 0.1mm² (0.017mm² each CB), where the area overhead for the Timing Matrix and Frame Bus is about 20%. The G_M cell and TIA are powered by a 1.2V supply, while all other analog and digital circuits (including the programmable logic and the frame generator) operate at a 0.9V supply. The positive and negative reference voltages are set to 0.9V and 0V, respectively.

The prototype can be configured to support over 4 architectures and 20 operation modes, as previously illustrated in Fig. 6. CDAC mismatches, comparator offsets and inter-stage gain errors are off-chip foreground calibrated using an LMS-based algorithm. The sampling skew is calibrated by a correlation-based algorithm [45] in the background (off-chip), which adjusts a 4-bit on-chip clock delayer in each CB.

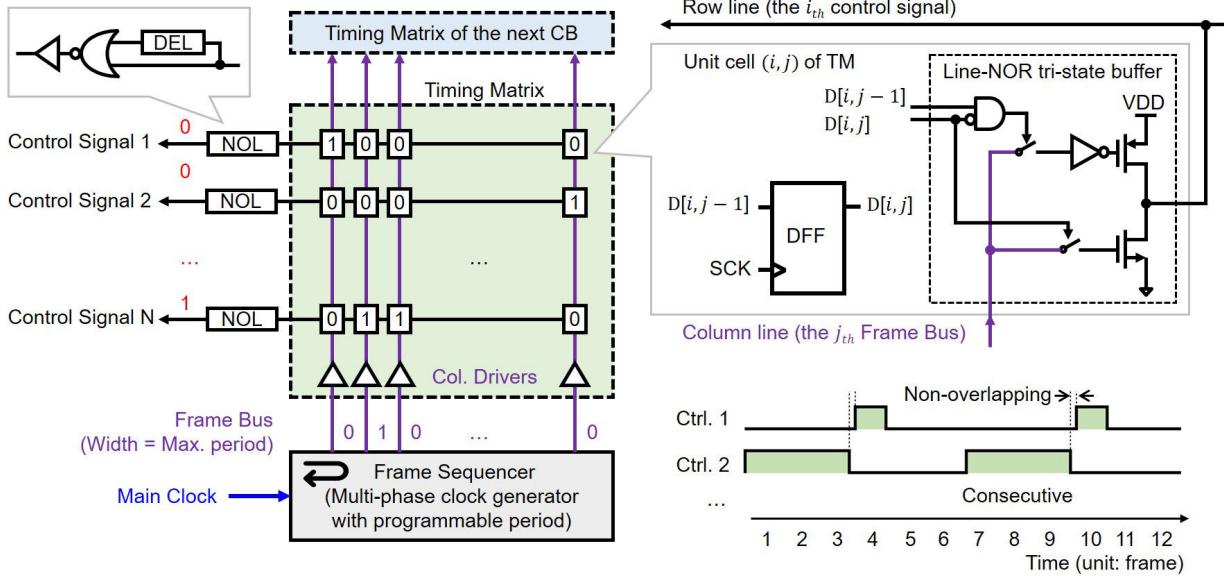


Fig. 12. Schematic of Timing Matrix and example output waveform.

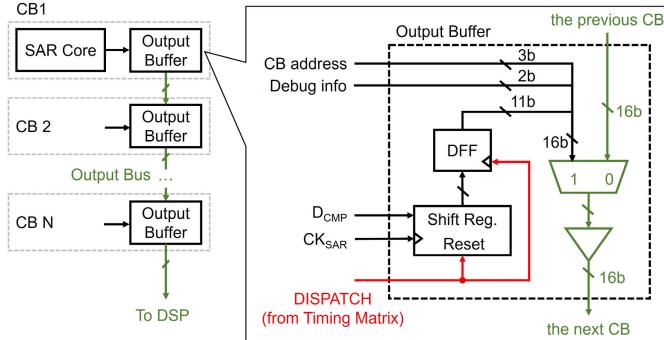


Fig. 13. Schematic of the Output Bus.

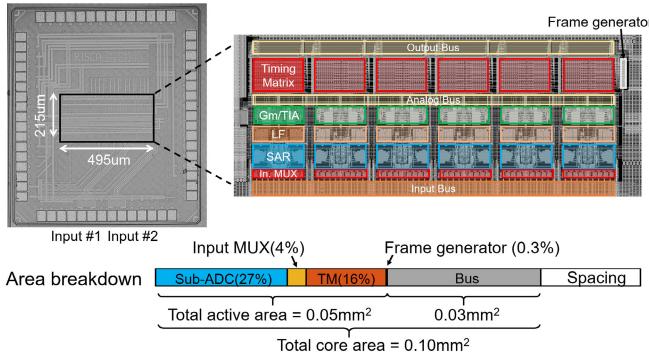


Fig. 14. Die photograph and area breakdown.

Fig. 15 shows the measured spectra and the corresponding timetable of some representative configurations (conf. A-N). The measured data are captured by an on-chip FIFO to ease output interface, thus the maximum FFT points are varied by frame configurations.

For Nyquist applications, an 8.7-ENoB plain-SAR ADC can be synthesized by taking a single CB (conf. A). A pipelined-SAR can be formed by taking an additional

low-resolution-SAR-configured CB as the first stage, by which the SNDR can be increased by 14dB (conf. B). Due to the speed limitation of residue transmission, the frame rate of this configuration is limited to 450MHz. By allocating more frames to the amplification phase, the frame rate can be increased to 1GHz to obtain a 250MHz sampling rate (conf. C). Additionally, configuring the first-stage CB as a full-resolution SAR can reduce the residue swing and relax the nonlinearity of the G_M cell, where the first-stage quantization noise leakage can be effectively suppressed (conf. D). To further improve accuracy, two CBs can be enabled simultaneously as the first stage, and their residue can be summed on the analog bus in the current domain (conf. E). The SNR can then be improved by 3dB without doubling the total power. The bus summing method is scalable, allowing for an additional 3dB gain in SNR by stacking four first stages (conf. F). Moreover, the two-phase settling option can be enabled to further enhance the SNR to 75.8dB, reaching a peak Schreier FOM of 176dB (conf. G).

Regarding pipe-SAR configurations, the PCA prototype can support up to six stages. However, the noise performance is dominated by the sampling kT/C noise and amplifier noise, adding stages beyond two for quantization noise reduction is unnecessary and yields negligible SNR improvements. Consequently, only two-stage pipe-SARs are reported above.

For higher bandwidth applications, time-interleaving can be applied on any Nyquist configurations mentioned above (conf. H-J). It is worth noting that the interleaving number can be extended by increasing the frame rate and duplicating the timetable, such that the interleaving number can be doubled (conf. I). In applications requiring higher performance with high-frequency inputs, additional bits should be added to the trimmers, potentially achieving an SFDR greater than 70dB. Additionally, a larger main clock driver can be employed to reduce jitter-induced noise, albeit with increased clock power consumption.

For oversampling and high-resolution applications, noise-shaping SAR architectures can be synthesized from a single

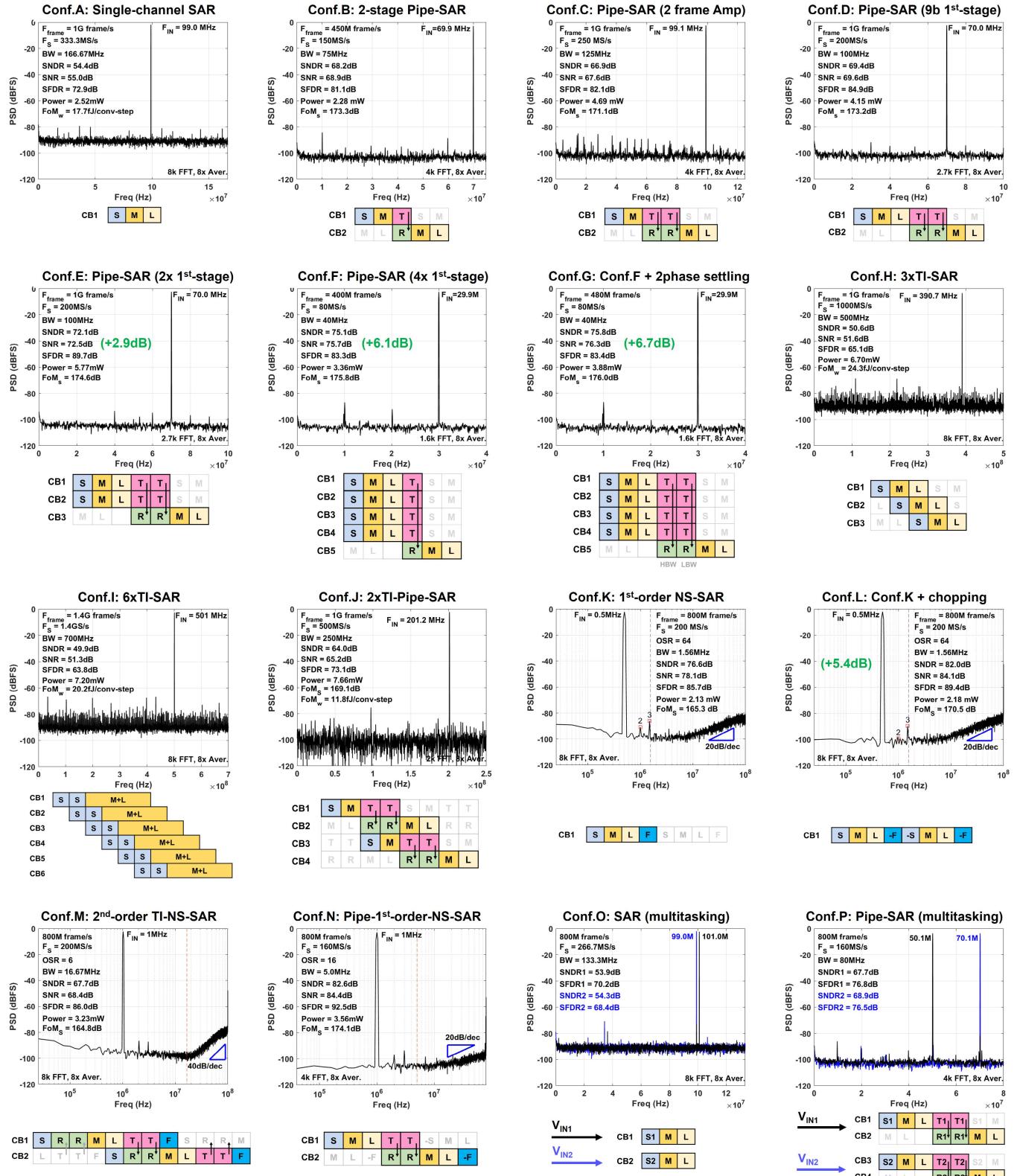


Fig. 15. Measured ADC output spectra for different configurations.

CB (conf. K). System chopping, as described in Section III-D, is implemented by inverting the input sampler and the output of the G_M , corresponding to $-S$ and $-F$ in the timing table of conf. L. This configuration effectively suppresses flicker noise originating from the G_M cell, resulting in an improvement

of the SNR by 5.4dB. Second-order noise-shaping can be also achieved by synthesizing a 2-way-time-interleaved noise-shaping SAR architecture [43] from 2 CBs (conf. M). A hybrid architecture doing noise shaping in the second stage of a pipe-SAR can be implemented as well (conf. N).

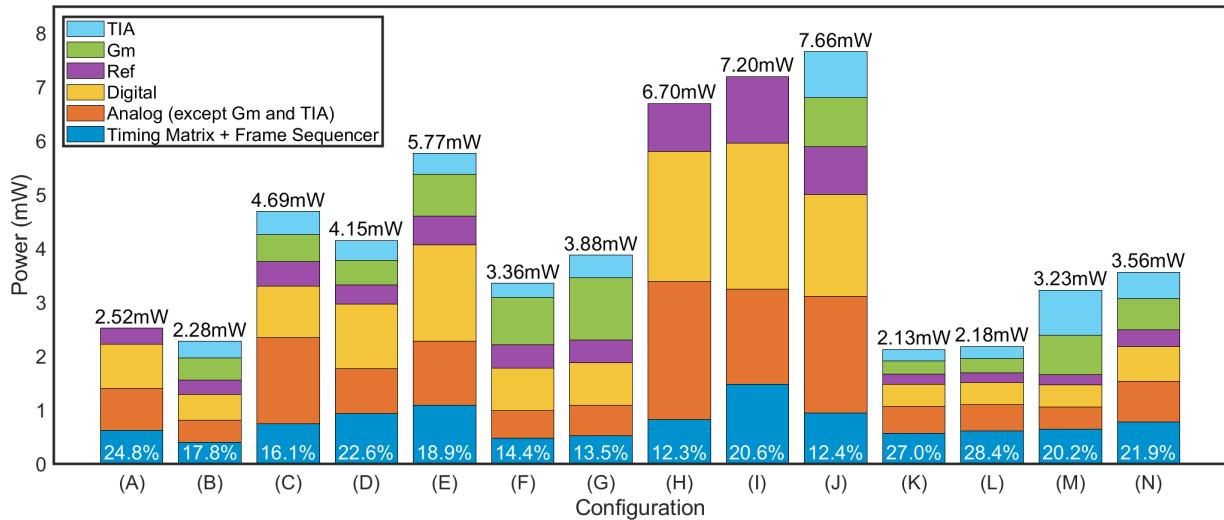


Fig. 16. Measured power consumption of configurations in Fig. 15.

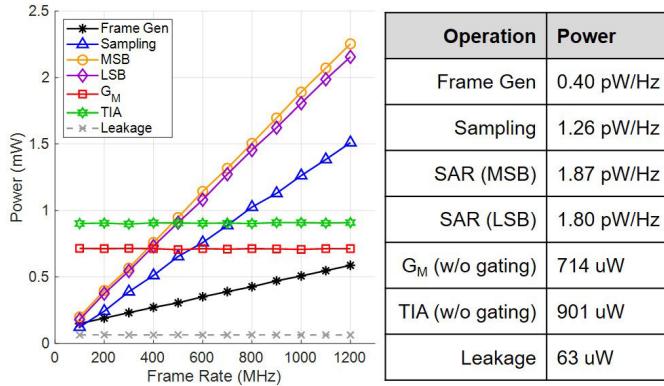


Fig. 17. Measured power for different operations across clock frequencies.

Fig. 16 presents the power breakdown of the various configurations above, revealing that the reconfigurable portion (Timing Matrix and Frame Generator) consumes only 12% to 28% of the total power. The power consumption of diverse configurations depends on the specific operations being configured. The total power of a configuration can be estimated by

$$P_{\text{total}} = \sum_{i=1}^N P_{\text{CB},i} + P_{\text{framegen}} + P_{\text{leak}} \quad (4)$$

where the first summation accounts for the power of all CBs, the second term represents the power of the shared frame generator, and P_{leak} denotes the leakage power due to the extensive use of ultra-low-V_{th} MOSFETs. The power consumption of each CB can be estimated by

$$P_{\text{CB}} = (E_{\text{sam}} N_{\text{sam}} + E_{\text{MSB}} N_{\text{MSB}} + E_{\text{LSB}} N_{\text{LSB}}) F_s + P_{\text{GM}} \eta_{\text{GM}} + P_{\text{TIA}} \eta_{\text{TIA}} + P_{\text{TM}} \quad (5)$$

Here, E denotes the unit energy of dynamic operations, N denotes the number of frames used in each sampling period, F_s is the sampling frequency, P_{GM} and P_{TIA} is the static power, η denotes the duty cycle of power gating, and P_{TM} can be estimated by Eq.(3). Fig. 17 presents the power consumption of different operations against frame frequency.

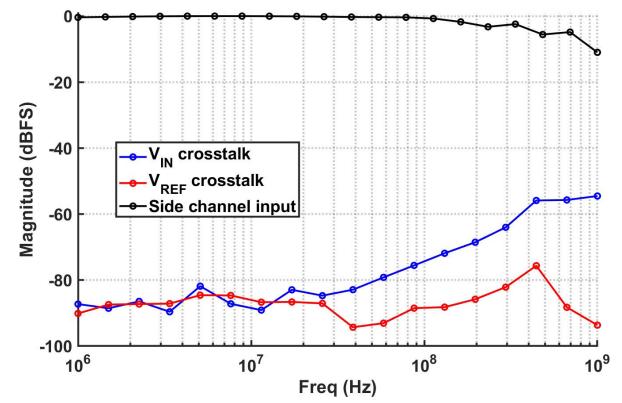


Fig. 18. Measured crosstalk versus frequency.

Techniques such as adjusting frame allocation, inserting empty frames, and clock scaling help optimize energy usage, while substituting regular-V_{th} devices reduces leakage.

To demonstrate the ability to handle concurrent A/D conversion tasks (i.e., multitasking), the prototype PCA is then configured as two parallel-running SAR ADCs (conf. O). The two paths of input signals are routed to the two ADCs by configuring the input multiplexer. Two concurrent pipe-SAR ADC is also realizable with more CBs for a higher performance (conf. P). Fig. 18 presents the relationships between frequency and crosstalk magnitude. By overlapping the sampling phase or the conversion phase of the two CBs, the crosstalk via input bus or via reference network can be measured respectively. A maximum crosstalk of -70dB is measured up to 100MHz, indicating that the crosstalk between concurrent channels is not a severe problem for most applications.

Fig. 19 and Fig. 20 show the measured performance versus input magnitude and frequency of four representative configurations. The measured dynamic range (DR) covers from 56dB to 84dB by these four configurations, where the trade-off between accuracy and bandwidth is evident. The SNDR degradation near Nyquist input frequency is due to the clock jitter and insufficient sampling bandwidth.

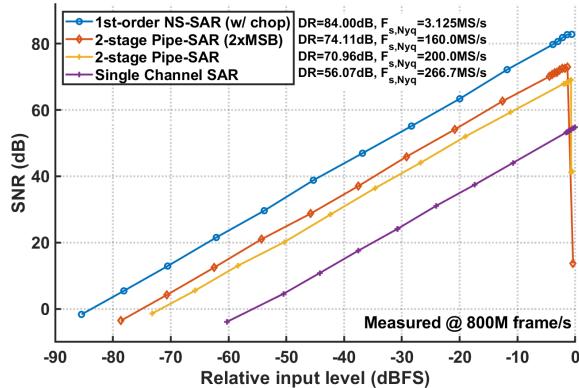


Fig. 19. Measured SNR versus input amplitude.

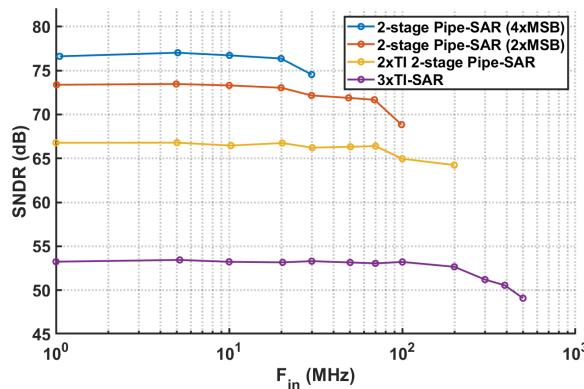


Fig. 20. Measured SNDR versus input frequency.

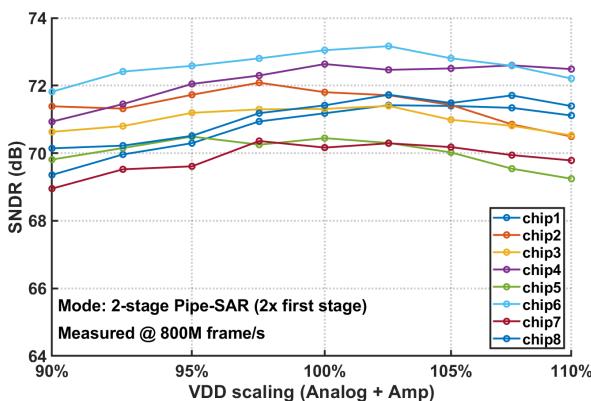


Fig. 21. Measured SNDR versus analog supply voltage, on 8 randomly selected devices.

The performance variation between devices and under power supply fluctuations is evaluated on conf. E. The SNDR of 8 tested devices vary within ± 1 dB under a $\pm 10\%$ supply voltage variation, and the variation across devices is within 3 dB, as shown in Fig. 21.

To have a comprehensive evaluation of the prototype, Fig. 22 plots the measured performances and their corresponding CB usage under 18 different configurations, where the trade-off between hardware resource and performance is evident. The 10dB/decade extension line indicates the performance range that can be covered by

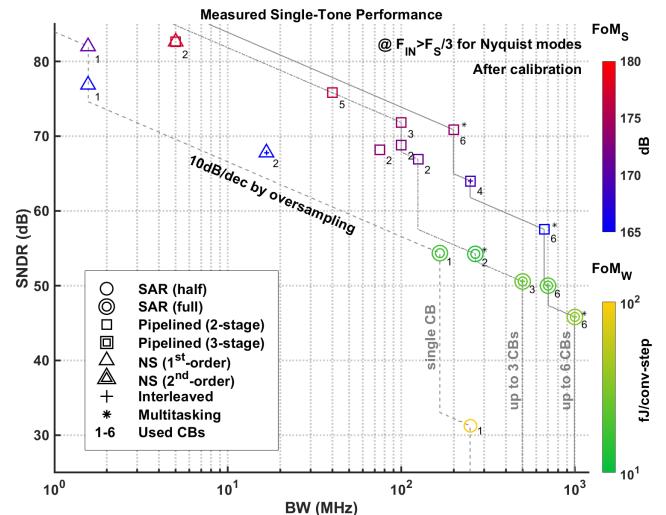


Fig. 22. Measured single-tone performances of 18 selected modes, and the corresponding CB resources usage.

TABLE II
COMPARISON WITH SOTA MULTI-MODE AND RECONFIGURABLE ADCS

Multi-mode ADC work	This work	ISSCC'19 Wang [9]	TCASII'22 Be [22]	TCASII'20 Erol [26]	ASSCC'13 Yousry [30]
Architecture	RISCA (PCA)	CT-DSM	TI-SAR	Zoom	Flash/Two-step
Programming Level	Architecture restructuring	Circuit tuning	Circuit tuning	Circuit tuning	Architecture switching
Process (nm)	28	28	28	130	65
Area (mm ²)	0.1 (6 CBs)	0.06	0.48	0.3	0.15
Concurrent task	2	1	1	1	1
BW span (MHz)	<1 ~ 1000*	20 ~ 160	150 ~ 450	0.1 ~ 10	750~2000
SNDR span (dB)	30 ~ 82	65 ~ 77	52 ~ 56	70 ~ 87	20 ~ 39
Peak FoMs _{S,SNDR} (dB)	176 @40M-BW	171 @10M-BW	156 @150M-BW	166 @1.92M-BW	141 @750M-BW

*Aggregate BW of two-task mode

trivial oversampling. The total available bandwidth of the prototype covers from DC to 1GHz, and the achievable SNDR covers from 30dB to 82dB, which demonstrates the high flexibility and wide performance range of the proposed PCA architecture. A peak Schreier figure of merit (FoMs) of 176dB is achieved around 40MHz bandwidth and 75.8dB SNDR by an enhanced pipe-SAR configuration, which is also competitive to the SoTA single-mode ADCs.

Fig. 2 provides a comparison of the performance and energy efficiency of our prototype in relation to notable published multi-mode ADCs and all single-mode ADCs from the ADC survey [31], showing that this work achieves the widest performance coverage among existing multi-mode ADCs. Table II compares the proposed PCA architecture with state-of-the-art (SoTA) multi-mode ADCs. To the best of our knowledge, this proposed PCA architecture represents the first multi-mode ADC capable of concurrently executing tasks while demonstrating the widest performance range.

Table III illustrates a case study, comparing the proposed PCA architecture with SoTA single-mode ADCs [35], [45], [48], [49], [50] orientating five typical wireless scenarios, including GSM/CDMA, LTE, NR FR1, NR FR2/Wi-Fi 6/7, and DPD. At medium speeds, the energy efficiency of PCA

TABLE III
COMPARISON WITH SoTA SINGLE-MODE ADCS WITH SIMILAR SPEC

Target	GSM/CDMA 2M-BW 80dB		LTE 40M-BW 75dB		NR FR1 100M-BW 70dB		NR FR2 / WiFi-7 200M-BW 60dB		NR FR2 / DPD 500M-BW 50dB	
	This work 28nm	VLSI'23 22nm [48]	This work	ISSCC'20 28nm [35]	This work	ISSCC'24 22nm [49]	This work	ISSCC'24 8nm [50]	This work	JSSC'24 28nm [45]
Arch.	NS-SAR OSR 64	DT-DSM OSR 24	Pipe-SAR	TI-Pipe-NS-SAR OSR 7.5	Pipe-SAR	Pipe-SAR	TI-Pipe-SAR	Pipe-SAR	TI-SAR	TI-SAR
Fs (MHz)	200	96	80	600	200	200	500	400	1000	1000
BW (MHz)	1.56	2	40	40	100	100	250	200	500	500
SNDR (dB)	82.0	79.9	75.8	75.2	72.1	70.7	64.0	62.8	50.6	59.3
Power (mW)	2.18*	1.04	3.88*	2.56	5.77*	2	7.66*	2.08	6.70*	3.7
FoMs _{S,SNDR} (dB)	170.5	172.7	176.0	177.1	174.6	177.7	169.1	172.6	159.3	170.6
Area (mm ²)	0.017 (1 CB**)	0.025	0.085 (5 CBs)	0.016	0.051 (3 CBs)	0.019	0.068 (4 CBs)	0.017	0.051 (3 CBs)	0.014

* Including all programmable logics (Timing Matrices) and the global sequencer

** Core area per CB = 0.017mm²

	This work	SoTA single mode ADCs covering similar specifications
Active area	0.05mm ²	(0.025+0.016+0.019+0.017+0.014)×2 ¹ =0.18mm ²
Core area	0.1mm ²	Much larger than 0.18mm ²

† Factor 2 for handling I/Q channels in these wireless standards

is comparable to SoTA single-mode ADCs, noting that this includes the power of all programmable logics and the global sequencer. Compared with using single-mode ADCs to cover the standards, the PCA solution saves 70% of the total active area.

V. CONCLUSION

To address the limitations in reconfiguration range, efficiency and concurrency support in multi-mode and reconfigurable ADCs, this work proposes the PCA architecture to offer remarkable flexibility, broad performance coverage, and mode concurrency through resource pooling in ADC arrays. The architecture is demonstrated by a prototype implemented in 28nm CMOS, configurable to over 16 modes, with an SNDR range of 30dB to 82dB and bandwidth from sub-MHz to 1000MHz. The prototype achieves a peak FoMs of 176dB at 40MHz-BW, maintaining over 165dB across most configurations, and occupies only 0.1mm² of silicon area. This work marks an initial step in a broader effort to aggregate AFE resources in multi-standard receivers by developing efficient multi-mode ADCs.

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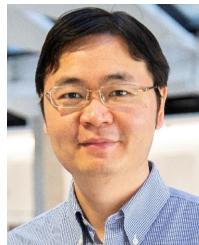
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