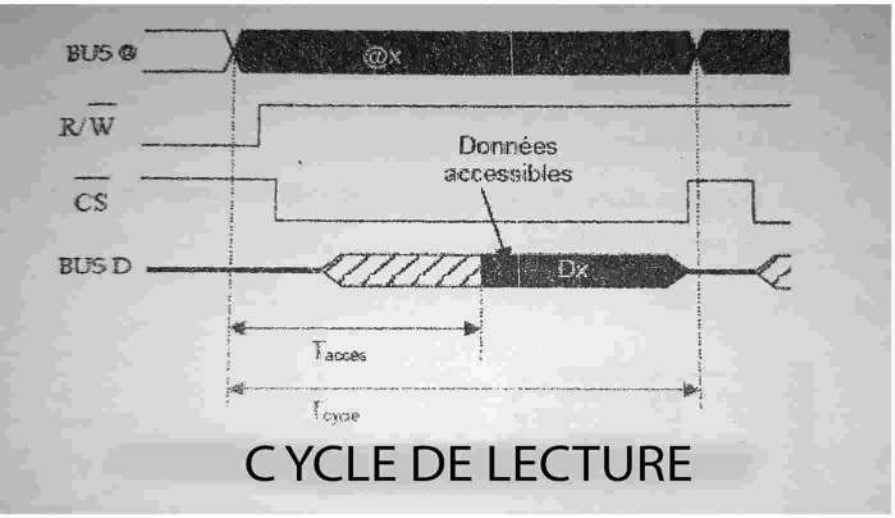
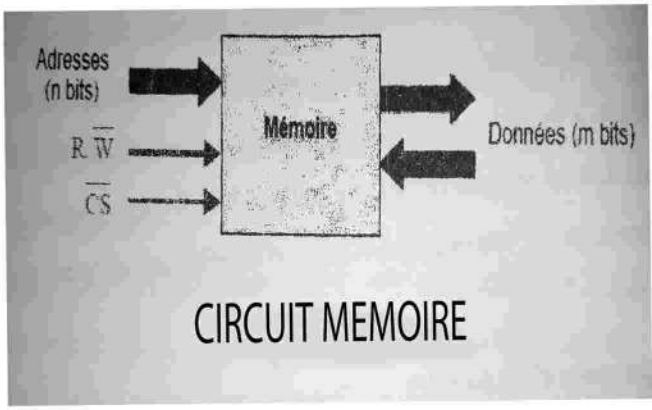
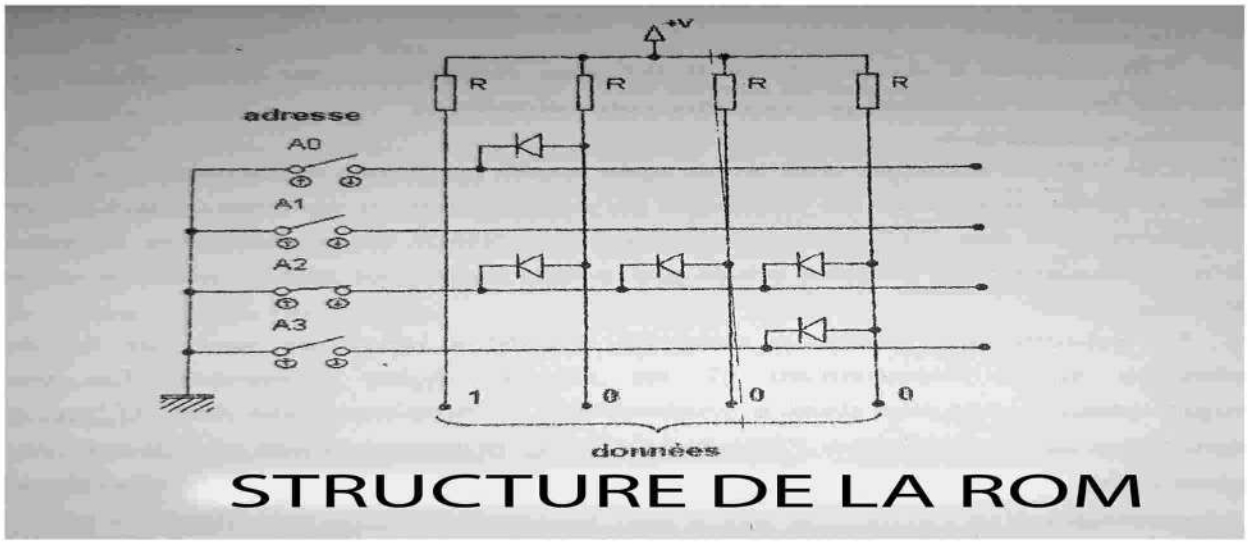


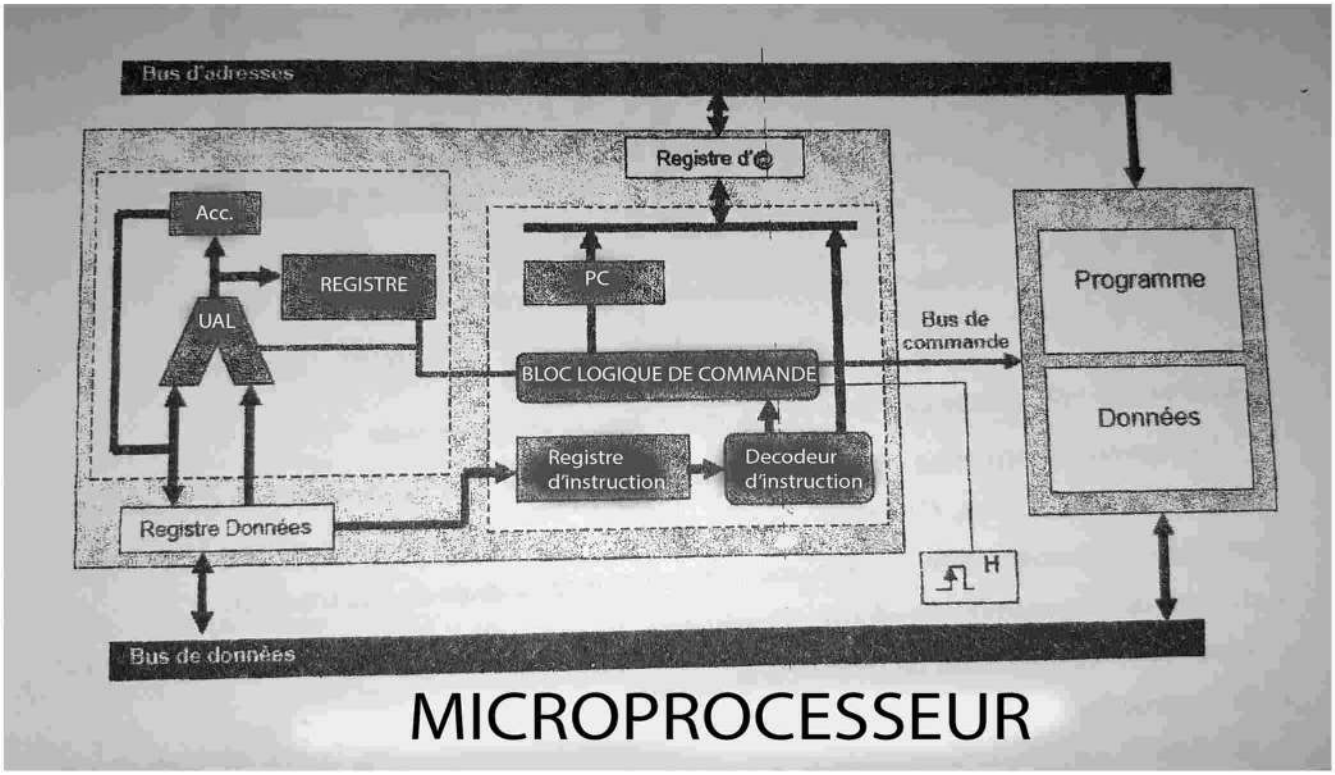
C YCLE DE LECTURE



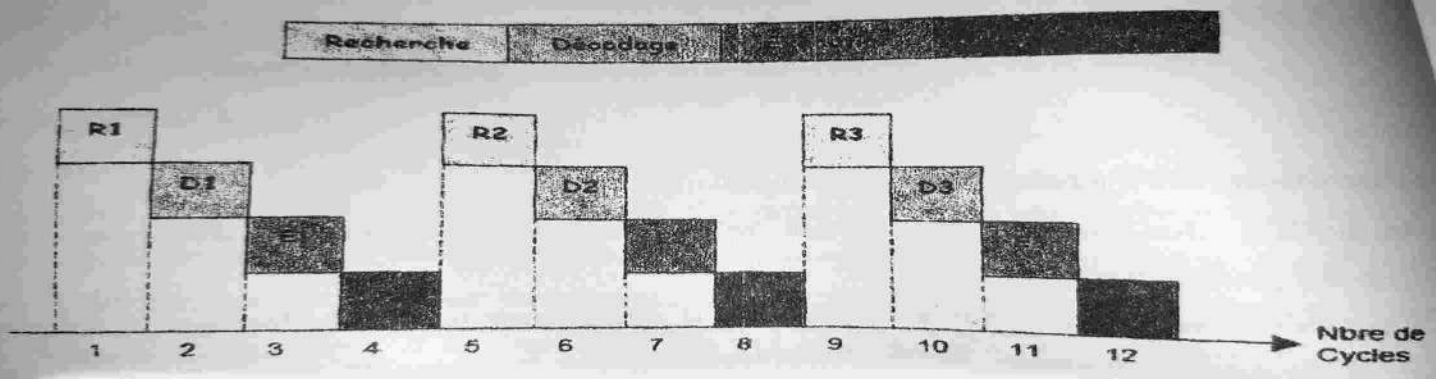
CIRCUIT MEMOIRE



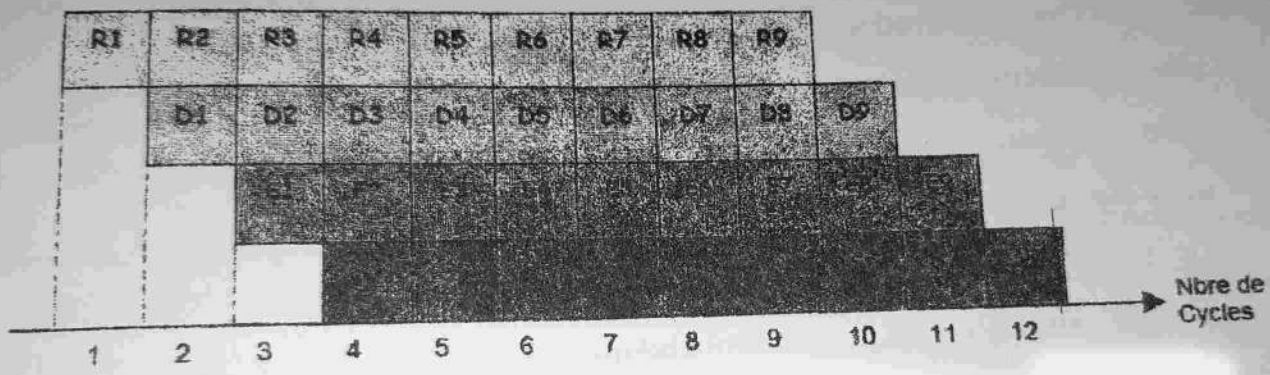
STRUCTURE DE LA ROM



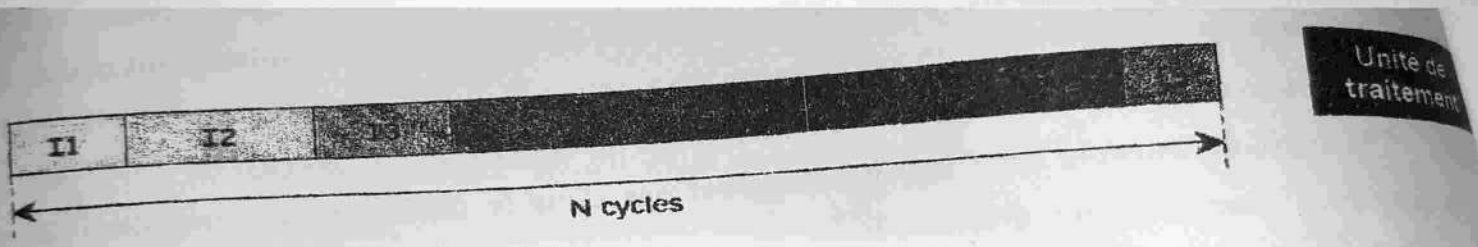
MICROPROCESSEUR



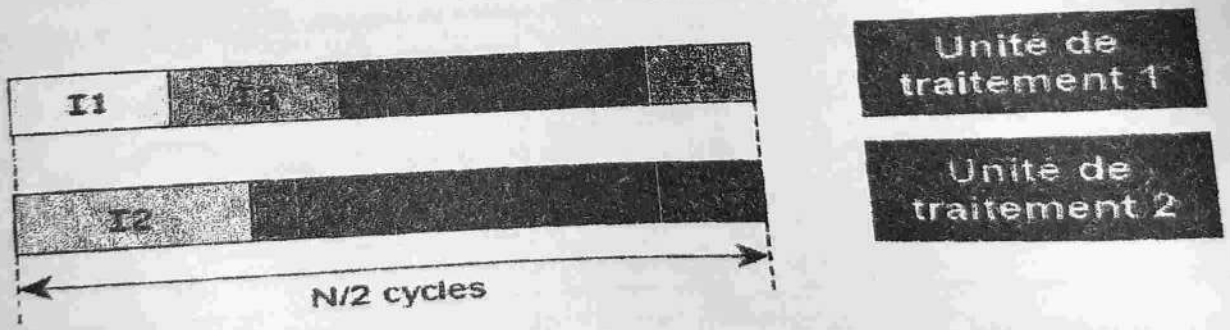
systeme d'execution d'instruction modèle classique



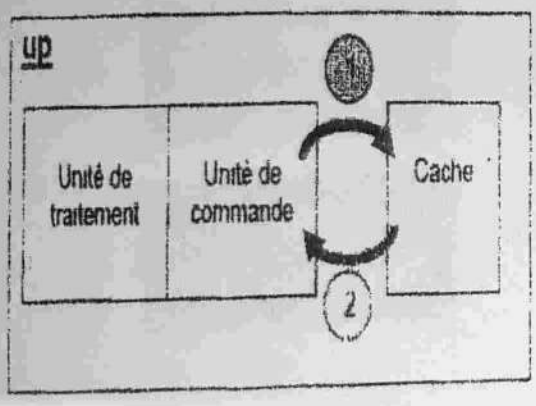
système d'execution d'instruction modèles pipeline



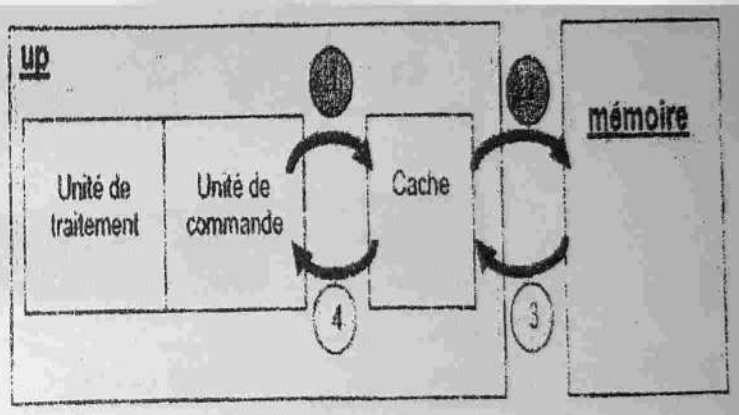
Architecture scalaire



Architecture superscalaire



Succès de cache



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