CH634 Chip Schematic Diagram and PCB Design Considerations

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The CH634 is a 4-port USB SuperSpeed hub controller chip compliant with the USB 3.2 Gen 1 protocol. It integrates 4 USB hubs and USB Power Delivery functionality on a single chip. This document focuses on the schematic and PCB design of the CH634 chip, summarizing some key considerations.
It primarily includes the following two sections:

I. CH634 Design Considerations

1. The 1.2V power supply used by the CH634 chip draws approximately 500mA. Some CH634s have a built-in DC-DC converter that steps down the VDD5 pin voltage to 1.2V. This DC-DC converter requires an external inductor, input capacitor, and output capacitor, placed as close to the chip as possible. A 2.2uH inductor is recommended, capable of handling no less than 1.5A. Inductors with low DC resistance are preferred. A 10uF capacitor is recommended for the DC-DC input. For the DC-DC output, a 0.1uF-1uF capacitor in parallel with a 10uF-22uF capacitor is recommended (place the larger capacitor immediately after the inductor, the smaller capacitor at the VFB pin), or at least two 4.7uF capacitors in parallel. MLCC capacitors with low ESR are preferred. The dedicated GND_DCDC circuit for the DC-DC converter can be noisy, so keep the PCB traces short and thick to avoid connecting to common signal traces.
2. Place a 0.1uF high-frequency capacitor on each of the 1.2V power pins as close to the chip as possible. If possible, connect multiple 1uF high-frequency capacitors in parallel to the P*VDD12 pins to improve power ripple and EMI. Alternatively, filter the 1.2V DC-DC output through an inductor before connecting it to the P*VDD12 pins.
3. The 3.3V power supply used by the CH634 chip draws approximately 100mA. Some CH634s have a built-in LDO that drops the VDD5 pin voltage to 3.3V. A 1uF to 10uF capacitor is recommended for the LDO's 3.3V output pin. The AVDD33 main power pin should be connected to ground with a capacitor close to the chip. A 0.1uF capacitor in parallel with a 4.7uF to 10uF capacitor is recommended. Use 0.1uF or 1uF capacitors for other 3.3V power pins (such as VDDIO). This means the 3.3V pin should have a 10uF capacitor and multiple 0.1uF or 1uF capacitors. If conditions permit, connect multiple high-frequency capacitors in parallel to improve ripple and EMI.
4. If there are two VDD5 pins, the VDD5 closest to VSW is the DC-DC power input, and the other VDD5 is the LDO power input. A 1μF or larger capacitor is recommended for the LDO power input VDD5. This can be combined with the DC-DC input capacitor to make a 0.1μF to 1μF capacitor, with a 10μF capacitor in parallel.
5. The CH634 chip operates at high current. PCB traces through which current flows should have at least two vias to withstand the high current. The corresponding ground traces should be copper-clad and have more vias. Especially for the 1.2V power supply, refer to the datasheet for voltage values (typically 1.23V). PCB traces should be as short and thick as possible.
6. The CH634 chip baseplate PCB design must facilitate heat dissipation while also handling high current. The baseplate should have at least nine large vias, and 25 is recommended. This is especially true for small packages like the CH634F.
7. Place the crystal and capacitors close to the chip; no external resistors are required. Choose a SMD crystal oscillator. The crystal frequency must be 24MHz, and the frequency deviation is recommended to be no more than 50ppm. For oscillator capacitance, refer to the crystal manual for specifications.
8. The PCB design for USB signal lines must follow the principles of high-speed differential signal lines. Calculate the characteristic impedance, consider trace width and spacing, and ensure impedance matching and compliance with USB specifications. It is recommended to avoid vias on signal lines and maintain clear space on both sides or use copper grounding with a high number of vias.
9. Depending on the application environment, low-voltage, high-frequency ESD devices can be added to

USB signals. Generally, overcurrent protection devices must be added to the VBUS power supply or each downstream port. A fuse resistor solution is simple, but the hub and USB host cannot sense overcurrent conditions. Furthermore, fuse resistors typically have an internal resistance of several hundred milliohms, resulting in a significant voltage drop when high current flows through them, causing the actual VBUS output voltage to be lower. It is recommended to use a USB current-limiting power switch chip. The preferred solution is dual independent mode, with independent switching and overcurrent protection for each downstream port. For simple applications, the GANG integrated mode can be used, sharing a single USB current-limiting power switch chip.

10. It is recommended to remove the peripheral components corresponding to each NC pin of the chip.

II. PCB Layout Examples

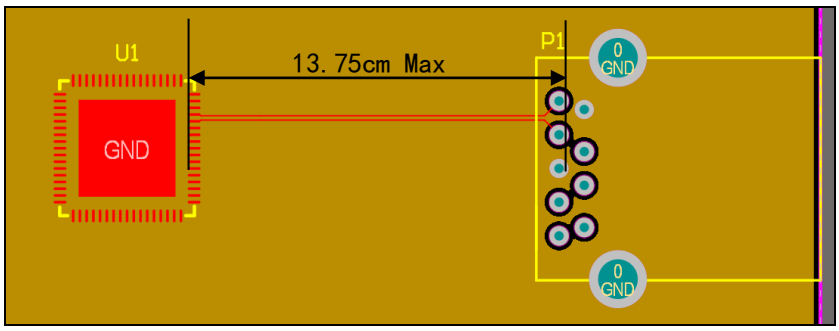
1. USB 3.0 Differential Signal Length Limits

USB 3.0 signal transmission rates reach 5Gbps and above. Excessively long traces can cause signal attenuation and reflection, affecting signal integrity and ultimately communication quality. Based on a -6.5dB loss calculation, the differential loss per inch of FR4 board is -0.8dB to -1.2dB. Theoretically, the maximum allowable trace length is 16.5cm under typical conditions, and 13.75cm under less favorable conditions. Therefore, it is best not to exceed 13.75cm for onboard PCB differential traces. Consult the PCB manufacturer for specific board loss parameters.

If onboard PCB traces are too long, pay attention to signal integrity. If possible, test the USB 3.0 signal eye diagram. When designing the PCB, impedance matching should be performed according to the USB specification.

In addition, the USB 3.0 protocol stipulates that the maximum total link loss is -20dB, -6.5dB on the host and device PCB ends respectively, and -7dB on the cable (C to C cable). Therefore, the recommended USB 3.0 cable length should not exceed 2m. The specific length depends on the cable quality. It is recommended to purchase USB-IF certified cables.

Schematic diagram of the longest differential line on the onboard PCB



2. AC coupling capacitors for USB3.0 signal TXA/TXB pins

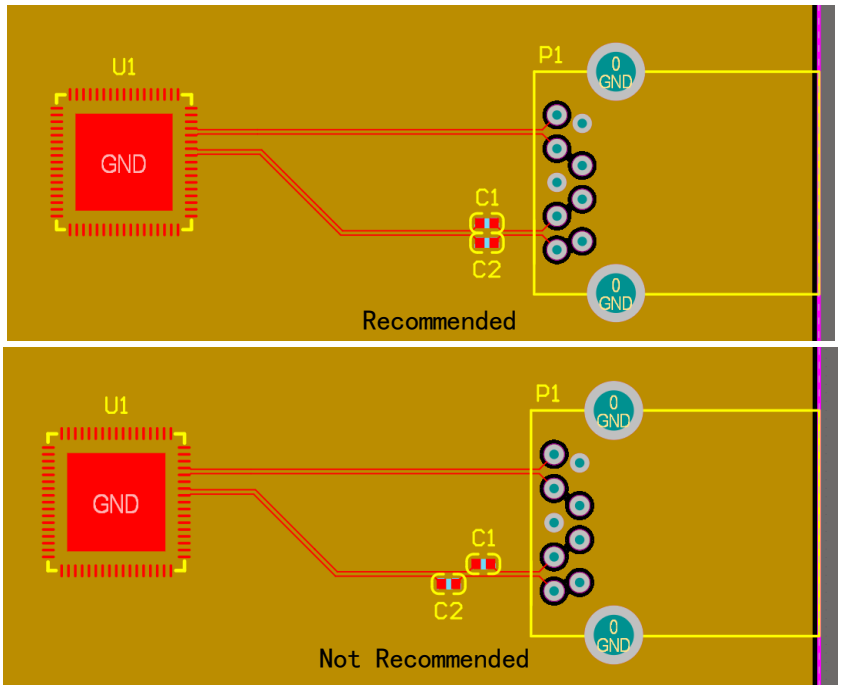
(1) The USB3.0 differential transmit signal line TXA/TXB pins (Px_SS_TXA, Px_SS_TXB) require an AC coupling capacitor;

(2) The USB3.0 differential receive signal line RXA/RXB pins (Px_SS_RXA, Px_SS_RXB) do not require an AC coupling capacitor;

(3) The AC coupling capacitor value is 0.1uF. It is recommended to place it near the connector and symmetrically;

(4) The smaller the package of the AC coupling capacitor, the better the effect. 0402 or 0201 packages are recommended.。

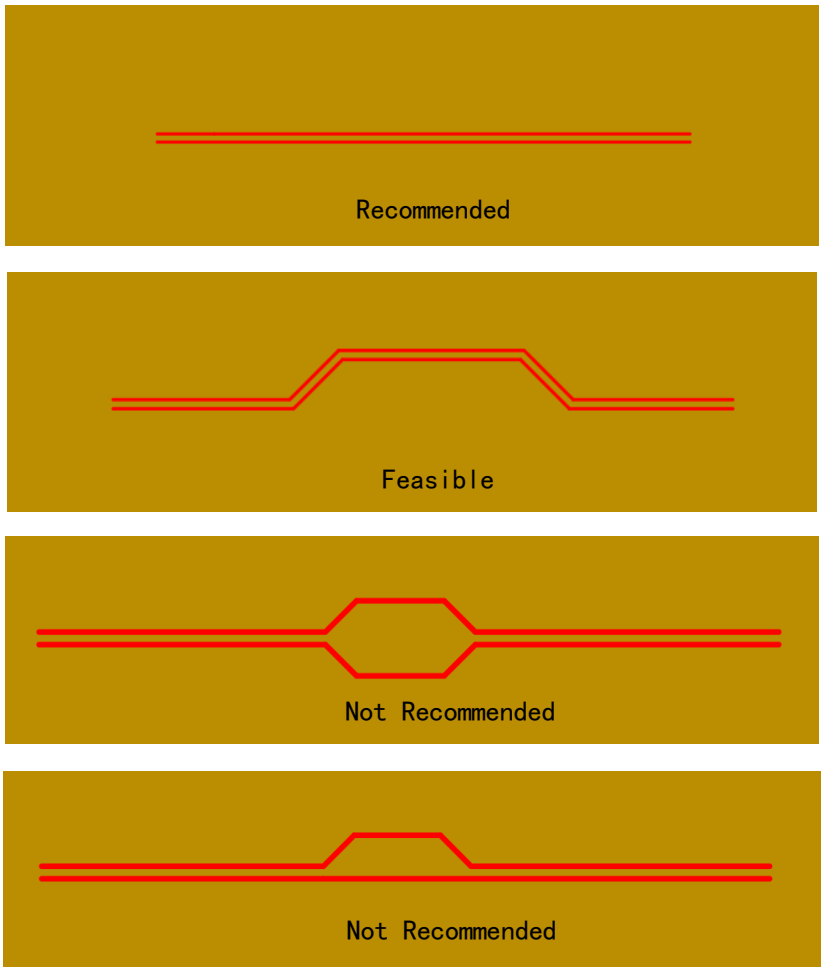
Schematic diagram of coupling capacitor placement



3. USB 3.0 differential signal line routing precautions

(1) USB 3.0 signals use differential routing. Keep the spacing between differential pairs consistent to avoid sudden narrowing or widening, which may cause impedance mismatch.

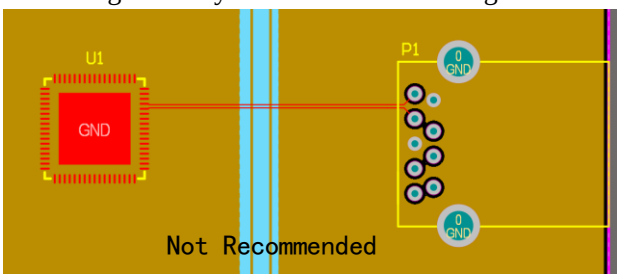
Differential signal routing diagram



(2) USB3.0 differential pair signal lines require a complete reference plane. The reference plane should

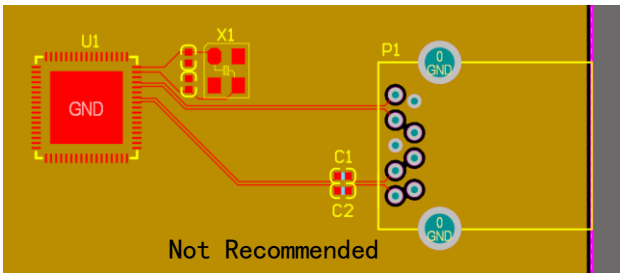
be continuous under the differential pair traces and should not be split or slotted to avoid interruption of the signal return path and changes in the characteristic impedance.

Schematic diagram of the ground layer under the USB3.0 signal line being disassembled



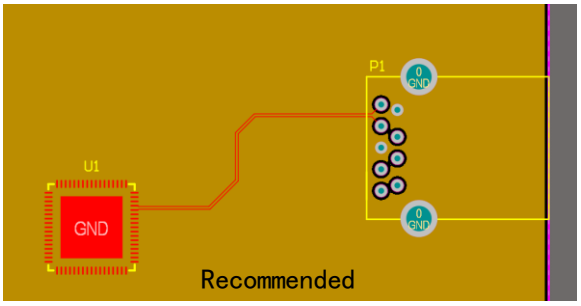
(3) USB 3.0 high-speed signals are easily interfered with by other signals and therefore need to be isolated from other signals. This can be achieved by increasing the distance or adding a ground line (ground plane) as an isolation barrier. For example 1: The distance between the USB 3.0 differential pair and other signals (such as crystal oscillators, clock signals, power lines, etc.) should be at least 20 mils; For example 2: The USB 3.0 differential pair should avoid being routed parallel to other high-speed signals (such as HDMI, PCIe, etc.) to reduce crosstalk;

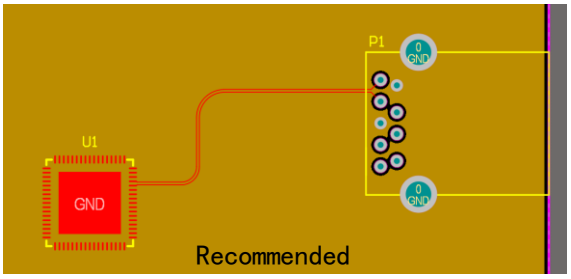
USB3.0 signal line is too close to the crystal oscillator diagram

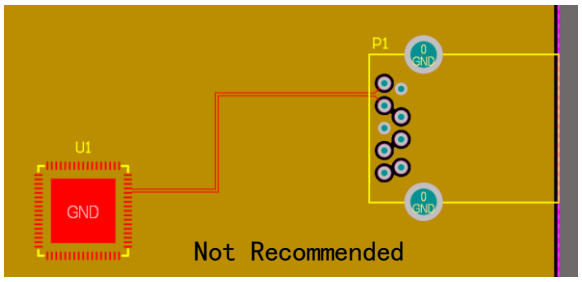


(4) USB3.0 differential signal lines can be routed at 45 degrees or in a circular arc, but not at 90 degrees.

High-speed differential signal line routing diagram

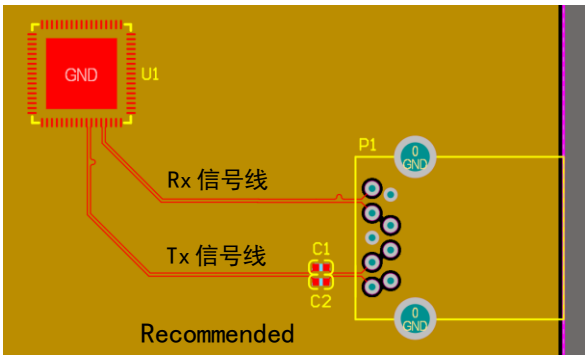






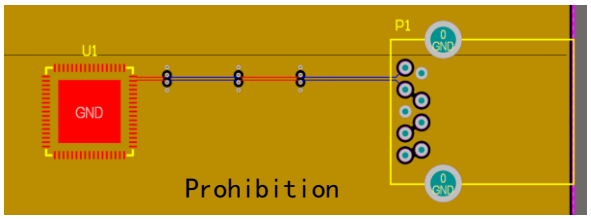
(5) The lengths of the two traces of the USB differential pair should be as equal as possible. The length difference of the USB 3.0 signal pair is recommended to be controlled within ±5 mil (0.127 mm); the length difference of the USB 2.0 signal pair is recommended to be controlled within ±50 mil (1.25 mm). When making the differential pair equal in length, it is recommended to align the USB 2.0 signal line and the USB 3.0 signal Rx signal line near the USB interface socket, and align the USB 3.0 signal Tx signal line near the chip.

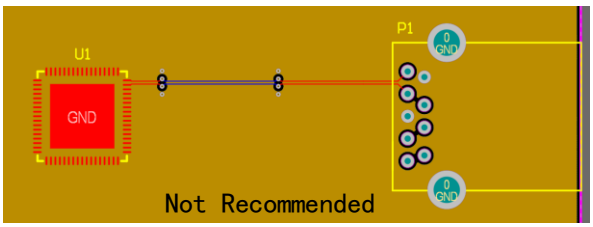
Schematic diagram of the position of differential signal equal length processing

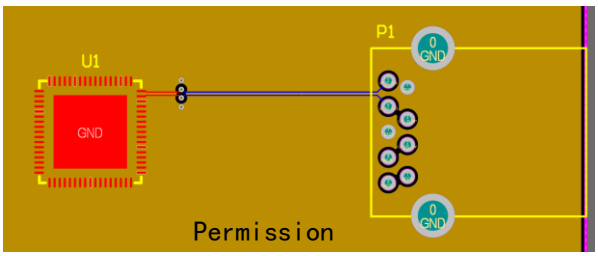


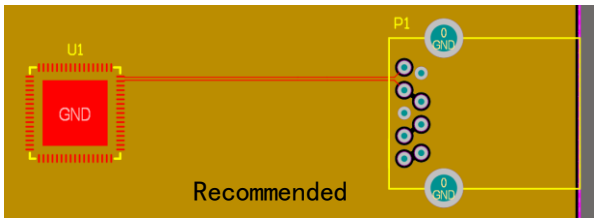
(6) The use of vias for USB3.0 differential signal lines should be minimized. The number of vias for each pair of differential lines should not exceed 2, and the vias need to be punched symmetrically, and the impedance of the vias should be matched with the impedance of the traces.

Recommended to reduce vias schematic



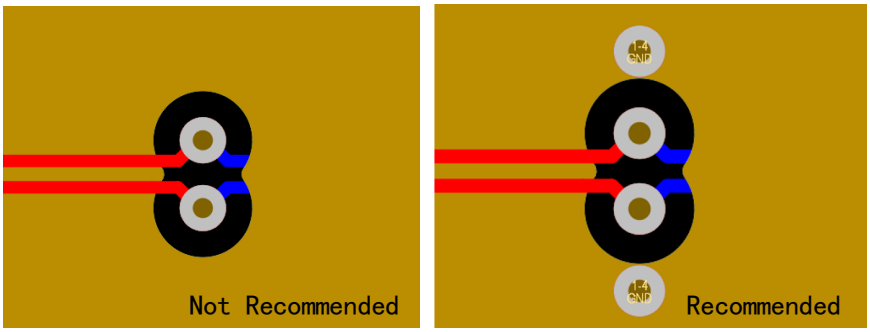






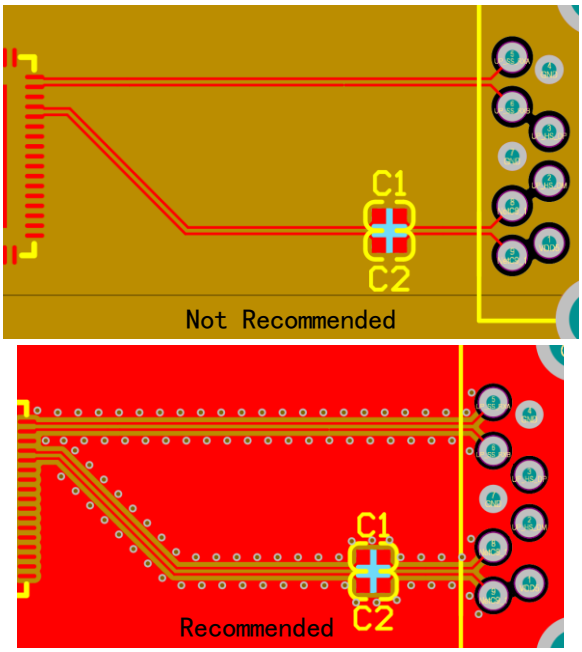
(7) When the USB3.0 differential signal line pair is processed through the via, a pair of return ground vias needs to be added near the via.

Schematic diagram of adding return ground vias



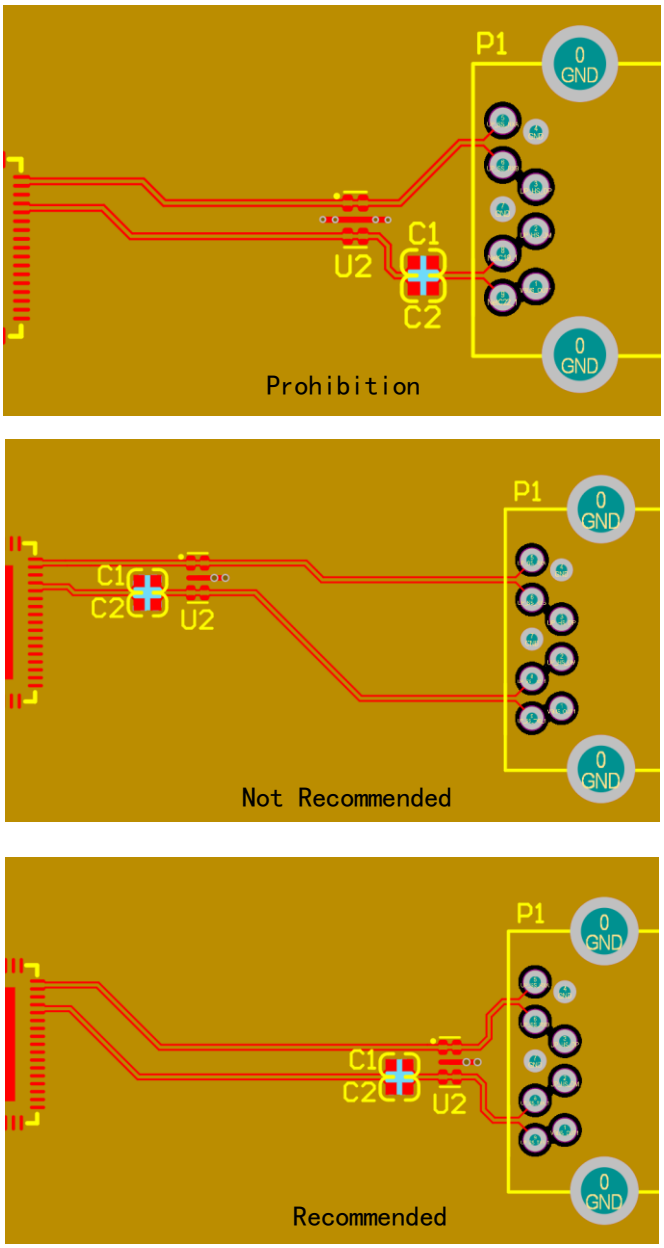
(8) When routing the USB3.0 differential pair, it is recommended to perform ground wrapping and drill a return ground via at intervals to reduce the interference of peripheral signals on the USB3.0 differential signal.

Schematic diagram of signal line grounding treatment



(9) If an ESD device is added to the USB3.0 differential signal line, the ESD device should be placed as close to the USB interface as possible, and the differential pair should first pass through the ESD device and then be connected to the chip end. The ESD device cannot be connected to the differential line in parallel.

Schematic diagram of ESD device placement



(10) The transmit signal lines TXA and TXB (Px_SS_TXA and Px_SS_TXB) of the USB3.0 differential signal line can be swapped, and the receive signal lines RXA and RXB (Px_SS_RXA and Px_SS_RXB) can be swapped, and the chip can automatically identify the crossover.

4. Recommended PCB Layer Count

The recommended PCB layer count is 4. The recommended PCB layer distribution is as follows:

Layer	Method 1	Method 2
Top	USB 3.0 differential signal	USB2.0 high-speed signal, control signal
2nd	GND	POWER、GND
3rd	POWER、GND	GND
Bottom	USB2.0 high-speed signal, control signal	USB 3.0 differential signal

If you need to design according to a 2-layer board, you need to pay attention to several aspects of routing, including: impedance matching, wiring rules, and signal integrity.

(1) Impedance matching: USB3.0 signal routing needs to be impedance matched according to the USB specification.

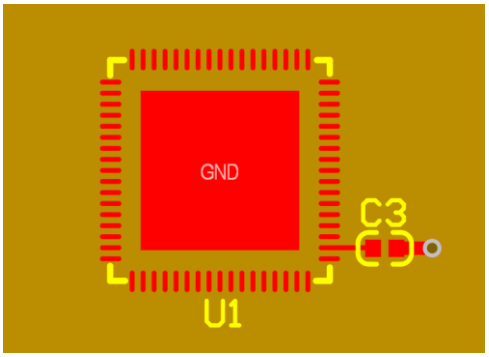
(2) Wiring rules: According to the description in the previous document, differential routing, via processing, equal length processing, grounding processing, and signal integrity processing are performed.

5. Power supply and decoupling capacitors

(1) Decoupling capacitors (such as 0.1uF and 10uF) need to be placed near the power pins to reduce power noise. The decoupling capacitors should be placed as close to the chip pins as possible.

C3 in the figure below is a 0.1uF power decoupling capacitor. It should be placed as close to the corresponding chip pins as possible.

Schematic diagram of decoupling capacitor placement



(2) The width of all power lines is recommended to be greater than 30 mils. If the power supply is on the second or third layer, the width is recommended to be greater than 35 mils.