EE224: Course Project

IITB-CPU

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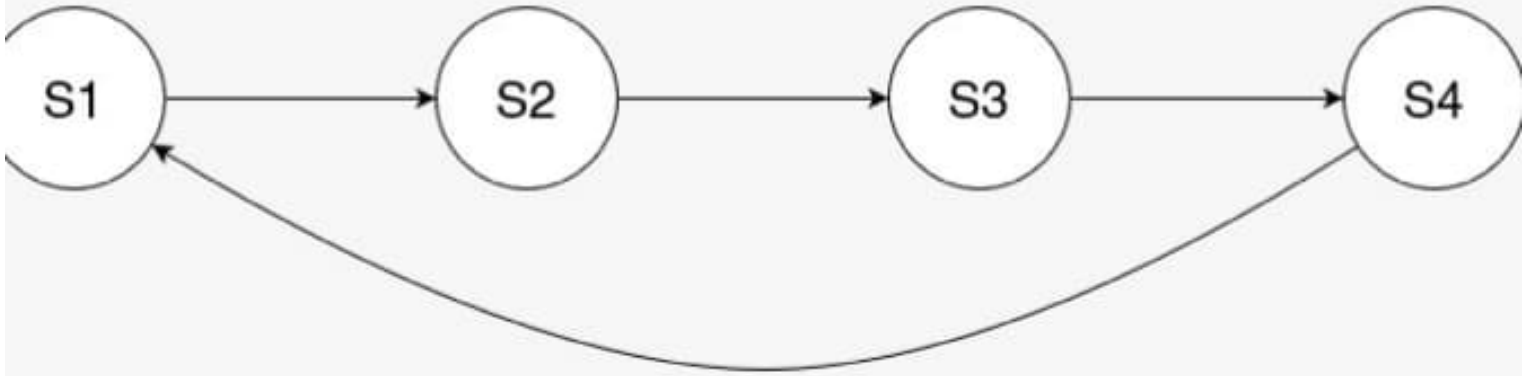
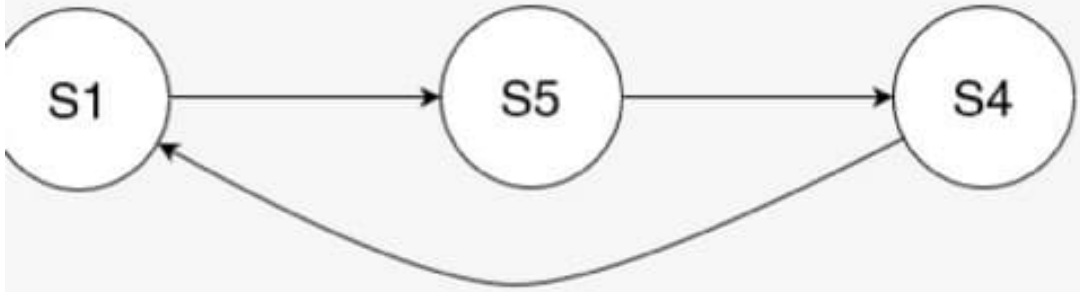
Major Components used in our DataPath:

1) Memory
2) ALU
3) Serial Extender
4) Temporary Registers
5) Register File
6) Multiplexer
7) Decoder
8) Universal Shifter
9) Flag registers
10) Instruction Register.

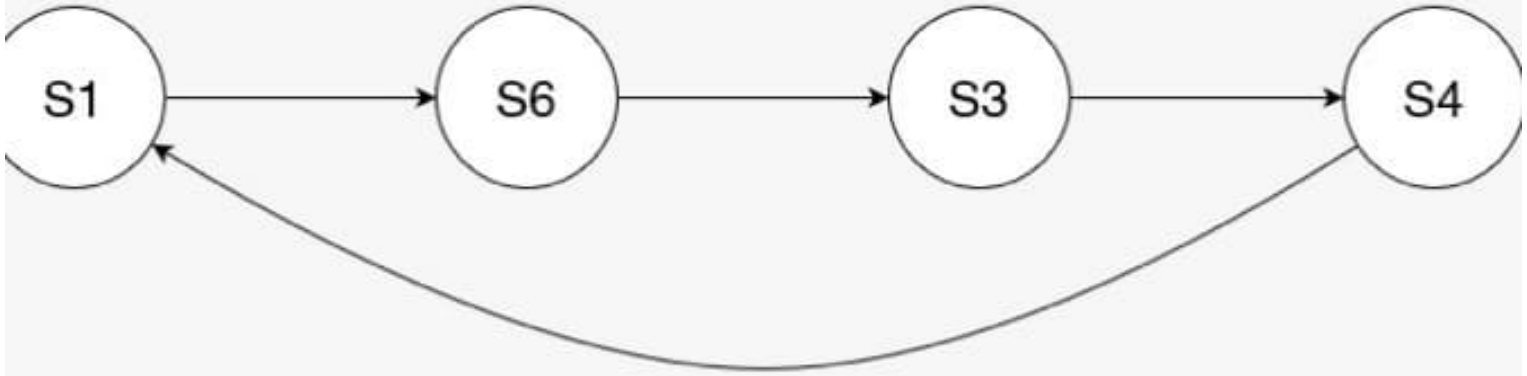
ALU



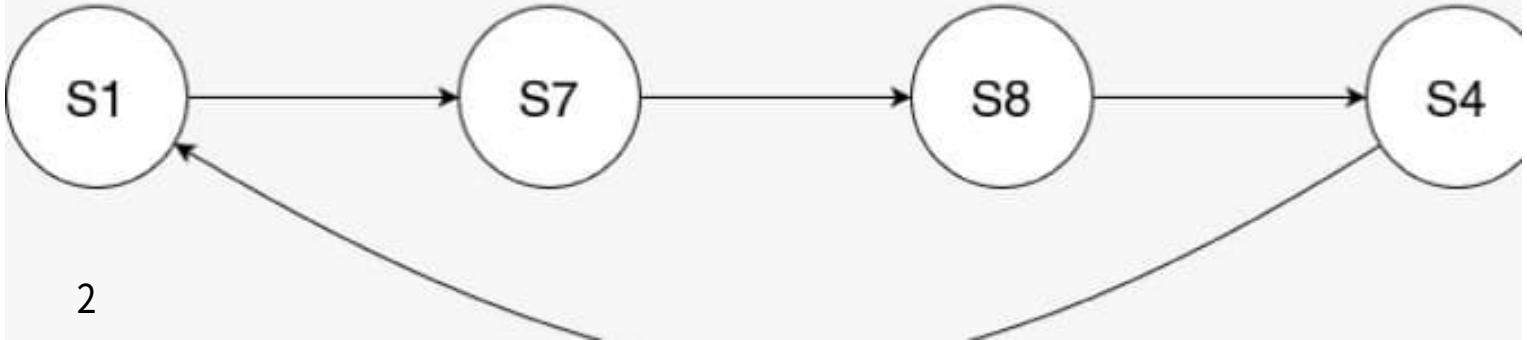
J- Type



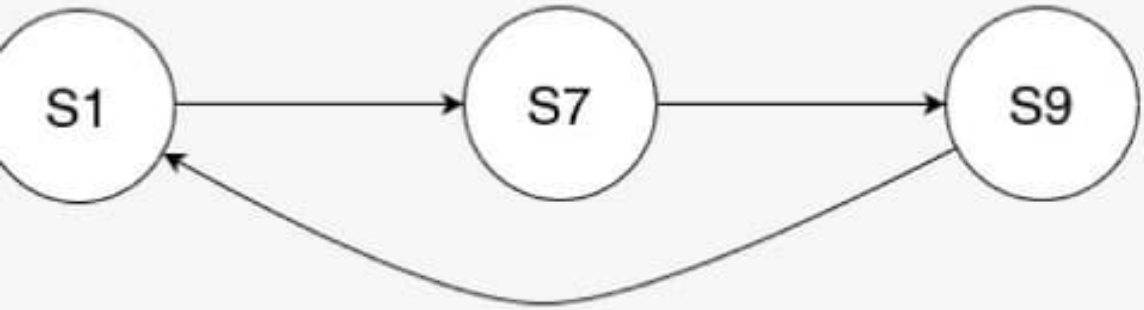
ADI



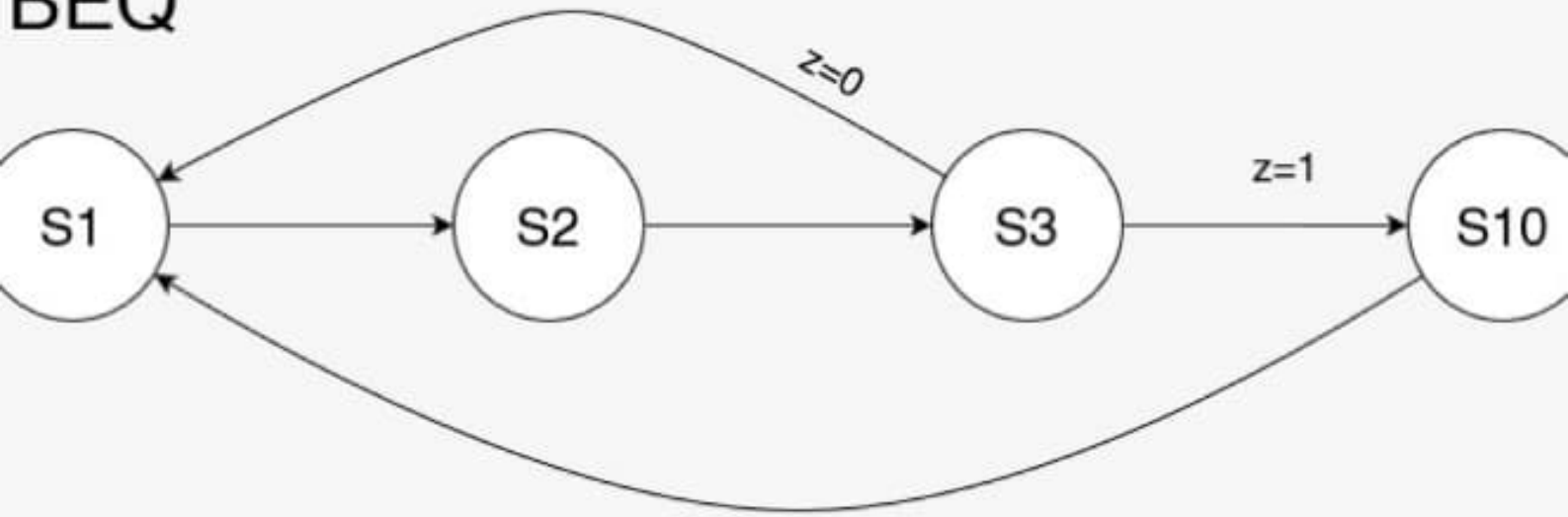
LW



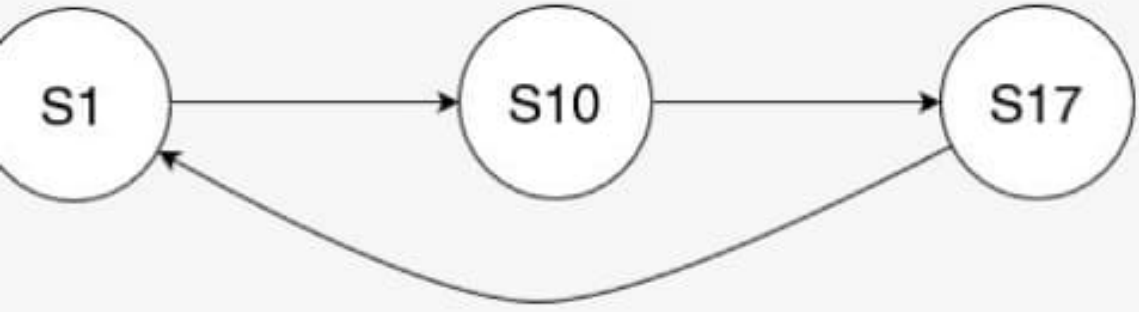
SW



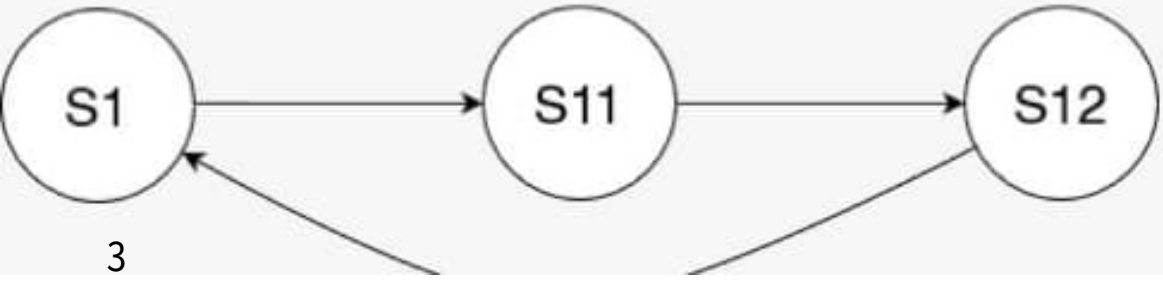
BEQ



JAL



JLR



States:

→ State description:

State 1: Read from memory and increment PC
State 2: Read Instruction (R type)
State 3: Execute specific ALU operation
State 4: Update Result
State 5: Read Instruction (LHI/LLI)
State 6: Read Instruction (ADI type)
State 7: Read Instruction (LW, SW type)
State 8: Read from memory
State 9: Store Memory
State 10: Branch To PC + Imm * 2
State 11: PC to Reg A.
State 12: Branch to Reg B

→ State functions

State 1:

"111"	→ A	RF_WR
01	→ Mem_Add	Mem_Read
01	→ ALU_A	IR_WR
Increment 1	→ ALU_B	R_WR
ALU_C	→ D3	OP
"111"	→ A	T_S_WR
Mem_Data	→ IR	
01	→ T_S	

State 2:

$IR_{11:9} \longrightarrow RF\_A_1$ $\quad T_1\_cl$

$IR_{8:6} \longrightarrow RF\_A_2$ $\quad T_2\_cl$

$RF\_D_1 \longrightarrow T_1$ $\quad T_4\_cl$

$RF\_D_2 \longrightarrow T_2$

$IR_{5:3} \longrightarrow T_4$

State 3:

$T_1 \longrightarrow ALU\_A$ $\quad ADD\ (OP)$

$T_2 \longrightarrow ALU\_B$ $\quad T_3\_cl$

$ALU\_C \longrightarrow T_3$

$ALU\_Z \longrightarrow Zin$

State 4:

$T_3 \longrightarrow RF\_D_3$ $\quad RF\_cl$

$T_4 \longrightarrow RF\_A_3$

State 5:

$IR_{8:0} \longrightarrow Shifter\_In$

$Shifter\_Out \longrightarrow T_3$

$IR_{11:9} \longrightarrow T_4$

State 6:

$IR_{9:11} \longrightarrow A1$ $\quad T_1\_cl$

$D1 \longrightarrow T1$ $\quad T_4\_cl$

$IR_{8:6} \longrightarrow T_4$

$IR_{0:5} \longrightarrow SE6\_IN$

$SE6OUT \longrightarrow T2$

State 7:

$IR_{9:11} \longrightarrow T_4$ $\quad T_4\_ld$

$IR_{0:6} \longrightarrow SE6\_IN$ $\quad T_3\_ld$

$SE6\_OUT \longrightarrow ALU\_A$

$IR_{6:8} \longrightarrow A2$

$O2 \longrightarrow ALU\_B$

$ALU\_C \longrightarrow T_3$

$IR_{9:11} \longrightarrow A_1$

$O1 \longrightarrow T1$

State 8:

$T_3 \longrightarrow Mem\_Add$ $\quad Mem\_Read$

$Mem\_Out \longrightarrow T_3$

State 9:

$T_1 \longrightarrow Mem\_In$ $\quad Mem\_write$

$T_3 \longrightarrow Mem\_Add$

State 10:

$T_5 \longrightarrow ALU\_A$

$Imm \longrightarrow SE_6\_In$

$SE_6\_out \xrightarrow[by\ 1]{leftShift} ALU\_B \rightarrow if\ (Z == 1)$

$ALU\_C \longrightarrow O_3$

$"111" \longrightarrow A_3$ $\quad RF\_wr$

State 11:

IR $\longrightarrow$ A_3 RF_wl

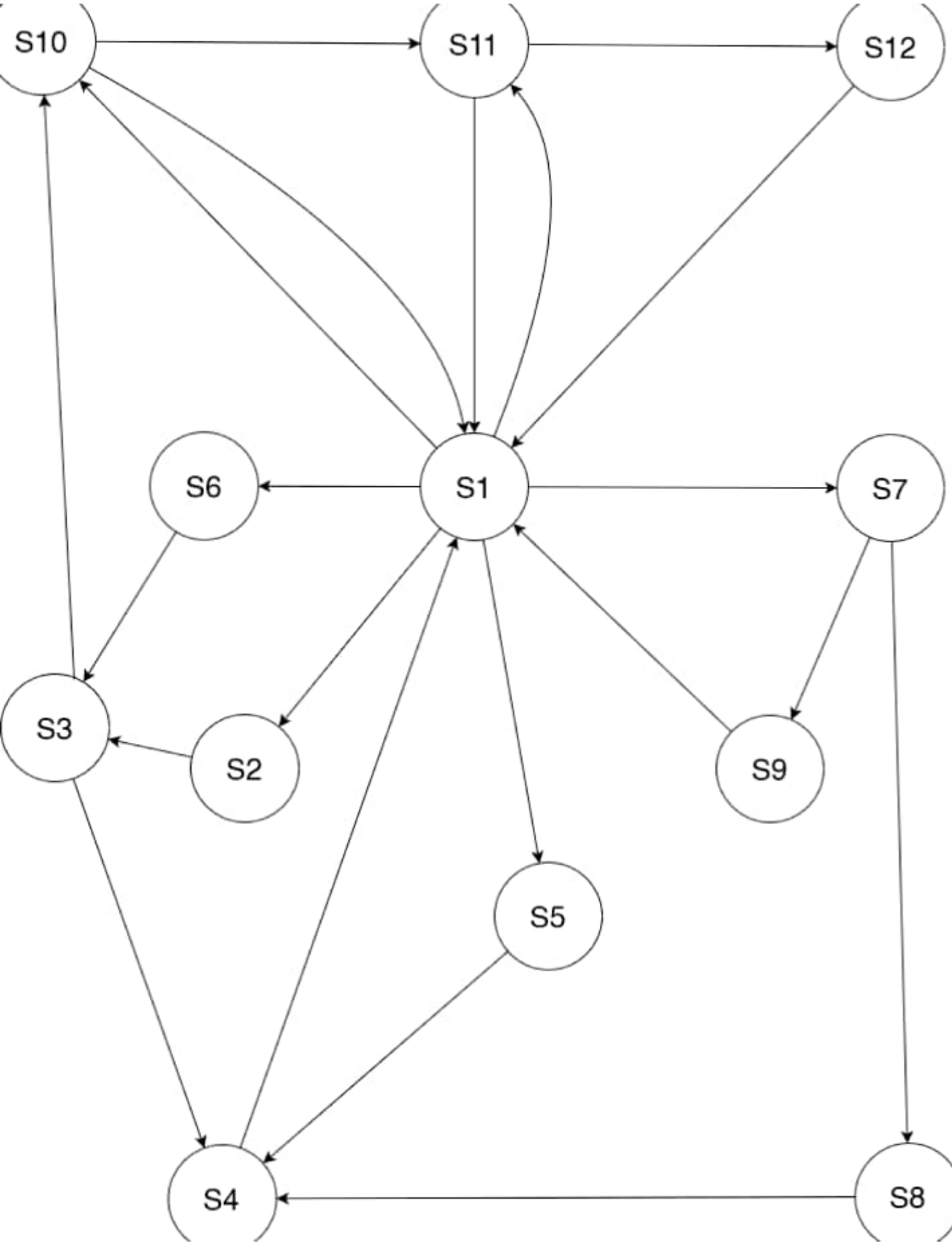
T_5 $\longrightarrow$ D_3

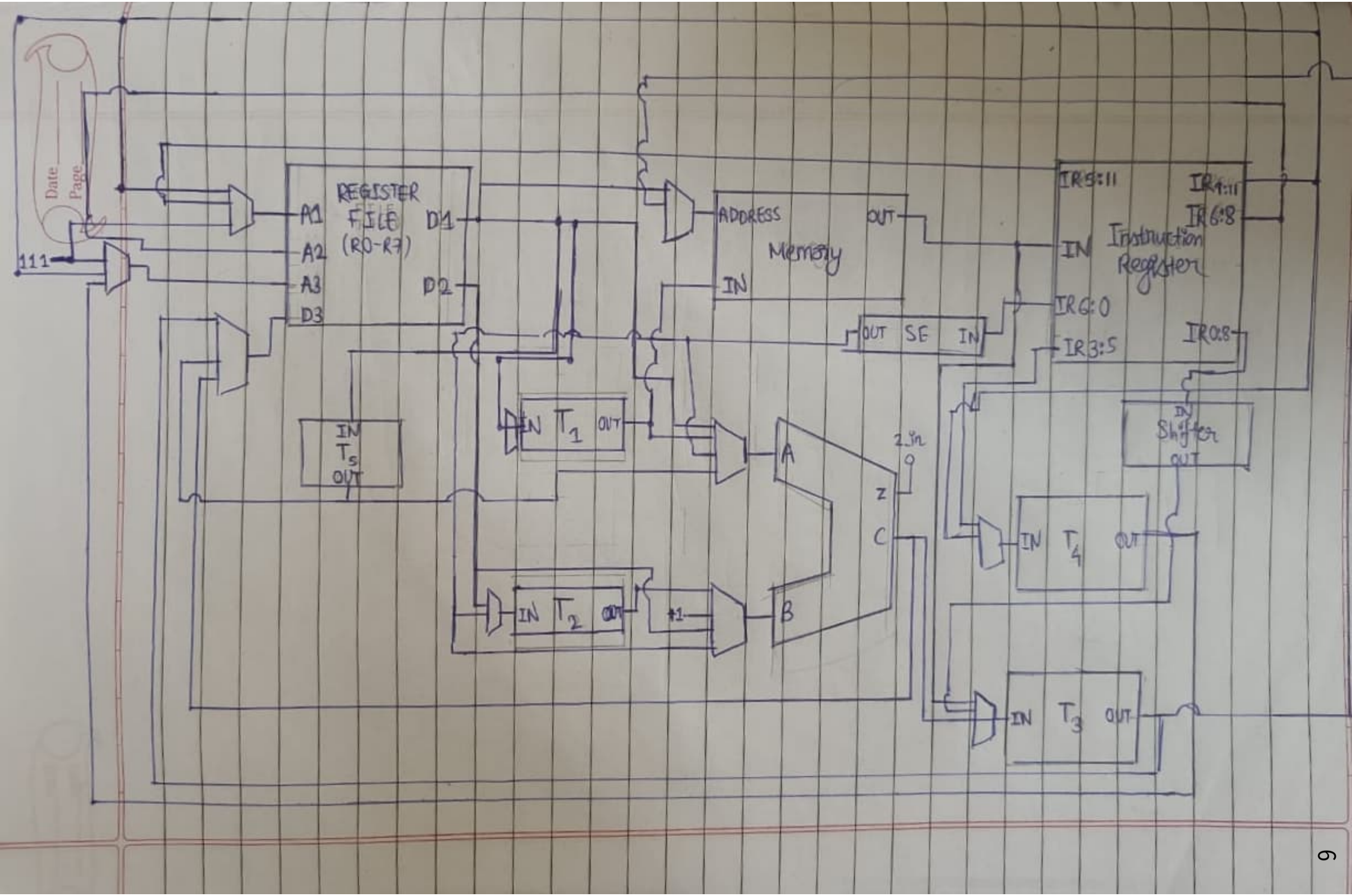
State 12:

IR $\longrightarrow$ A_2 RF_wl

D_2 $\longrightarrow$ D_3

"111" $\longrightarrow$ A_3


S10
S11
S12
S6
S1
S7
S3
S2
S9
S5
S4
S8


REGISTER FILE (R0-R7)
A1
A2
A3
D3
D1
D2
111
ADDRESS
Memory
IN
OUT
OUT SE IN
IR 5:11
IR 6:8
IR 0:5
IR 3:5
IR 0:8
Instruction Register
IN
Shifter
OUT
IN T_1 OUT
IN T_2 OUT
IN T_3 OUT
IN T_4 OUT
IN T_5 OUT
+1
A
B
Z
C
2 in