Row Buffer Management Policies

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Abstract

To implement a Hybrid-Row-Buffer-Management Policy (Adaptive Management Policy).

1. Implementation of the Row Buffer Management Policy

We implemented a 4-bit saturation counter, and chose two threshold values, 10 and 6 for High-Threshold and Low-Threshold respectively.

Initially we have set the counter to 8, and started with open based policy.

We switch from open to closed based policy if the counter exceeds the High-Threshold, and from closed to open based policy if the counter drops bellow the Low-Threshold.

Under Open-Page policy, if there is a page miss then we increment the counter. For this, we use the dram_state array specified in the memory controller, this gives the row which is currently active, if this is not equal to the row specified by the request then, the miss is identified and the counter is changed.

Under Closed-Page policy, if there is a page hit with the last closed page, then counter is decre.mented. For this we created a recent closed array, which keeps track of the previously closed page. Then we compare the current page with it, if it is the same then counter is changed accordingly.

In any other case no action is taken.

2. The Best Policy - Cycles taken by each policy

Open based

2cores - input/black – Cycles 208459212
2 cores - input/freq – Cycles 208459212

2 cores - input/comm1 - Cycles 257303732

2 cores – input/comm1 - Cycles 347019637
2 cores – input/comm2 - Cycles 347019637

1 core – input/comm2 - Cycles 303069945

2 cores – input/face, 2 cores – input/ferret - Cycles 272933485

2 cores each for – input/fluid, input/swapt, input/comm2, input/ferret - Cycles 421758733

2 cores each for – input/fluid, input/swapt, input/comm2, input/ferret, input/black, input/freq, input/comm1, input/stream - Cycles 530213121

2 cores – input/comm2, 1 core each for – input/fluid, input/swapt - Cycles 343904097

1 core each – input/MT0, input/MT1, input/MT2, input/MT3 - Cycles 450486649

4 cores – input/stream - Cycles 215059516

Closed Based

2cores - input/black – Cycles 197510088
2 cores - input/freq – Cycles 197510088

2 cores - input/comm1 - Cycles 232536352

2 cores – input/comm1 - Cycles 318549289
2 cores – input/comm2 - Cycles 318549289

1 core – input/comm2 - Cycles 269006193

2 cores – input/face, 2 cores – input/ferret - Cycles 255357697

2 cores each for – input/fluid, input/swapt, input/comm2, input/ferret - Cycles 392935533

2 cores each for – input/fluid, input/swapt, input/comm2, input/ferret, input/black, input/freq, input/comm1, input/stream - Cycles 498002125

2 cores – input/comm2, 1 core each for – input/fluid, input/swapt - Cycles 314517769

1 core each – input/MT0, input/MT1, input/MT2, input/MT3 - Cycles 421163857

4 cores – input/stream - Cycles 203539368

Hybrid Based

2cores - input/black – Cycles 197317152
2 cores - input/freq – Cycles 197317152

2 cores - input/comm1 - Cycles 232050868

2 cores – input/comm1 - Cycles 318374645
2 cores – input/comm2 - Cycles 318374645

1 core – input/comm2 - Cycles 269034753

2 cores – input/face, 2 cores – input/ferret - Cycles 255412501

2 cores each for – input/fluid, input/swapt, input/comm2, input/ferret - Cycles 393107393

2 cores each for – input/fluid, input/swapt, input/comm2, input/ferret, input/black, input/freq, input/comm1, input/stream - Cycles 498585945

2 cores – input/comm2, 1 core each for – input/fluid, input/swapt - Cycles 314477061

1 core each – input/MT0, input/MT1, input/MT2, input/MT3 - Cycles 421104269

4 cores – input/stream - Cycles 203639468

Since, closed-page policy performed better on 5 test parameters and hybrid-policy on 5 test. We say that hybrid implementation is better.

3. Two Address Mapping comparison

For Address mapping 2

Hybrid Based

2cores - input/black – Cycles 197317152
2 cores - input/freq – Cycles 197317152

2 cores - input/comm1 - Cycles 232050868

2 cores – input/comm1 - Cycles 318374645
2 cores – input/comm2 - Cycles 318374645

1 core – input/comm2 - Cycles 269034753

2 cores – input/face, 2 cores – input/ferret - Cycles 255412501

2 cores each for – input/fluid, input/swapt, input/comm2, input/ferret - Cycles 393107393

2 cores each for – input/fluid, input/swapt, input/comm2, input/ferret, input/black, input/freq, input/comm1, input/stream - Cycles 498585945

2 cores – input/comm2, 1 core each for – input/fluid, input/swapt - Cycles 314477061

1 core each – input/MT0, input/MT1, input/MT2, input/MT3 - Cycles 421104269

4 cores – input/stream - Cycles 203639468

For Address Mapping 0

Hybrid Based

2cores - input/black – Cycles 199356088
2 cores - input/freq – Cycles 199356088

2 cores - input/comm1 - Cycles 236611668

2 cores – input/comm1 - Cycles 314418420
2 cores – input/comm2 - Cycles 314418420

1 core – input/comm2 - Cycles 261421748

2 cores – input/face, 2 cores – input/ferret - Cycles 299555964

2 cores each for – input/fluid, input/swapt, input/comm2, input/ferret - Cycles 416882840

2 cores each for – input/fluid, input/swapt, input/comm2, input/ferret, input/black, input/freq, input/comm1, input/stream - Cycles 517556240

2 cores – input/comm2, 1 core each for – input/fluid, input/swapt - Cycles 323249048

1 core each – input/MT0, input/MT1, input/MT2, input/MT3 - Cycles 424806505

4 cores – input/stream - Cycles 213979040

Table Of Performance - Cycles

	Open	Closed	Hybrid
1 Test	208459212	197510088	197317152
2 Test	257303732	232550868	232036352
3 Test	347019637	318549289	318374645
4 Test	303069945	269006193	269034753
5 Test	272933485	255357697	255412501
6 Test	421758733	392935533	393107393
7 Test	530213121	498002125	498585945
8 Test	343904097	314517769	314477061
9 Test	450486649	421163857	421104269

10 Test	215059516	203539368	203639468