ProNoC

Interface Generator
User Manual

Summary

The IP generator allows adding new intellectual properties (IPs) to the ProNoC's library. It provides a GUI interface for mapping the module ports to the interfaces, defining how the module parameters must be collected from the user, add the list of source files and etc.

Generate a New IP

For adding a new IP to ProNoC first you need to have the Verilog file(s) describing the RTL code of the IP.

1. Click on 

button and select the Verilog file containing the top level module.

2. In case the verilog file contains several Verilog module select the top level module in "Select Module" field. Also define a name and category for the new IP. All IPs belong to the same category are listed under same tree branch in processing tile generator.

3. Using 

button you can add a short description about the IP. This description will be shown when the IP is selected in processing tile generator.

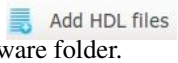
4. The 

button alllows you to define the header file for this peripheral device. You can use two variable of $BASEn and $IP in the header file. $BASE is the wishbone base address(es) and will be added during tile generation to tile_name.h file. If more than one slave wishbone bus are used define them as $BASE0, $BASE1 ... $BASEn. $IP: is the peripheral device name. When more than one peripheral device is allowed to be called in a tile, it is recommended to add $IP to the global variables, definitions and functions.

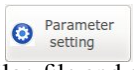
   header file example

```
#define $IP_REG_0    (*((volatile unsigned int *) ($BASE)))
#define $IP_REG_1    (*((volatile unsigned int *) ($BASE+4)))


#define $IP_WRITE_REG1(value)   $IP_REG_1=value
#define $IP_READ_REG1()         $IP_REG_1
```

5. Add the HDL files list by using 

button. All files listed here will be copied in the generated hardware folder.

6. By 

pressing button it extract all parameters inside the top module Verilog file and allow you to add, remove and define how to get their value from the user.

   - **Parameter name**: It is the parameter name which has been read from the verilog file.
   - **Default value**: When an IP is selected for first time in processing tile generator the parameter are loaded by this default value.

- **Widget type**: define how the parameter value must be taken from the user when loading the IP in processing tile generator. There are four ways to define it:
  - **Fixed**: The parameter is a fixed value and get the default value. User will not see the parameter and cannot change it.
  - **Entry**: The parameter value is received via *entry* widget. The user can type anything.
  - **Combo-box**: The parameter value can be selected from a list of pre-defined value.
  - **Spin-box**: The parameter is numeric and will be adjust using spin-box widget.
- **Widget content**: For Fixed and Entry leave it empty. For Combo box define the parameters which must be shown in combo box as: ”PAEAMETER1”,”PARAMETER2”...,”PARAMETERn”. For Spin box define it as ”minimum, maximum, step” e.g 0,10,1.
- **Parameter** if the parameter check box is on, the IP parameter will be defined as parameter in tile Verilog file as well, otherwise it will be defined as localparam. All tile parameters can be changed during MPSoC generator, allows calling same tile in different places with different parameter values.
- **Redefine**: If checked, the defined parameter/localparam in SoC will be passed to the IP core.

```
parameter PARAM1= n;  //redefined is on
localparam PARAM2=m;  //redefined is off

ip_name #(
        // redefined parameters
        .PARAM1(PARAM1)
) instance_name(
//ports

);
```

7. Add interface: You can add interfaces to the IP library by double clicking on an interfaces name located at the left top corner. After adding the interface it will appear in the interface box where you can adjust the interface setting such as, interface name, type, interface number. For wishbone slave interface you can select the wishbone address setting by pressing  button and do the following settings:

   - **Interface name**: define a name for each interface.
   - **Address Range**: select the address range for wishbone slave port.
   - **Block address setting**: define the maximum memory size required for this interface. It can be defined as a fixed number when the number of memory mapped register inside the interface is fixed or it can be defined by a parameter inside the IP Verilog file when the number of memory mapped

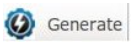
register depends on a parameter i.e. in a memory block which its size is parameterizable.

For socket interfaces, there is an option define the interface number as parameter (by selecting 

) or a fixed number by selecting 

condition.

8. After adding the interfaces you must mapped the top module ports to the interfaces ports. For each top level module port u need to define the interface name and interface port.

9. Finally by pressing 

you can generate the IP. You can also modify the previously added IPs by using 

button.