Processing Tile Generator user manual

January 28, 2016

A Processing Tile is a set of several IPs (processors and peripheral devices) connecting via interfaces. IPs can be selected from the left top corner. By double clicking on one IP, it will be added to the tile generator. Each IP box contain a setting button which allows to redefine the IP parameters. The IP box provide a gui interface for connecting the IPs interfaces. For each interface it lists the available contestable interfaces which the user can select among them.

1 Example

For an example, we want to generate a processing tile as shown in Figure 1. This example contain several IPs connected using one shared wishbone bus. From the IP list we select all 9 IPs which are needed for this processing tile. Note that one IP can be called several times with each has its own unique instance name.

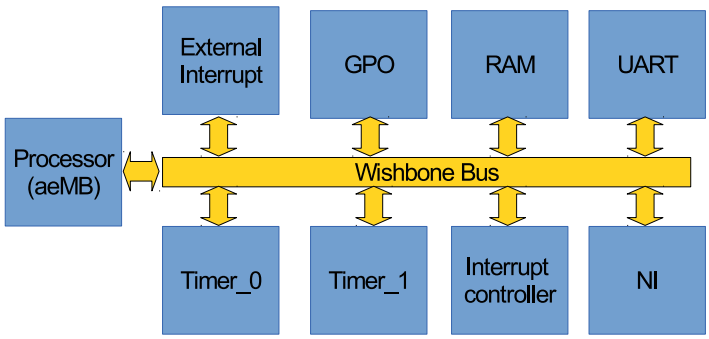


Figure 1:

Now we need to add two more components. A clock source and a wishbone bus. For wishbone bus you need to define the number of master and slave interfaces in parameter setting. Hence, we need to count the number of master

and slave interfaces to the wishbone bus. In this example aeMb has two and NI has one master interfaces. All peripheral devices here have one wishbone slave interface. As a result the wishbone bus has 3 master and 8 slave interfaces. These values are inserted by selecting setting button of wishbone bus as shown in Figure 2. We also need to define the number of intrrupt signals that the interrupt controller needs to handle which is 5 here. If the interrupt signal of a peripheral device is not needed you can simply leave it as NC, which means not connected.

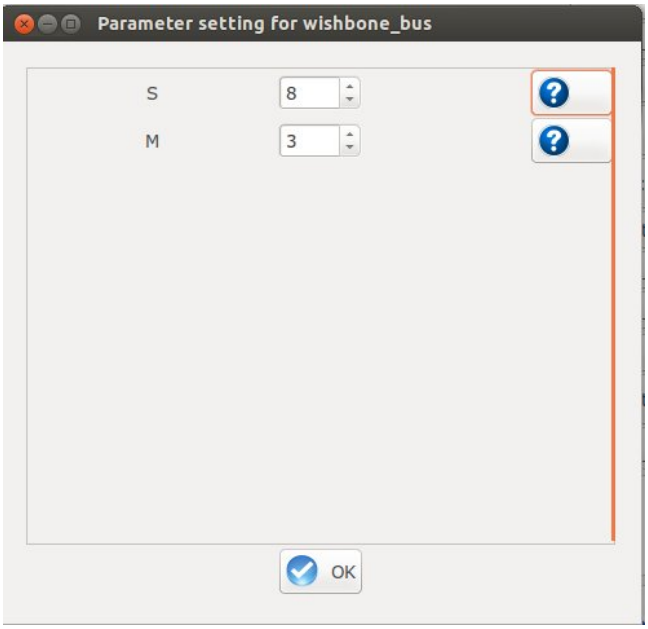
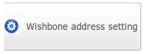


Figure 2:

After setting all IPs parameter, you can start with the connections. It is really simple as the list of all possible connection for an interface is available in a combo-box widget. Figure 3 shows the snapshot of PT generator. Here we shows the list of available connections for wishbone slave interface of timer 0. The connected interfaces are also shown in the list by "->" sign.

After doing the connection, the last things is to check the wishbone address setting. The wishbone slave addresses are assigned automatically based o the range and size which is given to the IP module during IP generation stage. By clicking on 

you can see the assigned wishbone addresses as shown in Figure 4. In this example the RAM address automatically assigned based on the defined memory size while the rest IPs had a fixed 4 (32-bit) register. You can also manually change the addresses. If there is no conflict in assigned addresses, the status must show  , otherwise  sign.

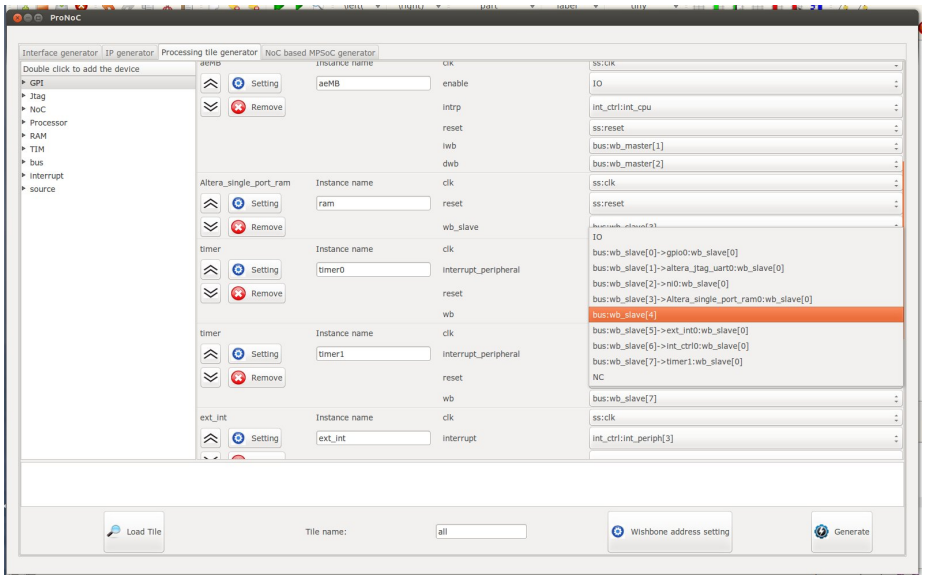


Figure 3: Processing tile generator snapshot.

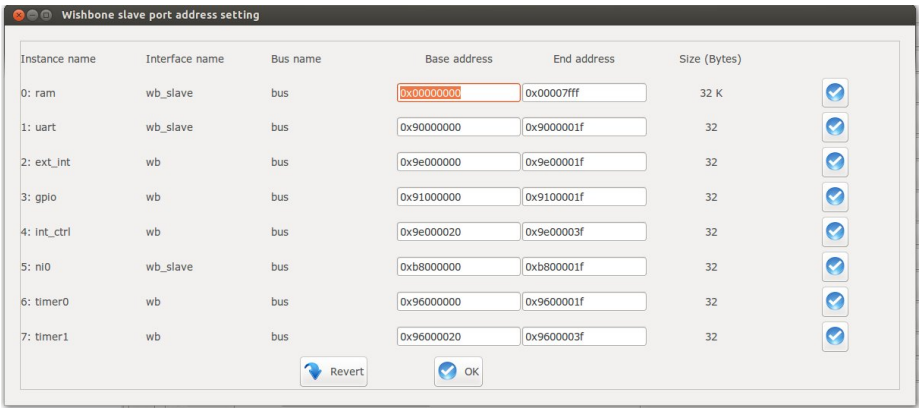


Figure 4: Wishbone address setting snapshot

Finally by pressing  you can generate the the processing tile. It will generate a top level Veriolog file containing the processing tile, plus required programming file and Verilog sources. You can also modify the previously added IPs by using  button. You can find several examples such as blinking led and interrupt test inside the example folder.