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CMT2300A Configuration Guideline

Introduction

The purpose of this document is to provide the guidelines for the users to configure the CMT2300A on the RFPDK. The part number covered by this document is shown in the table below.

Table 1. Part Number Covered in this Document

Part Number	Description	
CMT2300A	Ultra low power, high performance, OOK and (G)FSK RF transceiver for various 300 to 960 MHz wireless applications. It is part of the CMOSTEK NextGenRF TM family, which includes a complete line of	
	transmitters, receivers and transceivers.	

The RFPDK (RF Products Development Kit) is a PC application developed by CMOSTEK for the NextGenRFTM product line. Differing from traditional RF chip configuration methods, which usually require complex software programming and register-based controlling, the RFPKD revolutionarily simplifies the NextGenRFTM product configurations. The user can easily complete the product configuration by just clicking and inputting a few parameters. After that, the product can be directly used in the RF system without performing any further configurations.

This document describes the details of how to configure the features/parameters of the CMT2300A with the RFPDK.

To help the user develop their application with CMT2300A easily, CMOSTEK provides **CMT2300A Dual-Way RF Link Development Kits** that enables the user to quickly evaluate the performance, demonstrate the features and develop the application. The Development Kits includes:

- RFPDK
- USB Programmer
- RF-EB (evaluation boards for NextGenRFTM products)
- CMT2300A-EM (register control based TRx modules)

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1. Getting Started

Install RFPDK on the computer. The detail of the installation can be found in Chapter 7 of "AN103 CMT2110A/2210A One-Way RF Link Development Kits User's Guide".

Setup the development kits as shown in figure below before configuring the CMT2300A. The Application can be the CMT2300A-EM provided by CMOSTEK, or the PCB designed by the user with CMT2300A.

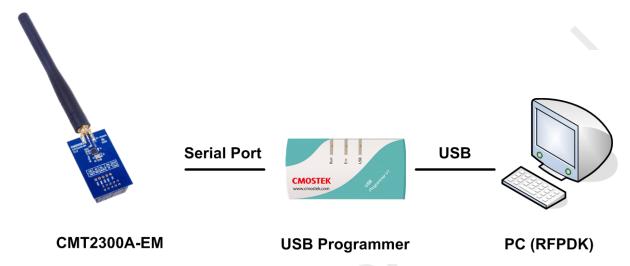


Figure 1. CMT2300A Configuration Setup

Start the RFPDK from the computer's desktop and select CMT2300A in the Device Selection Panel shown in figure below. Once a device is selected, the Device Control Panel appears as shown in Figure 3.

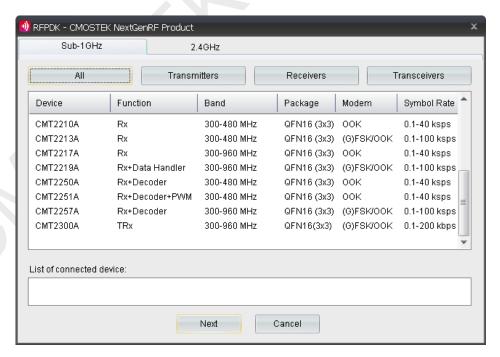


Figure 2. Device Selection Panel

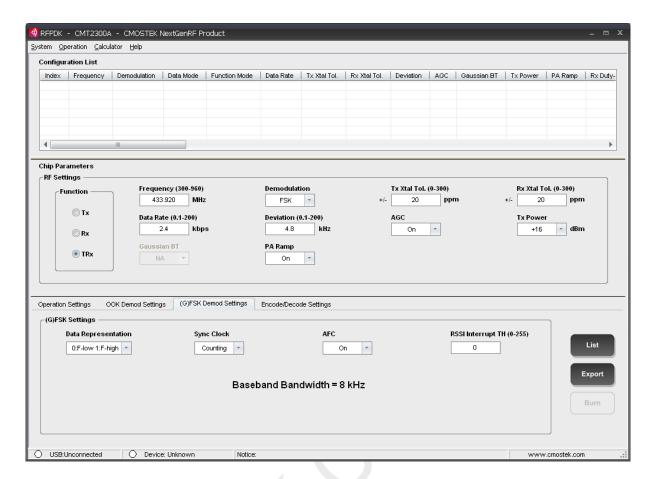


Figure 3. Device Control Panel

2. RF Settings

In the following chapters, the TRx function is chosen as the example to explain all of the configuration parameters. Both the Tx and Rx functions are a subset of the TRx function.



Figure 4. RF Settings

As shown in figure 4, the Tx, Rx and TRx options allow the RFPDK to display the parameters that are only used in the selected function. For example, if the device will be used as a transmitter only, by selecting the Tx, then the Rx related parameters will be disabled to fill in.

Table 2. RF Settings Parameters

Parameters	Descriptions	Default	Function
Frequency	The receive radio frequency, the range is from 300 to 960 MHz, with resolution of 0.001 MHz.	433.920 MHz	TRx
Demodulation	The demodulation type, the options are: OOK, FSK or GFSK demodulation.	FSK	TRx
Tx Xtal Tol.	The crystal frequency tolerance of the Tx side, the range is from 0 to ±300 ppm.	±20 ppm	Rx
Rx Xtal Tol.	The crystal frequency tolerance of the Rx side, the range is from 0 to ±300 ppm.	±20 ppm	Rx
Data Rate	The data rate, the range is from 0.1 to 200 kbps, with resolution of 0.1 kbps.	2.4 kbps	TRx
Deviation	The (G)FSK frequency deviation, the range is from 0.1 to 200 kHz, with resolution of 0.1 kHz.	4.8 kHz	TRx
AGC	The Automatic Gain Control for the demodulation, the options are: On or Off.	On	Rx
Tx Power	The transmitting output power, the range is from -20 dBm to +16dBm, in 1 dBm step size.	+16 dBm	Tx
Gaussian BT	The BT for the Gaussian Filter of the GFSK mode. The options are: 0.3, 0.5, 0.8 or 1. It is only available when GFSK is chosen.	0.5	Тх
PA Ramping	The PA output ramping control, the options are: On or Off.	On	Tx

2.1 Frequency

CMT2300A covers a wide range of the receive radio frequency from 300 to 960 MHz. The frequency is accurate to three decimal places on the RFPDK.

2.2 Modem

CMT2300A supports OOK, FSK and GFSK modulation/demodulation.

2.3 Data Rate

CMT2300A supports 0.1 - 200.0 kbps data rate for (G)FSK modem and 0.1 - 40 kbps data rate for OOK modem. With the Sync Clock turned off, the receiver is able to tolerate a wide range of data rate error. The less data rate error exists between the Tx and Rx, the higher performance the device can achieve.

If the sync clock technique is chosen as counting, the data rate tolerance is determined by the number of consecutive zeros/ones in the data packet. The computation can be done by:

$$Data\ Rate\ Tolerance = \frac{\pm 50\%}{Number\ of\ Consecutive\ Zeros\ or\ Ones}$$

For example, if the largest number of consecutive zeros/ones in the packet is 4, then the data rate tolerance is ±12.5%. The more number of long zeros or ones exist, the less error the receiver can tolerate.

If the sync clock technique is chosen as tracing, the maximum data rate tolerance is about ±8%.

If the sync clock is turned off, for FSK demodulation, the data error tolerance can be as large as $\pm 50\%$.

2.4 Deviation

The device supports a wide range of deviations in (G)FSK mode. The deviation is the maximum instantaneous difference between the modulated frequency and the nominal carrier frequency Fo.

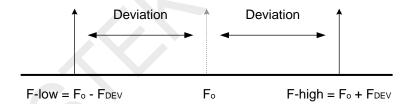


Figure 5. (G)FSK Deviation

The RFPDK will compute the receiver bandwidth according to the modulation index and the frequency error between a transmitter and the pairing receiver. The modulation index is given by:

$$Modulation\ Index = \frac{2 * F_{DEV}}{DR}$$

The deviation range that can be set on the RFPDK is from 0.1 to 200 kHz with a resolution of 25 Hz. To achieve the best performance, the user is recommended to follow below rules:

- Try to set the deviation in the range of 2 100 kHz
- When Data Rate is less than or equal to 50 kbps, Modulation Index = 2, i.e. F_{DEV} = DR
- When Data Rate is larger than 50 kbps, Modulation Index = 1, i.e. F_{DEV} = DR / 2

The baseband bandwidth, shown in the (G)FSK Demod Settings window, is a reference for the user to adjust the data rate, deviation and the crystal tolerance. The smaller the bandwidth is displayed, the better of sensitivity the device can achieve.

Once the AFC function is turned on, the receiver will try to remove the frequency error from a pairing transmitter, which is usually caused by the crystal tolerance, and reallocate the received signal inside the baseband bandwidth.

2.5 AGC

The Automatic Gain Control helps the device to deal with the co-channel interference. In OOK demodulation, AGC is always recommended to be turned.

2.6 Tx Power

Tx Power can be configured from -20 dBm to +16 dBm in 1 dB step size. The actual output power could be slightly different due to the user's PCB layout and the components used for matching network may differ from CMOSTEK's recommendations. Therefore, the user should select the proper value from the Tx Power pull down menu to meet the system output power requirement according to the actual measurement.

2.7 Gaussian BT

The Bandwidth Time product of the Gaussian Filter is for GFSK modulation. The Gaussian Filter is designed to reduce unwanted spectral components. The typical value of B*T is 0.5. However, the user is free to choose one of the 4 options that satisfy the desired transmitting frequency spectrum.

2.8 PA Ramp

The PA incorporates automatic ramp-up and ramp-down control to reduce unwanted spectral spreading. The ramping level is automatically optimized to its best value by the RFPDK.

3. Operation Settings



Figure 6. Operation Settings

The available operating options for the radio control are listed in the table below.

Table 3. Operation Settings Parameters

Parameters	Descriptions	Default	Function
Rx Duty-Cycle Mode	This turns on/off the receiver duty-cycle mode. The options are on or off.	Off	Rx
Sleep Timer	This turns on/off the sleep timer. It must be turned on when Rx Duty-Cycle Mode is turned on.	Off	TRx
Sleep Time	This parameter is only available when the Sleep Timer is turned on. The sleep time has the range from 3 to 134,152,192 ms.	10 ms	TRx
Rx Timer	This turns on/off the receive timer. It must be turned on when Rx Duty-Cycle Mode is turned on.	Off	Rx
Rx Time	This parameter is only available when the Rx Timer is turned on. The receive time has the range from 0.04 to 2,683,043.00 ms.	20.00 ms	Rx
Rx Time Ext	The extended receive time has the range from 0.04 to 2,683,043.00 ms. It is only available when Wake-On Radio is turned on and the Rx Timer is turned on.	200.00 ms	Rx
State After Rx Exit	This defines which state the device will switch to after finishing the receiving. The options are: SLEEP, STBY or RFS. It must be set to SLEEP when Rx Duty-Cycle Mode is turned on.	STBY	Rx
State After Tx Exit	This defines which state the device will switch to after finishing the transmission in packet mode. The options are: SLEEP, STBY or TFS. It is only available when Packet mode is used.	STBY	Tx
Wake-On Radio	Turn on/off the wake-on radio function, the options are: on or off.	Off	Rx
Wake-On Condition	The condition to wake on the radio, the options are: 1. Extended by RSSI 2. Extended by Preamble 3. Extended by Ext-Code 4. Switched to Rx Ext by RSSI	Extended by Preamble	Rx

5. Switched to Rx Ext by Preamble		
6. Switched to Rx Ext by Ext-Code		
7. Switched to Rx Ext by Preamble, extended by Sync		
8. Switched to Rx Ext by Ext-Code, extended by Sync		
It is only available when Wake-On Radio is turned on		
-		
3 3 3 3 3 3 4 3		
Extended Code for the WOR, it only available when		
Wake-On Condition is set to the type 3, 6 or 8. The range	0	Rx
is from 0 to 255.		
Turn on/off the system clock output on CLKO, the options	Off	TRx
are: on or off.	Oil	TKX
The system clock output frequency, the options are:		
13.000, 6.500, 4.333, 3.250, 2.600, 2.167, 1.857, 1.625,		
1.444, 1.300, 1.182, 1.083, 1.000, 0.929, 0.867, 0.813,		
0.765, 0.722, 0.684, 0.650, 0.619, 0.591, 0.565, 0.542,	6.500 MHz	TRx
0.520, 0.500, 0.481, 0.464, 0.448, 0.433, 0.419 or 0.406		
MHz. It is only available when System Clock Output is		
turned on.		
The threshold for the low battery detection. The range is		
from 1.9 to 3.3 V.	2.4 V	TRx
	6. Switched to Rx Ext by Ext-Code 7. Switched to Rx Ext by Preamble, extended by Sync 8. Switched to Rx Ext by Ext-Code, extended by Sync It is only available when Wake-On Radio is turned on. When the Rx Duty-Cycle is turned on, only the type 4, 5 and 6 can be used. Extended Code for the WOR, it only available when Wake-On Condition is set to the type 3, 6 or 8. The range is from 0 to 255. Turn on/off the system clock output on CLKO, the options are: on or off. The system clock output frequency, the options are: 13.000, 6.500, 4.333, 3.250, 2.600, 2.167, 1.857, 1.625, 1.444, 1.300, 1.182, 1.083, 1.000, 0.929, 0.867, 0.813, 0.765, 0.722, 0.684, 0.650, 0.619, 0.591, 0.565, 0.542, 0.520, 0.500, 0.481, 0.464, 0.448, 0.433, 0.419 or 0.406 MHz. It is only available when System Clock Output is turned on. The threshold for the low battery detection. The range is	6. Switched to Rx Ext by Ext-Code 7. Switched to Rx Ext by Preamble, extended by Sync 8. Switched to Rx Ext by Ext-Code, extended by Sync It is only available when Wake-On Radio is turned on. When the Rx Duty-Cycle is turned on, only the type 4, 5 and 6 can be used. Extended Code for the WOR, it only available when Wake-On Condition is set to the type 3, 6 or 8. The range is from 0 to 255. Turn on/off the system clock output on CLKO, the options are: on or off. The system clock output frequency, the options are: 13.000, 6.500, 4.333, 3.250, 2.600, 2.167, 1.857, 1.625, 1.444, 1.300, 1.182, 1.083, 1.000, 0.929, 0.867, 0.813, 0.765, 0.722, 0.684, 0.650, 0.619, 0.591, 0.565, 0.542, 0.520, 0.500, 0.481, 0.464, 0.448, 0.433, 0.419 or 0.406 MHz. It is only available when System Clock Output is turned on. The threshold for the low battery detection. The range is

3.1 Rx Duty-Cycle Mode

This parameter enables the device to work in the manually control mode or Rx duty-cycle mode. Once the device works in the duty-cycle mode, it doesn't require control from an external MCU. If the duty-cycle mode is turned on, the following parameters are limited to specific value(s) by the RFPDK:

- Sleep Timer is On
- Rx Timer is On
- State After Rx Exit is SLEEP
- If Wake-On Radio is turned on, the Wake-On Condition can only be set to either Switched to Rx Ext by RSSI, Switched to Rx Ext by Preamble, or Switched to Rx Ext by Ext-Code. This is because the other options require control from an external MCU

Under different circumstances, the external MCU must follow different procedures to enable the device enter the Rx duty-cycle mode.

- By means of programming the embedded EEPROM
 The device will automatically enter the Rx duty-cycle mode after it is powered up. The external MCU does not need to send any command.
- 2. By means of configuring the control registers
 The device stays in the SLEEP state after it is powered up. The MCU must issue the go_stby command to switch the device
 to the STBY state prior to initializing the configuration registers. The MCU then writes the HEX file generated by the RFPDK
 to the configuration registers. The HEX file contains the information that enable the device to work in the Rx duty-cycle mode.

After the configuration the MCU must issue the go_sleep command again to switch the device back to the SLEEP state. The device will automatically enter the Rx duty-cycle mode after receiving the go_sleep command.

3. Manually enter the Rx duty-cycle mode

The MCU can control the device to enter the Rx duty-cycle mode anytime by issuing the following commands.

- Issue go_stby command
- Set DC_EN to 1, to enable the Rx duty-cycle mode
- Set SL_EN to 1, to enable the sleep timer
- Set RX_EN to 1, to enable the Rx timer
- Set RX_EXIT_STA<1:0> to 00, to set the State After Rx Exit to SLEEP
- Issue go_sleep command

Note that above procedures do not involve setting up parameters of the Sleep Time and Rx Time. These two must be configured properly either using EEPROM burning or the Configuration Bank Registers.

In order to exit the Rx duty-cycle mode, the MCU should issue the following commands:

- Set DC_EN to 0, to disable the Rx duty-cycle mode
- Set SL_EN to 0, to disable the sleep timer
- Set RX_EN to 0, to disable the Rx timer
- Set RX_EXIT_STA<1:0> to the desired value (this is optional)
- Issue go_rfs command
- Wait about 20 ms
- Issue go_sleep command

After exiting the Rx duty-cycle mode, the device stays in the SLEEP state and waits for the next command from the MCU.

3.2 Sleep Timer, Sleep Time

The sleep time has the range from 3 to 134,152,192 ms. The sleep timer is driven by the LPOSC which has $\pm 1\%$ frequency error.

3.3 Rx Timer, Rx Time, Rx Time Ext

The Rx Time is the receive time that has the range from 0.04 to 2,683,043.00 ms. The Rx Time Ext is the extended receive time that has the same range as the Rx Time. It must be configured when Wake-On Radio (WOR) is turned on. The receive timer is driven by the crystal oscillator therefore the timer accuracy is crystal-dependent.

3.4 State After Rx Exit

If Rx Timer is turned on, the device leaves the RX State at the Rx timeout. The parameter tells the device which state it will switch to after leaving the RX State.

3.5 State After Tx Exit

In packet mode, once the device finishes transmitting the packet(s), it automatically exits the Tx state. This parameter tells the

device which state it will switch to after the end of transmission.

3.6 Wake-On Radio, Wake-On Condition

The wake-on radio (WOR) function is an effective power-consumption-saving technique that minimizes the receive time while it guarantees that the device can successfully capture the transmitted data. See the next sections for the details of WOR.

3.7 Application Examples

The following application examples are provided for good understanding of how to control the device operation state, timers and WOR with the external MCU.

3.7.1 Example 1: Sleep Timer Only

Table 4. Sleep Timer Only Configurations

Options	Value	Options	Value
Rx Duty-Cycle Mode	Off	State After Rx Exit	Ignored
Sleep Timer	On	Sleep Time	500 ms
RX Timer	Off	RX Time, RX Time Ext	Ignored, Ignored
Wake-On Radio	Off	Wake-On Condition	Ignored

In this example, the sleep time is set to 500 ms. The RX state entering and exiting is totally under the MCU's control.

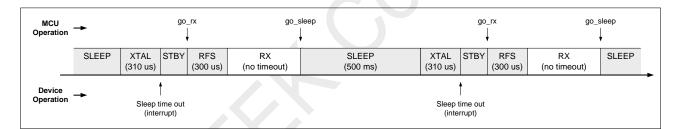


Figure 7. Sleep Timer Only Operation

Once the radio wakes up from SLEEP, it switches to STBY and generates an interrupt to notify the MCU. The MCU issues a 'go_rx' command to switch the radio into the RX state. Before entering the RX state, it takes about 300 us for the device to perform the frequency calibrations.

During the RX state, as usual the MCU uses the different data acquisition mode to obtain the data. The MCU issues a 'go_sleep' command to switch the radio back to SLEEP whenever it wants to.

3.7.2 Example 2: Fixed Duty

Table 5. Fixed Duty Configurations

Options	Value	Options	Value
Rx Duty-Cycle Mode	Off	State After Rx Exit	Ignored
Sleep Timer	On	Sleep Time	500 ms
RX Timer	On	RX Time, RX Time Ext	50 ms, Ignored
Wake-On Radio	Off	Wake-On Condition	Ignored

In this example, the sleep and receive time is set to 500 ms and 50 ms, respectively.

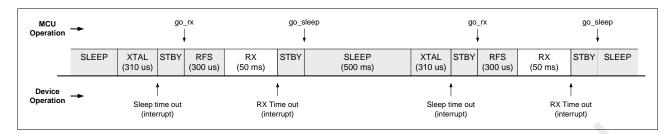


Figure 8. Fixed Duty Operation

Once the radio wakes up from SLEEP, it switches to STBY and generates an interrupt to notify the MCU. The MCU issues a 'go_rx' command to switch the radio to RX state. Before entering the RX state, it takes about 300 us for the device to perform the frequency calibrations.

During the RX state, as usual the MCU uses the different data acquisition mode to obtain the data. Once the radio exits the RX state, it switches to STBY and waits for the MCU's command. At the same time, it generates an 'rx_timeout' interrupt to notify the MCU.

The MCU is able to read the FIFO in the STBY state and during the time of the radio switching state from RX to STBY. However, the FIFO content will be cleared in the SLEEP state.

At the end of the cycle, the MCU issues a 'go_sleep' command to switch the radio back to the SLEEP state.

3.7.3 Example 3: Rx Duty-Cycle Mode

Table 6. Rx Duty-Cycle Mode

Options	Value	Options	Value
Rx Duty-Cycle Mode	On	State After Rx Exit	SLEEP
Sleep Timer	On	Sleep Time	500 ms
RX Timer	On	RX Time, RX Time Ext	10 ms, Ignored
Wake-On Radio	Off	Wake-On Condition	Ignored

If the Rx duty-cycle mode is turned on, it doesn't require control from the external MCU.

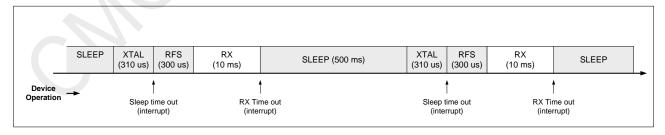


Figure 9. Duty-Cycle Operation

The MCU can use the RX_ACTIVE, SL_TMO and RX_TMO interrupts to observe the device's operational status. In addition, varies packet and FIFO interrupts are available for the data acquisition.

3.7.4 Example 4: Extended by Preamble

Options	Value	Options	Value
Rx Duty-Cycle Mode	Off	State After Rx Exit	Ignored
Sleep Timer	On	Sleep Time	500 ms
RX Timer	On	RX Time, RX Time Ext	10 ms, Ignored
Wake-On Radio	On	Wake-On Condition	2. Extended by Preamble

The wake-on radio function provides a more powerful scheme to save the power. In this example, the receive time is set to 10 ms which is much shorter than the packet length. The sleep time is still set as 500 ms.

When there is no effective signal received, the radio acts like the one introduced in the Example 1. Because the RX Time is much shorter, more power is saved.

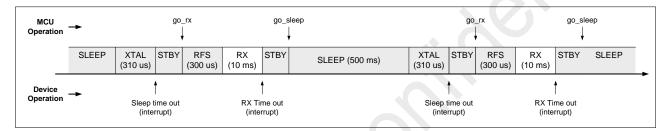


Figure 10. Extended by Preamble without Valid Signal Operation

If a valid preamble is received, the RX state is extended from RX Time to manual control (the RX Timer is off). The extension of the RX state allows the entire packet to be received. The MCU issues a 'go_sleep' command to switch the device back to SLEEP at the end of the cycle.

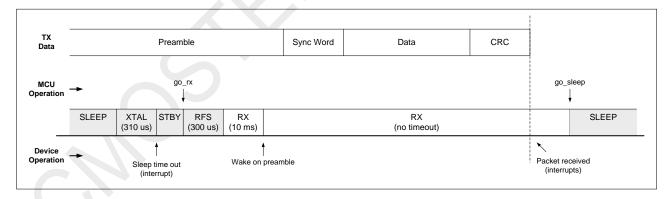


Figure 11. Extended by Preamble with Valid Signal Operation

If the wake-on condition is set to "Extended by RSSI", then the device will extend the RX state while detecting the valid RSSI. In OOK mode, the valid RSSI is the signal strength that is higher than the Auto Squelch threshold. In FSK mode, the valid RSSI is the signal strength that is high than the RSSI Interrupt TH.

If the wake-on condition is set to "Extended by Ext Code", the device will extend the RX state while detecting the 8-bit Extended Code. This will be useful when there is no preamble in the packet.

3.7.5 Example 5: Rx Duty-Cycle Mode + Switched to Rx Ext by Preamble

Table 8. Wake on Preamble Configurations

Options	Value	Options	Value
Rx Duty-Cycle Mode	On	State After Rx Exit	SLEEP
Sleep Timer	On	Sleep Time	500 ms
RX Timer	On	RX Time, RX Time Ext	10 ms, 100 ms
Mala On Dadia	On	Wake-On Condition	5. Switched to Rx Ext by
Wake-On Radio			Preamble

The wake-on radio function provides a more powerful power saving scheme. In this example, the sleep time is still set as 500 ms, the receive time is set to 10 ms, which is much shorter than the packet length.

When there is no effective signal received, the radio acts like the one introduced in the Example 3. Because the RX Time is much shorter, more power is saved.

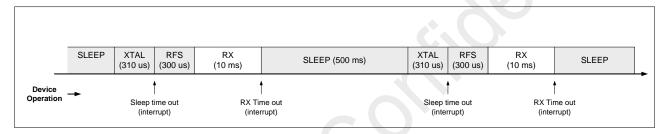


Figure 12. Rx Duty-Cycle Mode + Switched to Rx Ext by Preamble without Valid Signal

If a valid preamble is received, the radio switches from RX state to RX EXT. The RX EXT is just long enough to receive the whole packet.

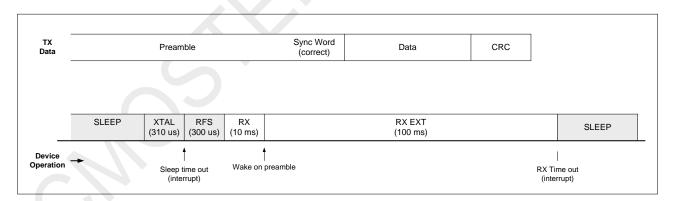


Figure 13. Rx Duty-Cycle Mode + Switched to Rx Ext by Preamble with Valid Signal

After the Rx Ext timeout, the RX_TMO interrupt is generated and the device is automatically switched back to the SLEEP state. The duty-cycle operation will continue. The whole process doesn't need control from the external MCU.

3.7.6 Example 6: Switched to Rx Ext by Preamble, then Extended by Sync Word

Table 9. Switched by Preamble, Extended by Sync Word Configurations

Options	Value	Options	Value
Rx Duty-Cycle Mode	Off	State After Rx Exit	SLEEP
Sleep Timer	On	Sleep Time	500 ms
RX Timer	On	RX Time, RX Time Ext	10 ms, 30 ms
Wala Oa Ba Ka	0.	Well of October 188	7. Extended by Preamble
Wake-On Radio	On	Wake-On Condition	then Sync Word

Comparing to the Example 4, this application scheme saves even more power by providing two stages of RX extension.

When there is no effective signal received, the radio acts as below.

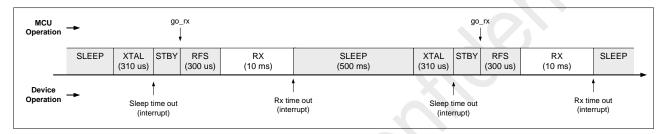


Figure 14. Switched by Preamble, Extended by Sync Word without Valid Signal Operation

If a valid preamble is received, the radio switches from RX state to RX EXT. The RX EXT is just long enough to receive the sync word. Later on, if the sync word validation is failed, the radio switches from RX to SLEEP state on the RX EXT timeout.

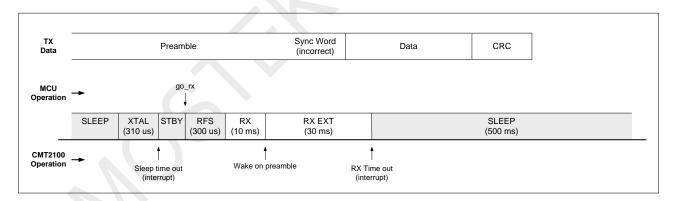


Figure 15. Switched by Preamble, Extended by Sync Word with Invalid Sync Word Operation

If the sync word is valid, the receive time is extended from RX EXT to manual control (when the RX timer is off). The extension of the RX state allows the entire packet to be received. The MCU issues a 'go_sleep' command to switch the device back to SLEEP at the end of the cycle.

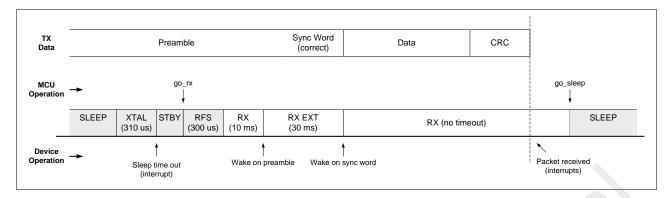


Figure 16. Switched by Preamble, Extended by Sync Word with Valid Sync Word Operation

If the wake-on condition is set to "Switched to Rx Ext by Ext-Code, Extended by Sync", the device will switch to RX EXT period when a valid 8-bit Ext-Code is detected.

3.8 System Clock Output, System Clock Frequency

If the system clock output is enabled on the RFPDK, a continuous clock signal divided down from the 26 MHz crystal clock is available on CLKO pin for driving the external MCU or other devices. The selectable clock frequency has a wide range from 0.406 to 13 MHz. Please note this clock is not available when the device is in the SLEEP and PUP state.

3.9 LBD Threshold

This parameter defines the threshold of the battery low level.

4. OOK Demod Settings



Figure 17. OOK Settings

Table 10. OOK Settings

Parameters	Descriptions	Default	Function
Bandwidth	The receiver bandwidth, the options are: Auto-Select, 50 kHz, 100 kHz, 200 kHz or 500 kHz.	Auto-Select	Rx
Sync Clock	The synchronization clock, the options are: on or off. The clock must be turned on in buffer mode and packet mode. Besides, in direct data transmit/receive mode, if the preamble or sync detection is required, it must be turned on.	On	Rx
Auto Squelch Enable	Turn on/off the auto squelch function. The options are: on or off.	Off	Rx
Auto Squelch	The value of the auto squelch threshold. The range is from 0 to 255.	40	Rx

4.1 Bandwidth

The OOK bandwidth determines the sensitivity of OOK demodulation. The smaller the bandwidth is, the better sensitivity the device has. It is recommended to choose the Auto-Select option which means the RFPDK automatically calculates the bandwidth based on the Data Rate and Xtal Tolerance settings, unless it can't meet the user's application.

4.2 Sync Clock

The synchronization clock is required while the device is configured to work in the buffer mode or packet mode. Also, in direct data transmit and receive mode, if preamble (preamble size is not set to 0) or sync word detection is enabled, it must be turned on. The user must be aware that if sync clock is used, the smaller data rate offset exists between the Tx and Rx, the larger number of consecutive zeros/ones in the packet can exist.

In direct mode, if no preamble and sync needs to be detected, it is recommended to turn off the sync clock.

4.3 Auto Squelch Enable, Auto Squelch

In OOK demodulation, if the Auto Squelch function is enabled, the device is able to mask the noise floor so that the DOUT is quiet while no effective signal is received. The idea is that the device will detect the average level of the noise floor and add up the value of "Auto Squelch" to create a demodulation threshold. Everything below this self-generated threshold is masked out, therefore logical 0 is output to DOUT pin.

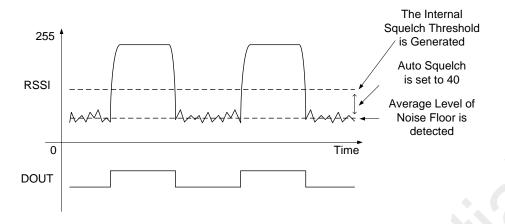


Figure 18. Auto Squelch

It is found that, normally, setting the Auto Squelch to about 30 – 40 will mask more than 95% of the noise. The user should be aware of that, using the Auto Squelch will lead to a few dB lost of sensitivity. The larger value the Auto Squelch is set to, the more sensitivity is lost, because the threshold also masks out a portion of useful signal.

This function is also very useful cooperating with the RSSI related WOR. When the Auto Squelch is properly set, for example, noise is fully masked out, the Rx time switching or extension will not happen. Only when the effective signal (RSSI) is received, the Rx time switching or extension will happen.

5. (G)FSK Settings

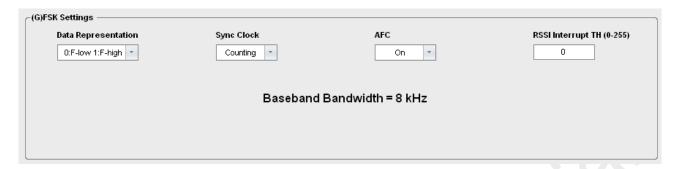


Figure 19.(G)FSK Settings

Table 11. (G)FSK Settings Parameters

Parameters	Descriptions	Default	Function				
	To select whether the frequency "F-high" represent data 0						
Data Representation	or 1. The options are: 0: F-low 1:F-high, or	0: F-low 1:F-high	Rx				
	0: F-high 1:F-low.	igh 1:F-low.					
	This parameter allows the user to select the method to						
Sync Clock	perform the clock data recovery. The options are: Tracing,	Counting	Rx				
	Counting, Manchester or None.						
450	The Automatic Frequency Control. The options are: On or	0	D.				
AFC	Off.	On	Rx				
DCCI Interment TII	The threshold to produce the RSSI_VLD interrupt, the	0	Dv				
RSSI Interrupt TH	range is from 0 to 255.	0	Rx				

5.1 Data Representation

This parameter determines whether the frequency "F-high" modulated frequency represent data 1, or data 0. It should be set according to the transmitter's configurations.

5.2 Sync Clock

The synchronization clock is required while the device is configured to work in the buffer mode or packet mode. Also, in direct data transmit/receive mode, if preamble (preamble size is not set to 0) or sync word detection is enabled, it must be turned on. The user must be aware that if sync clock is used, the smaller data rate offset exists between the Tx and Rx, the larger number of consecutive zeros/ones in the packet can exist.

The optional types of the sync clock are: Tracing, Counting and Manchester, which will be introduced respectively as below.

5.2.1 Tracing

The tracing method acts like a digital PLL. It takes a few symbols for the sync clock generator to trace the TX data rate and eventually lock to it. This is the default clock synchronization method option. Under this method, the receiver allows 10 - 15 symbols of the consecutive "0" or "1" to be correctly sampled, while tolerating $\pm 8\%$ of data rate error at most.

5.2.2 Counting

The counting method has the advantage of tolerating as large as ±30% (for GFSK/FSK demodulation) or ±25% (for OOK

demodulation) data rate error, while it has a drawback of requiring frequent data transitions to adjust the sync clock rate. If there is no data transition happening within 3 - 4 symbols or the data rate error is significantly large, the clock recovery and data capturing will start to go wrong.

Comparing to the Tracing method, the Counting method is more suited for the application where data to be transmitted is properly coded but the data rate can't be precisely controlled.

Even though the CMT2300A providing ways to deal with both data rate error and no data transition problem, it is always recommended for the user to avoid transmitting long string of "0" by encoding the data using the Manchester, data-whitening or similar encoding techniques.

5.2.3 Manchester

This sync clock method is particularly designed for synchronizing the clock from the Manchester encoded data, i.e. no more than two consecutive zeros/ones. It can only be used when the entire packet is encoded in Manchester format, including the preamble and the sync word. The advantage is that it has better performance of tolerating sudden change of data rate than the counting and tracing method.

The device does not encode/decode the sync word in Manchester format. The user must ensure that the sync word is encoded in Manchester format if this sync clock method is used.

5.3 AFC

The Automatic Frequency Control (AFC) is useful to minimize the RF frequency offset between the transmitter and the receiver. The AFC ensures the highest receiving performance by removing the frequency error prior to narrowing the baseband bandwidth.

The AFC is triggered once the device gets into the RX state. After the valid signal comes, it takes 4-8 symbols of time to remove most of the frequency error. It is recommended to transmit at least another 8-symbol of preamble than the preamble size defined on the RFPDK, to ensure the AFC can be done during the reception of the preamble, so that the sensitivity can be enhanced for the subsequent sync word and payload receiving.

5.4 RSSI Interrupt TH

This threshold is used to generate the RSSI_VLD interrupt in FSK demodulation. When the RSSI is higher than the threshold, the interrupt will be generated. This interrupt is also used to switch or extend the Rx time when the RSSI related WOR is used.

6. Encode/Decode Settings

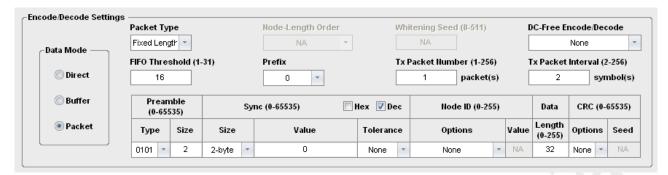


Figure 20.Encode/Decode Settings

The available options of Data Mode are shown in the table below.

Table 12. Decode Settings Parameter

Parameter	Descriptions	Default	Function
Data Mode	The data acquisition mode, the options are: Direct, Buffer or Packet. Table 14, Table 15 and Table 16 will show the available parameters for each data mode.	Packet	TRx

The table below shows the digital pins used to connect to the external MCU. The selection of the pin functions are not done on the RFPDK, instead, it is done by writing the control registers in the external MCU program. The subsequent sections will explain the behavior of the device according to Table 13.

Table 13. Digital Pin Functions

Pin	Name	I/O	Functions
14	CSB	ı	4-wire SPI chip register select input.
15	SDA	Ю	4-wire SPI data input and output.
16	SCL	1	4-wire SPI clock input.
1	FCSB	-	4-wire SPI chip FIFO select input, active low. Internally pulled high, leave floating when programming the EEPROM.
2	GPIO3	0	Programmable output, options are: CLKO (default), INT1, INT2 and DCLK.
5	GPIO2	10	Programmable input and output, options are: INT1 (default), INT2, DCLK or DOUT/DIN
6	GPIO1	IO	Programmable input and output, options are: DOUT(default)/DIN, INT1, INT2 or DCLK.

6.1 Direct Mode

In Rx mode, the data from the demodulator's output can be directly captured by the MCU on the DOUT. The synchronization clock is output on the DCLK if it is configured. In Tx mode, the data to be transmitted can be directly sent into the device on the DIN. No synchronization clock is required.

The optional preamble and sync word is supported, as shown in the table below.

Table 14. Configurable Parameters in Direct Mode

Parameter	Descriptions	Default	Function
Preamble Type	The pattern of the preamble, the options are: 0101 or 1010.	0101	TRx
	The size of the valid preamble, the range is from 0 to 65535		
Preamble Size	bytes. When setting to 0 means no preamble is transmitted by	2	TRx
	the transmitter or detected by the receiver.		
Cura Ciaa	The size of the Sync Word, the options are: None, 1-byte,	O huda	TRx
Sync Size	2-byte, 3-byte, 4-byte, 5-byte, 6-byte, 7-byte or 8-byte.	2-byte	IRX
Sync Value	The value of the Sync Word, the range is from 0 to 2 ^{Sync_Size} -1.	0	TRx
	The number of bits tolerated for the Sync Word recognition. The		
Sync Tolerance	options are: None, 1 Error, 2 Errors, 3 Errors, 4 Errors, 5 Errors,	None	Rx
	6 Errors or 7 Errors.		

6.1.1 Preamble

The preamble detection is optional in direct mode. In Rx mode, the preamble is usually used as the wake-on condition.

6.1.2 Sync Word

The sync word detection is optional in direct mode. The sync word is defined by the parameters of Sync Size and Sync Value. In Rx mode, a successful detection of a sync word generates an active-high interrupt that can be assigned to INT1 or INT2. The external MCU use this information to filter the received data. For example, if the Sync Tolerance is set to 2 Errors, it means that a valid sync word is received when less or equal to 2 bits of error in the sync word.

6.1.3 Application Information

The figure below shows the data path from the MODEM to the I/Os in the direct mode.

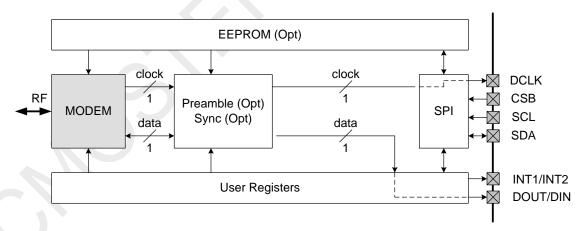


Figure 21. Data Path of Direct Mode

Rx Processing

In direct mode, the data coming from the demodulator is directly sent to the MCU via the DOUT. The synchronization clock is output via the DCLK. The DOUT and DCLK should be mapped to different GPIOs. The optional preamble and sync word detection interrupts are supported upon requirements.

The data receiving works independently of the preamble and sync word detection in the direct mode. This means, no matter

whether a valid preamble or a sync word is detected or not, the demodulated data will be transparently output on the DOUT.

The sync clock is generated with two purposes: removing the glitches exist on the data output, and assisting the external MCU to sample the data at the correct instance.

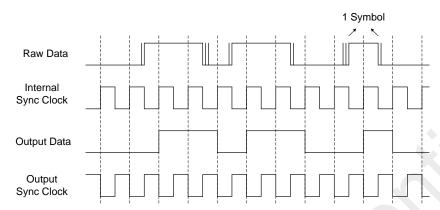


Figure 22. Demodulated Data and Sync Clock Timing Characteristics

In the figure above, the raw data is the output of the demodulator. When the SNR of the incoming signal is very low, glitches possibly exist on the raw data. The device will remove those glitches by internally sampling the raw data using the recovered clock. The clean data is output to the DOUT. The sync clock is delayed by half cycle and output to the DCLK. The rising edge of the output sync clock is centered on the output data. If the sync clock is turned off, the raw data will be directly output to the DOUT.

The MCU should do the following things to receive the data in the direct mode:

- 1. Setup the GPIOs using the IO_SEL control register.
- 2. Issue the go_rx command.
- 3. Continuously capture the received data on DOUT.
- 4. Issue go_sleep/go_stby/go_rfs command to exit receiving.

Tx Processing

In direct mode, the data to be transmitted is directly sent from the MCU into the device via the DIN pin. Any data rate, which is determined by the MCU, within the device specification can be used, with the exception that, when the GFSK is selected as the modulation scheme, where the actual data rate must have less than \pm 7% offset of the data rate configured on the RFPDK. No external clock for synchronization is required.

Preamble and sync detection is not supported.

The MCU should do the following things to transmit the data in the direct mode:

- 1. Set the control register bit TX_DIN_EN to 1.
- 2. Set the control register bit TX_DIN_SEL to 0 to use GPIO1 as DIN, or 1 to use GPIO2 as DIN.
- 3. Drive DIN to either logic 0 or 1.
- 4. Issue the go_tx command, the device starts transmitting the data on DIN, now the logic 0/1 is transmitted.
- 5. Continuously send in the data on DIN, the data is transmitted immediately.
- 6. Set TX_STOP bit to 1.
- 7. Issue go_sleep/go_stby/go_rfs command to exit the transmitting.

6.2 Buffer Mode

In Rx mode, the data coming from the demodulator is shifted into the FIFO. The sync clock recovery is always enabled. The MCU can use the 4-wire SPI to read the FIFO. The FIFO will retain its content to be readable in the STBY, RFS and RX state.

In Tx mode, the FIFO is used to store the data to be transmitted.

By using the FIFO_MERGE bit in the control register, the user can choose whether to use a 32-byte FIFO dedicated to Rx mode and another 32-byte FIFO dedicated to Tx mode, or a single 64-byte FIFO for either Tx or Rx mode by means of merging the two 32-byte FIFO into one.

The optional preamble is supported. The sync word detection is also required, as shown in the table below.

Table 15. Configurable Parameters in Buffer Mode

Parameter	Descriptions	Default	Function
Preamble Type	The pattern of the preamble, the options are: 0101 or 1010.	0101	TRx
Preamble Size	The size of the valid preamble, the range is from 0 to 65535 bytes. When setting to 0 means no preamble is transmitted by the transmitter or detected by the receiver.	2	TRx
Sync Size	The size of the Sync Word, the options are: 1-byte, 2-byte, 3-byte, 4-byte, 5-byte, 6-byte, 7-byte or 8-byte.	2-byte	TRx
Sync Value	The value of the Sync Word, the range is from 0 to 2 ^{Sync_Size} -1.	0	TRx
Sync Tolerance	The number of bits tolerated for the Sync Word recognition. The options are: None, 1 Error, 2 Errors, 3 Errors, 4 Errors, 5 Errors, 6 Errors or 7 Errors.	None	TRx
FIFO Threshold	This defines the FIFO threshold that once it is reached, an interrupt is generated to notify the external MCU. The range is: 1. From 1 to 32 when FIFO_MERGE = 0, 2. From 1 to 64 when FIFO_MERGE = 1.	16	TRx
Prefix	This defines whether the transmitter sends out 0/1/preamble before sending out the packet.	0	Тх

6.2.1 Preamble

The preamble detection is optional in buffer mode. In Rx mode, the preamble is usually used as the wake-on condition. The preamble will not be shifted into the FIFO, it will be taken off after the chip has detected it.

6.2.2 Sync Word

The sync word detection must be enabled in buffer mode. The sync word is defined by the parameters of Sync Size and Sync Value. A successful detection of a sync word generates an active-high interrupt that can be assigned to INT1 or INT2. The received data will be shifted into the FIFO only if a valid sync word is detected. It should be noted, if the Sync Tolerance is set to 2 Errors, it means that less or equal to 2 bits of error in the sync word does not stop the subsequence data reception.

6.2.3 FIFO Threshold

This parameter allows the user to choose how many bytes of unread/unsent data will set the FIFO_TH interrupt to high. For example, if it is set to 16, it means when the unread/unsent data in the FIFO is equal to or more than 16 bytes, the FIFO_TH interrupt stays high. This threshold takes effect in both of the Tx and Rx mode.

6.2.4 Application Information

The figure below shows the data path from the demodulator to the I/Os in the buffer mode.

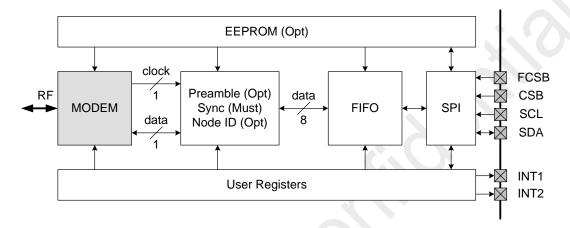


Figure 23. Data Path of Buffer Mode

Rx Processing

In buffer mode, the data coming from the demodulator output are shifted into the FIFO after a valid sync word is detected. The MCU use the 4-wire SPI to read the FIFO. The FIFO will retain its content to be readable in the STBY, RFS and RX state. The MCU can use the FIFO interrupts to assist to the FIFO reading. The optional preamble detection is supported. The Sync Clock must be set to Counting, Tracing or Manchester in buffer mode.

Since the chip does the data buffering work automatically, the MCU can spend time on other tasks during the data buffering process. Therefore, the MCU's performance requirement is greatly reduced in terms of speed and reactivity.

The data receiving is independent of the preamble detection. This means, no matter whether a valid preamble is detected or not, the subsequent sync word detection and FIFO filling will be performed.

The sync word detection is compulsory in the buffer mode. The demodulated data will be shifted into the FIFO while a valid sync word is detected. Once the sync word is detected, the FIFO will still be continuously filled with noise or data as long as it is not full, until that the MCU sets the FIFO _CLR bit in the user register FIFO_CTL. After the FIFO is cleared, the device is able to detect the next incoming sync word again. Moreover, the FIFO_CLR bit clear the current status of the packet handler.

Five interrupts are provided to assist the FIFO reading. Please refer to the user register FIFO_FLG in CMT2300A datasheet for the details. The interrupts timing characterizes are shown in the figure below.

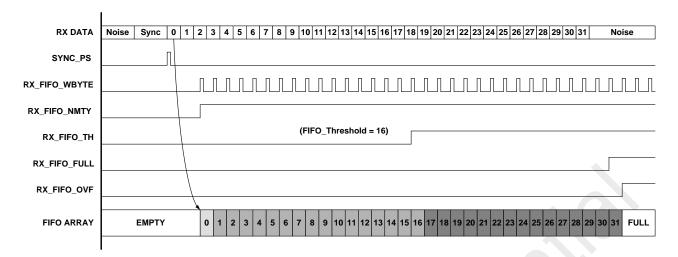


Figure 24. RX FIFO Interrupts Timing Characteristics

Below list a few ways to use the FIFO interrupts:

- RX_FIFO_WBYTE: The MCU reads the FIFO once the RX_FIFO_WBYTE goes high, as long as the MCU processing speed is fast enough, byte 0 will always be read out before byte 1 is filled. This is the fastest way to read out the FIFO content.
- RX_FIFO_NMTY: This is the FIFO "Not Empty" interrupt. The MCU starts to read the FIFO once the RX_FIFO_NMTY interrupt goes high. This interrupt will be cleared automatically once the FIFO is found empty.
- RX_FIFO_TH: The "FIFO_Threshold" parameter allows the user to configure how many bytes of unread data will set the RX_FIFO_TH interrupt to high. The MCU starts reading the data once the RX_FIFO_TH goes high. This interrupt will be cleared automatically once it is found that the number of unread data bytes is less than the threshold.
- RX_FIFO_FULL: The MCU starts reading the FIFO once the RX_FIFO_FULL goes high. This interrupt will be cleared automatically once the FIFO is found not full. This is the easiest and slowest way to read out the content of the FIFO.
- RX_FIFO_OVF: The RX_FIFO_OVF reflects that the FIFO overflows. Once the FIFO overflows the incoming data cannot
 be shifted into the FIFO and therefore they will be lost. This interrupt will be cleared automatically once it is found that the
 FIFO does not overflow.

The user should consider the FIFO filling and reading speed to decide which FIFO interrupt is the most suitable one in the system. The speed of filling the FIFO is the data rate divided by 8. The speed of reading the FIFO is determined by the MCU and the SPI interface speed.

Application Flow Example:

- Setup the GPIOs using the IO_SEL control register.
- Setup the interrupts using the INT1_CTL and INT2_CTL registers.
- Issue the go_rx command.
- Read the FIFO according to the chosen interrupt status.
- Issue go_sleep/go_stby/go_rfs command to save power.

Tx Processing

In buffer mode, the MCU can preload the data into the FIFO in the STBY/TFS state, or write the FIFO in the TX state while the

data is being transmitted, or combine these two methods by preloading part of the payload into the FIFO in the STBY/TFS state, then fill the rest of them in the TX state during the transmission.

The device can produce the TX_FIFO_FULL, TX_FIFO_NMTY and TX_FIFO_TH interrupts to let MCU know about the FIFO's status. These interrupts have the same definition of those of RX FIFO.

The MCU should do the following to transmit the data in the buffer mode:

- Setup the GPIOs using the IO_SEL control register.
- Issue the go_stby/go_tfs command if any data must be preloaded into the FIFO.
- Issue the go_tx command.
- Write data (if any) into the FIFO according to the chosen interrupt status.
- Issue the tx_stop command.
- Issue go_sleep/go_stby/go_rfs command to save power.

6.3 Packet Mode

In packet mode, a hardware packet handler is available to perform data packing/depacking and encoding/decoding. The data filling or receiving is done through the FIFO.

The available options of data decoding in the packet mode are listed in the table below.

Table 16. Configurable Parameters in Packet Mode

Parameter	Descriptions	Default	Function				
Packet Type	The device supports two packet types. The options are: Fixed Length or Variable Length.	Fixed Length	TRx				
Node-Length Order	This parameter defines in variable length packet, the node ID is placed in before or after the length byte. The options are: First Node, then Length, or First Length, then Node.	First Node, then Length	TRx				
Whitening Seed	The initial seed for the data whitening polynomial. This parameter is only available when DC-Free Encode/Decode is set to "Whitening". The range is from 0 to 511.	511	TRx				
DC-Free Encode/Decode	DC-Free The options of DC-free data encoding/decoding are None, Manchester 1 (01=one, 10=zero), Manchester 2 (10= one,						
FIFO Threshold	This defines the FIFO threshold that once it is reached, an interrupt is generated to notify the external MCU. The range is: From 1 to 32 when FIFO_MERGE = 0; From 1 to 64 when FIFO_MERGE = 1.	TRx					
Prefix	This defines whether transmitting 0, 1 or preamble before the useful data start to transmit.	0	Тх				
Tx Packet Number	This defines the number of packets to be transmitted in one transmission cycle. The range is from 1 – 256 packet(s)	1 packet	Тх				
Tx Packet Interval	This defines the packet interval if more than 1 packet is transmitted in one transmission cycle. The range is 2 – 256 symbols.	2 symbols	Tx				
Preamble Type	The pattern of the preamble, the options are: 0101 or 1010	0101	TRx				
Preamble Size	The size of the valid preamble, the range is from 0 to 65535 bytes. When setting to 0 means no preamble is transmitted by the transmitter or detected by the receiver.	2	TRx				

Parameter	Descriptions	Default	Function
Sync Size	The size of the Sync Word, the options are: None, 1-byte, 2-byte, 3-byte, 4-byte, 5-byte, 6-byte, 7-byte or 8-byte.	TRx	
Sync Value	The value of the Sync Word, the range is from 0 to 2 ^{Sync_Size} –1.	0	TRx
Sync Tolerance	The number of bits tolerated for the Sync Word recognition. The options are: None, 1 Error, 2 Errors, 3 Errors, 4 Errors, 5 Errors, 6 Errors or 7 Errors.	None	TRx
Node ID Options	The options for the Node ID detection are: None, Detect Node ID, Detect Node ID and 0x00, or Detect Node ID, 0x00 and 0xFF.	None	TRx
Node ID Value	This parameter is only available when the Node ID Options is not set to "None". It defines the value of the Node ID. The range is from 0 to 255.	NA	TRx
Data Length	This defines the number of bytes of data in a fixed length packet. The range is from 0 to 255.	32	TRx
CRC Options	The options for the CRC polynomial are: None, CCITT or IBM.	None	TRx
CRC Seed	This parameter is only available when CRC Options is not set to "None". It defines the initial seed for the CRC polynomial. The range is from 0 to 65535.	0	TRx

6.3.1 Packet Type

The device supports two packet types: Fixed length and Variable length.

Fixed Length Packet

The fixed length means that the payload length is configured into the device and will not be changed during the transmission. The RX and TX shall have the same payload length in this case. The payload contains the optional Node ID and the Data. The maximum payload length is 256 bytes, which is not limited to the FIFO size.

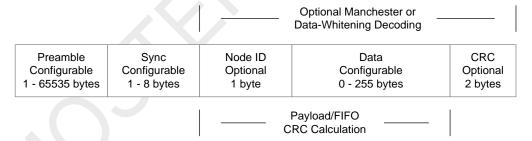


Figure 25. Fixed Length Packet Structure

The sync word detection is compulsory in the packet mode. The size of preamble, sync word and payload (Node ID + Data) are all configurable. The Node ID can be disabled by setting the "Node ID Option" to "None". Only the optional Node ID and the Data will be shifted into the FIFO once the sync word is detected.

Variable Length Packet

The variable length means that the payload length can vary in different packets. In this case, an additional "Length" byte is given as the part of the payload to indicate the payload length of the current packet. The maximum payload length can be indicated by the Length byte is 255, because the Length byte itself is not included in the calculation. For example, if the Length byte indicates that the payload is 255 bytes, and the Node ID is supported, it means that there will be 1 byte of Node ID and 254 bytes of Data incoming.

While the payload length is larger than the FIFO size, it requires the external MCU to read out the FIFO content during the receiving before it is full.

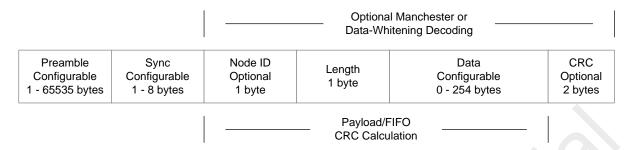


Figure 26. Variable Length Packet Structure

The FIFO filling and reading mechanism is identical to the buffer mode. The FIFO starts being filled once the sync word and optional node ID validation is successful. The CRC validation failure does not clear the FIFO. The state changing from RX to STBY/RFS does not disturb the FIFO reading.

6.3.2 Node-Length Order

In variable packet, the Node ID can be placed before or after the Length Byte.

6.3.3 FIFO Threshold

This parameter allows the user to choose how many bytes of unread data will set the FIFO_TH interrupt to high. For example, if it is set to 16, it means when the unread data in the FIFO is equal to or more than 16 bytes, the FIFO_TH interrupt stays high. This takes effect in both of the Tx and Rx mode.

6.3.4 Prefix

After getting into the TX state, the device will start the transmission once it is found that the FIFO is not empty. If the MCU has not fill any data into the FIFO when the device is in the TX state, the device can transmit data 0, 1 or the same pattern of preamble until the FIFO is filled, which can be selected on the RFPDK by the Prefix parameter.

6.3.5 Tx Packet Number, Tx Packet Interval

The device can continuously transmit a number of packets with the same payload in the TX state. This parameter defines how many packets are transmitted. This saves the time and effort of the MCU to repeatedly fill the same set of data into the FIFO. The time gap of these packets is defined by the parameter Tx Packet Interval. The time unit is symbol. The minimum packet interval is 2 symbols.

6.3.6 Preamble

The preamble detection is optional in packet mode. In Rx mode, the preamble is usually used as the wake-on condition. The preamble will not be shifted into the FIFO, it will be taken off after the chip has detected it.

6.3.7 Sync Word

The sync word detection is optional in packet mode. The sync word is defined by the parameters of Sync Size and Sync Value. A successful detection of a sync word generates an active-high interrupt that can be assigned to INT1 or INT2. The user can introduce some tolerance of the sync word filtering. For example, if the Sync Tolerance is set to 2 Errors, it means that less or

equal to 2 bits of error in the sync word does not stop the subsequence data reception.

6.3.8 Node ID

The Node ID detection is an option in packet mode. The Node ID is defined by the parameters of Node ID Value and Node ID Options. A successful detection of a node ID generates an active-high interrupt that can be assigned to INT1 or INT2. Beside the sync word detection, the Node ID allows the user to further filter the incoming data. The parameter of "Node ID Options" provides 4 options for the Node ID filtering as shown below.

- None: The Node ID filtering is not supported.
- Detect node ID: The node ID filtering is supported. Only after the chip has detected a node ID and it matches the value set in the parameter Node ID, it will continue to process the packet.
- Detect node ID, 0x00: The Node ID filtering is supported. Only after the chip has detect a node ID ant it either equals to 0x00 or matches the value set in the parameter Node ID, it will continue to process the packet.
- Detect Node ID, 0x00, 0xFF: The Node ID filtering is supported. Only after the chip has detected a node ID ant it either equals to 0xFF or matches the value set in the parameter Node ID, it will continue to process the packet.

6.3.9 CRC Checksum

The CRC validation is optional in the packet mode. The 'CRC Type' parameter is used to select the two types of CRC the device supported: CCITT or IBM.

The CCITT CRC polynomial is: $X^{16} + X^{12} + X^5 + 1$

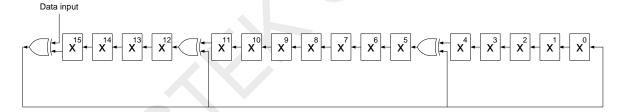


Figure 27. CCITT CRC Structure

The IBM CRC polynomial is: $X^{16} + X^{15} + X^2 + 1$

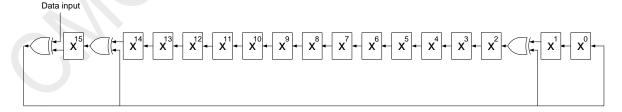


Figure 28. IBM CRC Structure

The 'CRC Seed' parameter defines the initial seed of both of the 2 polynomials.

The chip compares the checksum to the 2-byte CRC in the packet. If they are identical, it means that the payload has been received correctly and the CRC_PS interrupt will be asserted. If the CRC check fails, the payload is stilled filled into the FIFO and

the PKT_DONE interrupt will be asserted. But the CRC_PS interrupt and the corresponding register flag will not generate.

6.3.10 DC-Free Encode/Decode

Two DC-Free encode/decode techniques are supported: Manchester and Whitening. They are only supported in Packet Mode.

Manchester

The chip can decode the payload and CRC which has been converted into the Manchester code by the transmitter. This function is only available in the Packet Mode. The RFPDK allows the user to select 2 types of conventional Manchester Decoding. For Manchester 1, logic 1 is converted to "01" and logic 0 is converted to "10".

Table 17. Encode/Decode Using Manchester 1 Method

	Preamble				Sync Word				Payload & CRC								
Encoded Data	1	0	1	0		0	1	1	0		0	1	1	0	0	1	
Decoded Data	1	0	1	0		0	1	1	0			1	()		1	

For Manchester 2, logic 1 is converted to "10" and logic 0 is converted to "01".

Table 18. Encode/Decode Using Manchester 2 Method

		Pı	eamb	le		Sy	nc Wo	ord		•		Paylo	oad &	CRC		
Encoded Data	1	0	1	0	 0	0 1 1 0				0	1	1	0	0	1	
Decoded Data	1	0	1	0	 0	1	1	0		(0 1		()		

The receiver converts the encoded data back to the NRZ data. After the decoding, the payload will be filled into the FIFO. Therefore, the MCU won't need to do the Manchester decoding.

Whitening

The device can decode the payload and CRC which have been whitening encoded by the transmitter. The whitening or de-whitening process is that the input data XOR with a specific polynomial, which produces a pseudo-random sequence. The advantage of whitening compare to the Manchester coding is that it does not reduce the actual data rate into a half, so that it saves the power after all. The de-whitening process is transparent to the MCU. The whitening and the de-whitening shares the same polynomial.

Whitening/De-Whitening polynomial: $X^9 + X^5 + 1$

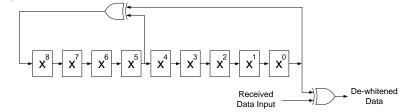


Figure 29. Whitening/De-Whitening Algorithm Structure

The parameter Whitening Seed allows the user to define the 9-bit initial seed for the polynomial. The seeds on the Tx and the Rx must be identical.

6.3.11 Application Information

The figure below shows the data path from the demodulator to the I/Os in the packet mode.

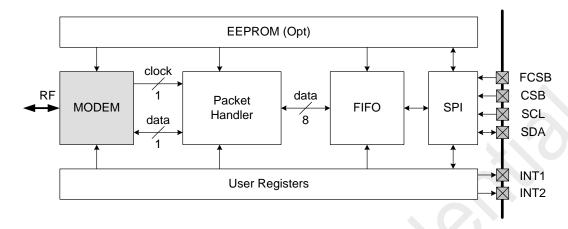


Figure 30. Data Path of Packet Mode

Rx Processing

In packet mode, the received data are obtained by reading the FIFO, which is similar to in the buffer mode. The FIFO will retain its content in the STBY, RFS and RX state. The MCU use the FIFO interrupts to assist the FIFO reading. The packet handler provides various functions to decode and validate the incoming data. This can further reduce the work load and user program size of the MCU. The FIFO_CLR bit clears the current status of the packet handler and the FIFO pointers. The RSSI valid, preamble, sync word, node ID, packet done and CRC interrupt clearing can be done by setting the related bit in the INT_CLR register, but they do not take effect in the SLEEP state.

The MCU should do the following to receive the data in the packet mode:

- Setup the GPIOs using the IO_SEL control register.
- Setup the interrupts using the INT1_CTL, INT2_CTL and INT_EN registers.
- Issue the go_rx command.
- Read the FIFO according to the chosen interrupt status.
- Issue go_sleep/go_stby/go_rfs command to save power.
- Clear the packet interrupt status using the INT_CLR register.

Tx Processing

Similar to what is in the buffer mode, in packet mode, the MCU can preload the data into the FIFO in the STBY/TFS state, or write in the FIFO in the TX state while the data is being transmitted, or combine these two methods by preloading part of the payload into the FIFO in the STBY/TFS state, then fill the rest of them in the TX state during the transmission.

Once gets into the TX state, the device firstly detects if the FIFO is empty. If the FIFO is not empty, it immediately transmits the optional packet components in front of the payload, i.e. preamble, sync, node ID and length. If the FIFO is empty, it transmits one of the 3 prefix options which is set as parameter TX Prefix on the RFPDK, until the first byte of payload is filled into the FIFO. After all the payload is sent, the device adds the optional 2-byte CRC at the end of the packet.

The MCU operation flow is similar to that of the buffer mode, but does not need to issue the tx_stop command at the end of the transmission, because the device knows when to end the transmission by getting the information from the payload length or the length byte.

7. Document Change List

Table 19. Document Change List

Rev. No.	Chapter	Description of Changes	Date
0.6	All	Initial released version.	2015-08-06

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