# Homework 6

**Total Points: 100**

**Firm deadline:** Submit the XLSX file by the end of Sunday, 4/9/2023.

An Excel file is provided. Put answers in the file and submit it. The file has multiple sheets. Pay attention to the sheet names. Do not add or remove cells in the files.

## 1 Processor pipeline.

We study how a 5-stage pipeline executes instructions in detail, using an example from an online chapter of the textbook. We can download the entire chapter from the publisher via a link provided in slides. We also provide a shortened version in HuskyCT. In the shortened version, we also corrected errors in Figures e4.14.11 to e4.14.14, where PC should be saved in IF/ID.

The pipeline in Figures e4.14.11 to e4.14.14 does not handle hazards. We assume hazards are removed in software.

We study how the pipeline executes the five instructions at the bottom of page 365.e15. The page numbers are at the top corners of a page in the PDF file. In addition to the five instructions from the PDF file, we also provided additional instructions before and after them in file "`hw6.1.s`", so we know the signal values when the instructions are executed.

The task is to find out the signal values in the pipeline when LW instruction is in the WB stage (cycle 5 as in Figure e4.14.13 on page 365.e23) and in cycle 6. The signals are listed in the spreadsheet. Note that there are two sheets, one for cycle 5 and one for cycle 6.

Here are requirements/tips/clarification, which are continued on the next page.

- We only need to find out the value of signals listed in the spreadsheet. The signals roughly follow their order in the figures, from top to bottom, in each stage. Signals in light blue shaded cells are stored in pipeline registers. In ID and IF, we also have signals from later stages in the same cycle. Those signals are in dark red. Not all signals are labeled in the figures. We can locate the signals in the single-cycle processor diagram.
- The signal values are the values near the end of the cycles, when signals are stable.
- Write register numbers in decimal. Write 32-bit values in hexadecimal. Add "0b" before multiple bits, e.g., the value of ALUop. Do NOT add “0b” for single-bit signals.
- Many signals have their values marked in the figures in the PDF.
- For PC, instruction, and data read from registers or memory, we can find their values by assembling and running `hw6.1.s` in RARS.

- In this question, we do not assume how ImmGen sets output for R-type instructions. So the output of ImmGen is "X" for R-type instructions. The branch target is "X" if the immediate is "X". Otherwise, it needs to be computed.
- If MemRead is 0, Read Data (from the data memory) is "X".

## 2 Hazards on a Processor without Forwarding.

Assume we use a RISC-V processor with a 5-stage pipeline that does **NOT** have any forwarding paths. The processor detects data hazards and stalls if needed.

Complete the pipeline diagram for the instruction sequences in the spreadsheet. Submit the spreadsheet in HuskyCT.

## 3 Hazards on a Processor with Forwarding.

Assume we use a RISC-V processor with a 5-stage pipeline that has all necessary forwarding paths. The processor detects data hazards and stalls if needed.

Complete the pipeline diagram for the instruction sequences in the spreadsheet. In addition, show the forwarding path (`EX/MEM->EX`, `MEM/WB->EX`, `MEM/WB->MEM`, or `EX/MEM->ID`), if any, used to obtain registers rs1 and rs2 in an instruction. Leave the cell blank if the register value is not forwarded. Submit the spreadsheet in HuskyCT.