Saber Ganjisaffar

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Education

Ph.D. Student in Computer Science - University of California, Riverside (UCR) *California, US*

Current GPA: 3.62/4 *09/2022 - 09/2027 (Expected)*

Thesis: Microarchitectural Support for Heterogenous Systems Security and Memory Safety

M.S. in Computer Systems Architecture - Shahid Beheshti University *Tehran, Iran*

GPA: 3.77/4 *2018 - 2021*

Thesis: A Novel Hardware Cache Coherence Mechanism for GPU-Based Near Memory Architectures

B.S. in Computer Science - Semnan University *Semnan, Iran*

Last Two Years GPA: 3.42/4 *2012 - 2017*

Project: Congestion Management and Simulation for Network on Chip (NoC) Systems

Research Interests

Computer Architecture and Microarchitecture Design
Heterogeneous System Architectures, including GPU and Specialized Accelerators
Microarchitectural Support for Security
Memory Safety and Reliability Enhancements
Simulation Frameworks for Architecture/Microarchitecture Modeling

Projects

Extending Gem5 Simulator with ARM Memory Tagging Extension (MTE) Support *2023-Present*

Gem5

- ARM's Memory Tagging Extension (MTE) is an new hardware feature designed to enhance memory safety through an efficient hardware-based mechanism called memory tagging. I am currently developing an ISA extension and microarchitectural modifications to the Gem5 simulator to fully support ARM's MTE instructions. This work involves implementing a comprehensive set of instructions for memory tagging, which integrates seamlessly with software tools like the LLVM MemTagSanitizer and the hardened memory allocators such as Scudo. By extending Gem5 in this way, this project aims to provide a valuable platform for future research and testing of ARM's MTE, advancing memory safety techniques in hardware.

A Simulator for Architectures Leveraging GPU Cores for Near-Memory Processing *2021-2022*

Accel-Sim (GPGPU-Sim v4.0), DRAMSim3

- During my research on Near-Memory Processing (NMP) architectures utilizing GPU cores as processing units, I identified a gap in available simulation tools for this type of architecture. My goal was to model a heterogeneous system, with a primary GPU on one side and smaller GPU cores integrated into the main memory, such as a 3D-stacked memory like HBM, on the other side. To achieve this, I integrated GPGPU-Sim to simulate the GPU cores and DRAMSim3 to model the 3D-stacked memory system.

MGPUSim Support for Near-Memory Processing *2020-2021*

MGPUSim (Akita Simulation Engine)

- I implemented a novel cache coherence mechanism for near-memory processing architectures leveraging GPU cores as part of my thesis. To achieve this, I utilized MGPUSim, a high-performance single/multi-GPU simulator known for its fast execution through concurrent processing. The simulator's hierarchical and modular design enabled me to effectively implement and modify the architecture to test and validate the proposed cache coherence mechanism.

Design of a Genetic Algorithm Processor *2019*

Verilog, Xilinx Vivado, Modelsim

- Due to the heavy computational load of genetic algorithms, they usually take a long time to find the optimum solution. I designed a fast, pipelined, and efficient, Genetic Algorithm Processor(GAP) that can find the optimum solution based on a fitness function defined. I adopted some of the best practices and research ideas at that time for designing this processor. As it is general-purpose and modular, one can easily use it for any fitness function.

Traffic and Congestion Simulator for Complex Network on Chip (NoC) Modeling *2018*

Python, NetworkX

- Designed and developed a Network-on-Chip (NoC) simulator to model congestion behavior in complex and arbitrary NoC architectures. The simulator allows for the introduction of various traffic patterns and enables dynamic monitoring of network traffic and congestion. I utilized Python and the NetworkX library to construct the network topology based on configuration files and simulate the real-time traffic flow and congestion dynamics within the system.

Technical Skills

Languages and Frameworks: C/C++, Golang, Python, Assembly, Verilog, SystemC, TensorFlow

Multicore and Parallel Programming: CUDA, OpenCL, OpenMP

Tools and Technologies: Linux, Bash, Git/Github, Xilinx Vivado, Intel Quartus Prime, Intel HLS, ModelSim, LaTex

Architectural Simulators: Accel-Sim (GPGPU-Sim), MGPUSim, Vortex GPGPU, Gem5, DRAMSim3, Ramulator, Verilator, CACTI

Publications

S. Ganjisaffar, E. Mohammadian Koruyeh, J. Zellmer, H. Asghari-Esfeden, C. Song, N. Abu-Ghazaleh. *ISCA 2025*

SpecASan: Mitigating Transient Execution Attacks Using Speculative Address Sanitization.

https://doi.org/10.1145/3695053.3731119 *20 June 2025*

Experience

Teaching Assistant, CS 153 - Design of Operating Systems

University of California, Riverside *Fall 2024, Summer 2024*

Teaching Assistant, CS 010A - Introduction to Computer Science for Science, Mathematics, and Engineering 1 (Beginner C++ Programming)

University of California, Riverside *Spring 25, Winter 25, Spring 24*

Teaching Assistant, CS 010B - Introduction to Computer Science for Science, Mathematics, and Engineering 2 (Intermediate C++ Programming)

University of California, Riverside *Winter 24*

Research Assistant, Secure and Efficient Architecture Systems (SEAS) Lab

University of California, Riverside *July 2023 - January 2024*

Research Assistant, Computer Architecture Lab

Institute for Research in Fundamental Sciences (IPM) *July 2021 - January 2022*

Teaching Assistant, Design of Digital Circuits

Shahid Beheshti University *Fall 2020*

Honors and Awards

Dean's Distinguished Fellowship Award.

Awarded by University of California, Riverside (UCR) for Academic year 2022 *March 2022*

Services

Volunteer, ASPLOS 2024 Conference Organizing Team

International Conference on Architectural Support for Programming Languages and Operating Systems *April 2024*

Certificates

Deep Learning Specialization *Coursera*

DeepLearning.ai *December 2022*

https://www.credly.com/badges/544e29b5-28ac-4bc4-9218-9402f77510ee