Archit Halder
Student

An Engineer seeking the position where I can utilize my professional skills towards the growth of the organization. Ability to accept professional challenges and opportunities to make use of my strength and build up my career.

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Jamshedpur, India 📍

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EDUCATION

M.TECH
National Institute of Technology, Jamshedpur

07/2019 - Present   *CGPA - 9.45*

Project
- Difference between Wet and Dry Oxidation at different temperature and pressure variations using Athena (TCAD)

B.TECH
Maharaja Agrasen Institute of Technology, Delhi

08/2014 - 07/2018   *Percentage - 81.63%*

Projects
- Data Aquisition System
- Automatic Density based Traffic Light Systems

HIGHER SECONDARY
Kendriya Vidyalaya (CBSE)

03/2013   *Percentage - 93.8% (PCMB - 12th)*

WORK EXPERIENCE

Design Verification Trainee
MasterVLSI

05/2020 - Present   *Bangalore*

Achievements/Tasks
- Knowledge in TEST CASE writing RTL Debugging.
- Experience in developing SystemVerilog and UVM based Verification Environment.
- Real Time Script Development using Python and PERL for Regression Analysis.
- Real Time Script Development of RAL based Verification Environmet.

Online FDP on Embedded UVM on open source Emulation and Functional Verification
IIT Guwahati

07/2020 - Present

Tasks-
- Simple DuT with UVM testbench.
- SHA3 Dut with UVM testbench.
- Accessing the FPGA design from C code running on Cyclon V HPS.

SKILLS

UVM · SystemVerilog · Verilog · APB · AXI · AHB · gVIM · Python Scripting · PERL Scripting · Digital VLSI Design · C · Computer Architecture & Organization · git · Ubuntu · CTAGS · RAL · Quartus · iVerilog · Questasim · JTAGs · RISC

PERSONAL PROJECTS

Project 1: MEMORY verification VIP development using UVM
- VIP component development for memory verification protocols. As part of this project we have developed SEQUENCER, DRIVER (Heart of verification module), MONITOR, SCOREBOARD.
- Development and Coding of Memory Architecture.
- Successfully developed TESTBENCH PLAN. Methodology used in UVM.

Project 2: APB 1.0 Development using UVM
- Developed VIP component for APB protocol. Development of Sequencer, Driver, Monitor.
- Developed basic scenarios targetting all features of APB protocol.
- Responsibilities included the development and coding APB architecture using UVM methodology. Preparation of Testbench plan.

Project 3: AHB 2.0 VIP Development using UVM
- Developed VIP component for AHB protocol. Developed Sequencer, Driver, Monitor for the same.
- Prepared Testbench plan and verified different test cases using UVM Methodology.

Project 4: Implementation of (2,1,4) Convolutional Encoder and Viterbi Decoder using Verilog

LANGUAGES

English ● ● ● ● ○

Hindi ● ● ● ● ○

Bengali ● ● ● ○ ○