EE224 Digital Circuits-Project

IIT-B CPU

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Finite State Machines for Instructions:

1. **ADD, ADC, ADZ.**

S1

Operations	**Control Signal**
RF_7 → MEM_ADD MEM_DATA → IR RF_7 → ALU _A +1 → ALU_B ALU_C → RF_7	MEM_RD RF_7 RF_WR IR_E ADD

S2

Operations	**Control Signal**
if(ins == 0001): IR(8-6)→ RF_AD_OUT1 RF_DA_OUT1 → T1 elseif(ins == 0000 or ins == 0010 or ins == 1100): IR(8-6)→ RF_AD_OUT_1 RF_DA_OUT 1→ T1 IR(11-9) → RF_AD_OUT_2 RF_DA_OUT_2 → T2 elseif(ins==0100 or ins==0101) IR(8-6) →RF_AD_OUT1 RD_DA_OUT1 → T1 IR(5-0) →SE16 _6 → T2	T1_E T2_E

S3

Operations	**Control Signal**
T1 → ALU_A T2 → ALU_B ALU_C → T1	ADD T1_E

S4

Operations	**Control Signal**

If((C==0 && Z==0) ‖(C==1&& Z==0&&Cen==1)‖(Z==1&&Zen ==1&&C==0))
{
IR *5-3* → RF_AD_IN
	RF_WR

T1 → RF_DA_IN }	

2. NDU, NDC, NDZ

S1

Operations	**Control Signal**
RF_7 → MEM_ADD MEM_DATA → IR RF_7 → ALU _A +1 → ALU_B ALU_C → RF_7	MEM_RD RF_7 RF_WR IR_E ADD

S2

Operations	**Control Signal**
if(ins == 0001): IR(8-6)→ RF_AD_OUT1 RF_DA_OUT1 → T1 elseif(ins == 0000 or ins == 0010 or ins == 1100): IR(8-6)→ RF_AD_OUT_1 RF_DA_OUT 1→ T1 IR(11-9) → RF_AD_OUT_2 RF_DA_OUT_2 → T2 elseif(ins==0100 or ins==0101) IR(8-6) →RF_AD_OUT1 RD_DA_OUT1 → T1 IR(5-0) →SE16 _6 → T2	T1_E T2_E

S5:

Operations	**Control Signal**
T1 → ALU_A T2 → ALU_B ALU_C → T1	NAND T1_E

S4

Operations	**Control Signal**

If((C==0 && Z==0) ‖(C==1&& Z==0&&Cen==1)‖(Z==1&&Zen ==1&&C==0))
{
IR *5-3* → RF_AD_IN
T1 → RF_DA_IN
}
	RF_WR

3. ADI

S1

Operations	**Control Signal**
RF_7 → MEM_ADD MEM_DATA → IR RF_7 → ALU _A +1 → ALU_B ALU_C → RF_7	MEM_RD RF_7 RF_WR IR_E ADD

S2

Operations	**Control Signal**
if(ins == 0001): IR(8-6)→ RF_AD_OUT1 RF_DA_OUT1 → T1 elseif(ins == 0000 or ins == 0010 or ins == 1100): IR(8-6)→ RF_AD_OUT_1 RF_DA_OUT 1→ T1 IR(11-9) → RF_AD_OUT_2 RF_DA_OUT_2 → T2 elseif(ins==0100 or ins==0101) IR(8-6) →RF_AD_OUT1 RD_DA_OUT1 → T1 IR(5-0) →SE16 _6 → T2	T1_E T2_E

S3

Operations	**Control Signal**
T1 → ALU_A T2 → ALU_B ALU_C → T1	ADD T1_E

S6

Operations	**Control Signal**
T1 → RF_DA_IN $IR_{(8-6)}$→ RF_AD_IN	RF_WR

4. LHI

S1

Operations	**Control Signal**
RF_7 → MEM_ADD MEM_DATA → IR RF_7 → ALU _A +1 → ALU_B ALU_C → RF_7	MEM_RD RF_7 RF_WR IR_E ADD

S7

Operations	**Control Signal**
$IR_{(8-0)}$ → SE16_9 → T1	T1_E

S8

Operations	**Control Signal**
IR(11−9)->RF_AD_IN T1 → RF_DA_IN	RF_WR

5. LW

S1

Operations	**Control Signal**
R7 → MEM_ADD MEM_DATA → IR PC → ALU _A +1 → ALU_B ALU_C → R7	MEM_RD PC_E IR_E ADD

S2

Operations	**Control Signal**
if(ins == 0001): IR(8-6)→ RF_AD_OUT1 RF_DA_OUT1 → T1 elseif(ins == 0000 or ins == 0010 or ins == 1100): IR(8-6)→ RF_AD_OUT_1 RF_DA_OUT 1→ T1 IR(11-9) → RF_AD_OUT_2 RF_DA_OUT_2 → T2 elseif(ins==0100 or ins==0101) IR(8-6) →RF_AD_OUT1 RD_DA_OUT1 → T1 IR(5-0) →SE16 _6 → T2	T1_E T2_E

S3

Operations	**Control Signal**
T1 → ALU_A T2 → ALU_B ALU_C → T1	ADD T1_E

S9

Operations	**Control Signal**
IR(11-9) →RF_AD_IN T1 → MEM_ADD MEM_DATA → RF_DA_IN	MEM_RD RF_W

6. **<u>SW</u>**

<u>S1</u>

Operations	**Control Signal**
R7 → MEM_ADD MEM_DATA → IR PC → ALU _A +1 → ALU_B ALU_C → R7	MEM_RD PC_E IR_E ADD

S2

Operations	**Control Signal**
if(ins == 0001): IR(8-6)→ RF_AD_OUT1 RF_DA_OUT1 → T1 elseif(ins == 0000 or ins == 0010 or ins == 1100): IR(8-6)→ RF_AD_OUT_1 RF_DA_OUT 1→ T1 IR(11-9) → RF_AD_OUT_2 RF_DA_OUT_2 → T2 elseif(ins==0100 or ins==0101) IR(8-6) →RF_AD_OUT1 RD_DA_OUT1 → T1 IR(5-0) →SE16 _6 → T2	T1_E T2_E

S3

Operations	**Control Signal**
T1 → ALU_A T2 → ALU_B ALU_C → T1	ADD T1_E

S10

Operations	**Control Signal**
IR(11-9) →RF_AD_OUT T1→MEM_AD RF_DA_OUT→MEM_DATA	MEM_W

7. **<u>LM</u>**

S1

Operations	**Control Signal**
RF_7 → MEM_ADD MEM_DATA → IR RF_7 → ALU _A +1 → ALU_B ALU_C → RF_7	MEM_RD RF_7 RF_WR IR_E ADD

S18

Operations	**Control Signal**
IR(7-0) → Zero_Checker IF(Z=1) S1 Elseif(Z=0) S19	

S19

Operations	**Control Signal**
IR(7-0) → PEN_I PEN_O → RF_AD_IN IR(11-9) → RF_AD_OUT RF_DA_OUT → MEM_AD,T1 MEM_DATA → RF_DA_IN IR(7-0),PEN_O →LU_I LU-O →IR(7-0)	MEM_RD RF_WR IR_E

S20

Operations	**Control Signal**
T1 → ALU _A +1 → ALU_B IR(11-9) → RF_AD_IN ALU_C → RF_DA_IN	RF_WR IR_E ADD

Send to S18

8. **<u>SM</u>**

S1

Operations	**Control Signal**
RF_7 → MEM_ADD MEM_DATA → IR RF_7 → ALU _A +1 → ALU_B ALU_C → RF_7	MEM_RD RF_7 RF_WR IR_E ADD

S22

Operations	**Control Signal**
IR(7-0) →Zero_Checker IF(Z=1) S1 Elseif(Z=0) S21	MEM_RD T3_E

S21

Operations	**Control Signal**
IR(7-0) → PEN_I PEN_O → RF_AD_OUT1 IR(11-9) → RF_AD_OUT_2 RF_DA_OUT_2→ MEM_AD RF_DA_OUT1→MEM_DATA IR(7-0),PEN_O →LU_I LU-O →IR(7-0)	MEM_WR IR_WR

S20

Operations	**Control Signal**
T1 → ALU _A +1 → ALU_B IR(11-9) → RF_AD_IN ALU_C → RF_DA_IN	RF_WR IR_E ADD

Send to S22

9. BEQ

S1

Operations	**Control Signal**
RF_7 → MEM_ADD MEM_DATA → IR RF_7 → ALU _A +1 → ALU_B ALU_C → RF_7	MEM_RD RF_7 RF_WR IR_E ADD

S2

Operations	**Control Signal**
if(ins == 0001): IR(8-6)→ RF_AD_OUT1 RF_DA_OUT1 → T1 elseif(ins == 0000 or ins == 0010 or ins == 1100): IR(8-6)→ RF_AD_OUT_1 RF_DA_OUT 1→ T1 IR(11-9) → RF_AD_OUT_2 RF_DA_OUT_2 → T2 elseif(ins==0100 or ins==0101) IR(8-6) →RF_AD_OUT1 RD_DA_OUT1 → T1 IR(5-0) →SE16 _6 → T2	T1_E T2_E

S11

Operations	**Control Signal**
T1→ALU.A T2→ ALU.B ALU.C →T1	SUB

IF Z=1 THEN

S12

Operations	**Control Signal**
RF_7→ALU A +1→ALU.B ALU.C →RF_7	SUB RF_WR

S13

Operations	**Control Signal**
IR(5-0)→SE16_6→ALU B RF_7→ALU.A ALU.C →RF_7	ADD RF_WR

10. <u>JAL</u>

S1

Operations	**Control Signal**
RF_7 → MEM_ADD MEM_DATA → IR RF_7 → ALU _A +1 → ALU_B ALU_C → RF_7	MEM_RD RF_7 RF_WR IR_E ADD

S12

Operations	**Control Signal**
RF_7→ALU A +1→ALU.B ALU.C →RF_7	SUB RF_WR

S14

Operations	**Control Signal**
IR(11-9) →RF_AD_IN RF_7 → RF_DA_IN	RF_W

S15

Operations	**Control Signal**
RF_7 → ALU_A IR(0-8) →SE16_9→ALU.B ALU.C→ RF_7	RF_W RF_S7 ADD

11. JLR

S1

Operations	**Control Signal**
RF_7 → MEM_ADD MEM_DATA → IR RF_7 → ALU _A +1 → ALU_B ALU_C → RF_7	MEM_RD RF_7 RF_WR IR_E ADD

S16

Operations	**Control Signal**
RF_7→ALU A +1→ALU.B IR(11-9) →RF_AD_IN ALU.C →RF_DA_IN	SUB RF_WR

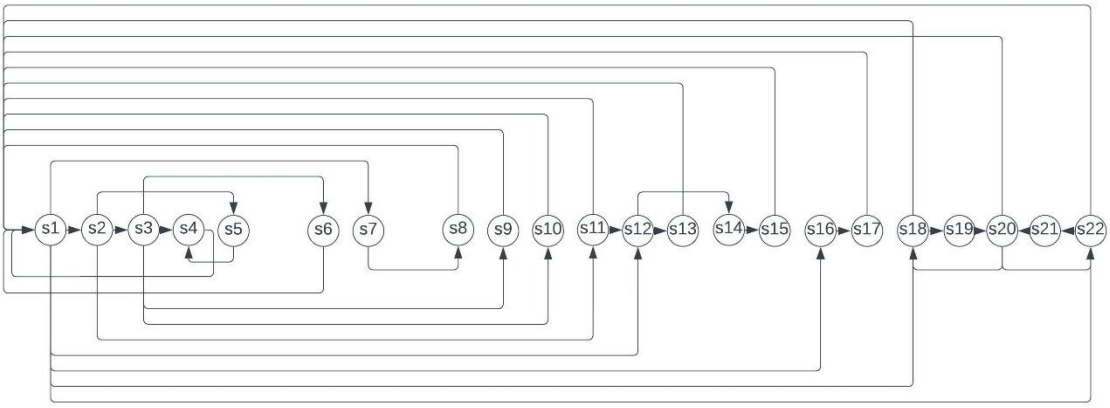
S17

Operations	**Control Signal**
IR(8-6) → RF_AD_OUT RF_DA_OUT → RF_7_IN	RF_WR

State Transition Table

Current	Next	Condition
S1	S2	(!IR15 and !IR14 and !IR13 and !IR12) or (!IR15 and !IR14 and !IR13 and IR12) or (!IR15 and !IR14 and IR13 and !IR12) or (!IR15 and IR14 and !IR13 and !IR12) or (!IR15 and IR14 and !IR13 and IR12) or (IR15 and IR14 and !IR13 and !IR12)
S1	S7	!IR15 and !IR14 and IR13 and IR12
S1	S12	IR15 and !IR14 and !IR13 and !IR12
S1	S16	IR15 and !IR14 and !IR13 and IR12
S1	S18	!IR15 and IR14 and IR13 and !IR12
S1	S22	!IR15 and IR14 and IR13 and IR12
S2	S3	(!IR15 and !IR14 and !IR13 and !IR12) or (!IR15 and !IR14 and !IR13 and IR12) or (!IR15 and IR14 and !IR13 and !IR12) or (!IR15 and IR14 and !IR13 and IR12)
S2	S5	!IR15 and !IR14 and IR13 and !IR12
S2	S11	IR15 and IR14 and !IR13 and !IR12
S3	S4	!IR15 and !IR14 and !IR13 and !IR12
S3	S6	!IR15 and !IR14 and !IR13 and IR12
S3	S9	!IR15 and IR14 and !IR13 and !IR12
S3	S10	!IR15 and IR14 and !IR13 and IR12
S4	S1	unconditional
S5	S4	unconditional
S6	S1	unconditional
S7	S8	unconditional
S8	S1	unconditional
S9	S1	unconditional
S10	S1	unconditional
S11	S1	!Z
S11	S12	Z
S12	S13	IR15 and IR14 and !IR13 and !IR12
S12	S14	IR15 and !IR14 and !IR13 and !IR12
S13	S1	unconditional
S14	S15	unconditional
S15	S1	unconditional
S16	S17	unconditional
S17	S1	unconditional
S18	S1	Z
S18	S19	!Z
S19	S20	unconditional
S20	S18	!IR15 and IR14 and IR13 and !IR12
S20	S22	!IR15 and IR14 and IR13 and IR12
S22	S1	Z
S22	S21	!Z
S21	S20	unconditional

State Diagram



Datapath