**EE224 Digital Circuits-Project**

*IIT-B CPU*

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**Finite State Machines for Instructions:**

1. **ADD, ADC, ADZ.**

**S1**

|  |  |
| --- | --- |
| **Operations** | **Control Signal** |
| RF\_7 → MEM\_ADD  MEM\_DATA → IR  RF\_7 → ALU \_A  +1 → ALU\_B  ALU\_C → RF\_7 | MEM\_RD  RF\_7  RF\_WR  IR\_E  ADD |

**S2**

|  |  |
| --- | --- |
| **Operations** | **Control Signal** |
| if(ins == 0001):  IR(8-6)→ RF\_AD\_OUT1  RF\_DA\_OUT1 → T1  elseif(ins == 0000 or ins == 0010 or ins == 1100):  IR(8-6)→ RF\_AD\_OUT\_1  RF\_DA\_OUT 1→ T1  IR(11-9) → RF\_AD\_OUT\_2  RF\_DA\_OUT\_2 → T2  elseif(ins==0100 or ins==0101)  IR(8-6) →RF\_AD\_OUT1  RD\_DA\_OUT1 → T1  IR(5-0) →SE16 \_6 → T2 | T1\_E  T2\_E |

**S3**

|  |  |
| --- | --- |
| **Operations** | **Control Signal** |
| T1 → ALU\_A  T2 → ALU\_B  ALU\_C → T1 | ADD  T1\_E |

**S4**

|  |  |
| --- | --- |
| **Operations** | **Control Signal** |
| If( (C==0 && Z==0) ||(C==1&& Z==0&&Cen==1)||(Z==1&&Zen==1&&C==0))  {  IR *5-3* → RF\_AD\_IN  T1 → RF\_DA\_IN  } | RF\_WR |

1. **NDU, NDC, NDZ**

**S1**

|  |  |
| --- | --- |
| **Operations** | **Control Signal** |
| RF\_7 → MEM\_ADD  MEM\_DATA → IR  RF\_7 → ALU \_A  +1 → ALU\_B  ALU\_C → RF\_7 | MEM\_RD  RF\_7  RF\_WR  IR\_E  ADD |

**S2**

|  |  |
| --- | --- |
| **Operations** | **Control Signal** |
| if(ins == 0001):  IR(8-6)→ RF\_AD\_OUT1  RF\_DA\_OUT1 → T1  elseif(ins == 0000 or ins == 0010 or ins == 1100):  IR(8-6)→ RF\_AD\_OUT\_1  RF\_DA\_OUT 1→ T1  IR(11-9) → RF\_AD\_OUT\_2  RF\_DA\_OUT\_2 → T2  elseif(ins==0100 or ins==0101)  IR(8-6) →RF\_AD\_OUT1  RD\_DA\_OUT1 → T1  IR(5-0) →SE16 \_6 → T2 | T1\_E  T2\_E |

**S5:**

|  |  |
| --- | --- |
| **Operations** | **Control Signal** |
| T1 → ALU\_A  T2 → ALU\_B  ALU\_C → T1 | NAND  T1\_E |

**S4**

|  |  |
| --- | --- |
| **Operations** | **Control Signal** |
| If( (C==0 && Z==0) ||(C==1&& Z==0&&Cen==1)||(Z==1&&Zen==1&&C==0))  {  IR *5-3* → RF\_AD\_IN  T1 → RF\_DA\_IN  } | RF\_WR |

1. **ADI**

**S1**

|  |  |
| --- | --- |
| **Operations** | **Control Signal** |
| RF\_7 → MEM\_ADD  MEM\_DATA → IR  RF\_7 → ALU \_A  +1 → ALU\_B  ALU\_C → RF\_7 | MEM\_RD  RF\_7  RF\_WR  IR\_E  ADD |

**S2**

|  |  |
| --- | --- |
| **Operations** | **Control Signal** |
| if(ins == 0001):  IR(8-6)→ RF\_AD\_OUT1  RF\_DA\_OUT1 → T1  elseif(ins == 0000 or ins == 0010 or ins == 1100):  IR(8-6)→ RF\_AD\_OUT\_1  RF\_DA\_OUT 1→ T1  IR(11-9) → RF\_AD\_OUT\_2  RF\_DA\_OUT\_2 → T2  elseif(ins==0100 or ins==0101)  IR(8-6) →RF\_AD\_OUT1  RD\_DA\_OUT1 → T1  IR(5-0) →SE16 \_6 → T2 | T1\_E  T2\_E |

**S3**

|  |  |
| --- | --- |
| **Operations** | **Control Signal** |
| T1 → ALU\_A  T2 → ALU\_B  ALU\_C → T1 | ADD  T1\_E |

**S6**

|  |  |
| --- | --- |
| **Operations** | **Control Signal** |
| T1 → RF\_DA\_IN  → RF\_AD\_IN | RF\_WR |

1. **LHI**

**S1**

|  |  |
| --- | --- |
| **Operations** | **Control Signal** |
| RF\_7 → MEM\_ADD  MEM\_DATA → IR  RF\_7 → ALU \_A  +1 → ALU\_B  ALU\_C → RF\_7 | MEM\_RD  RF\_7  RF\_WR  IR\_E  ADD |

**S7**

|  |  |
| --- | --- |
| **Operations** | **Control Signal** |
| → SE16\_9 → T1 | T1\_E |

**S8**

|  |  |
| --- | --- |
| **Operations** | **Control Signal** |
| IR(11−9)->RF\_AD\_IN  T1 → RF\_DA\_IN | RF\_WR |

1. **LW**

**S1**

|  |  |
| --- | --- |
| **Operations** | **Control Signal** |
| R7 → MEM\_ADD  MEM\_DATA → IR  PC → ALU \_A  +1 → ALU\_B  ALU\_C → R7 | MEM\_RD  PC\_E  IR\_E  ADD |

**S2**

|  |  |
| --- | --- |
| **Operations** | **Control Signal** |
| if(ins == 0001):  IR(8-6)→ RF\_AD\_OUT1  RF\_DA\_OUT1 → T1  elseif(ins == 0000 or ins == 0010 or ins == 1100):  IR(8-6)→ RF\_AD\_OUT\_1  RF\_DA\_OUT 1→ T1  IR(11-9) → RF\_AD\_OUT\_2  RF\_DA\_OUT\_2 → T2  elseif(ins==0100 or ins==0101)  IR(8-6) →RF\_AD\_OUT1  RD\_DA\_OUT1 → T1  IR(5-0) →SE16 \_6 → T2 | T1\_E  T2\_E |

**S3**

|  |  |
| --- | --- |
| **Operations** | **Control Signal** |
| T1 → ALU\_A  T2 → ALU\_B  ALU\_C → T1 | ADD  T1\_E |

**S9**

|  |  |
| --- | --- |
| **Operations** | **Control Signal** |
| IR(11-9) →RF\_AD\_IN  T1 → MEM\_ADD  MEM\_DATA → RF\_DA\_IN | MEM\_RD  RF\_W |

1. **SW**

**S1**

|  |  |
| --- | --- |
| **Operations** | **Control Signal** |
| R7 → MEM\_ADD  MEM\_DATA → IR  PC → ALU \_A  +1 → ALU\_B  ALU\_C → R7 | MEM\_RD  PC\_E  IR\_E  ADD |

**S2**

|  |  |
| --- | --- |
| **Operations** | **Control Signal** |
| if(ins == 0001):  IR(8-6)→ RF\_AD\_OUT1  RF\_DA\_OUT1 → T1  elseif(ins == 0000 or ins == 0010 or ins == 1100):  IR(8-6)→ RF\_AD\_OUT\_1  RF\_DA\_OUT 1→ T1  IR(11-9) → RF\_AD\_OUT\_2  RF\_DA\_OUT\_2 → T2  elseif(ins==0100 or ins==0101)  IR(8-6) →RF\_AD\_OUT1  RD\_DA\_OUT1 → T1  IR(5-0) →SE16 \_6 → T2 | T1\_E  T2\_E |

**S3**

|  |  |
| --- | --- |
| **Operations** | **Control Signal** |
| T1 → ALU\_A  T2 → ALU\_B  ALU\_C → T1 | ADD  T1\_E |

**S10**

|  |  |
| --- | --- |
| **Operations** | **Control Signal** |
| IR(11-9) →RF\_AD\_OUT  T1→MEM\_AD  RF\_DA\_OUT→MEM\_DATA | MEM\_W |

1. **LM**

**S1**

|  |  |
| --- | --- |
| **Operations** | **Control Signal** |
| RF\_7 → MEM\_ADD  MEM\_DATA → IR  RF\_7 → ALU \_A  +1 → ALU\_B  ALU\_C → RF\_7 | MEM\_RD  RF\_7  RF\_WR  IR\_E  ADD |

**S18**

|  |  |
| --- | --- |
| **Operations** | **Control Signal** |
| IR(7-0)→ Zero\_Checker  IF(Z=1)  S1  Elseif(Z=0)  S19 |  |

**S19**

|  |  |
| --- | --- |
| **Operations** | **Control Signal** |
| IR(7-0)→ PEN\_I  PEN\_O → RF\_AD\_IN  IR(11-9) → RF\_AD\_OUT  RF\_DA\_OUT → MEM\_AD,T1  MEM\_DATA → RF\_DA\_IN  IR(7-0),PEN\_O →LU\_I  LU-O →IR(7-0) | MEM\_RD  RF\_WR  IR\_E |

**S20**

|  |  |
| --- | --- |
| **Operations** | **Control Signal** |
| T1 → ALU \_A  +1 → ALU\_B  IR(11-9) → RF\_AD\_IN  ALU\_C → RF\_DA\_IN | RF\_WR  IR\_E  ADD |

**Send to S18**

1. **SM**

**S1**

|  |  |
| --- | --- |
| **Operations** | **Control Signal** |
| RF\_7 → MEM\_ADD  MEM\_DATA → IR  RF\_7 → ALU \_A  +1 → ALU\_B  ALU\_C → RF\_7 | MEM\_RD  RF\_7  RF\_WR  IR\_E  ADD |

**S22**

|  |  |
| --- | --- |
| **Operations** | **Control Signal** |
| IR(7-0)→Zero\_Checker  IF(Z=1)  S1  Elseif(Z=0)  S21 | MEM\_RD  T3\_E |

**S21**

|  |  |
| --- | --- |
| **Operations** | **Control Signal** |
| IR(7-0)→ PEN\_I  PEN\_O → RF\_AD\_OUT1  IR(11-9) → RF\_AD\_OUT\_2  RF\_DA\_OUT\_2→ MEM\_AD  RF\_DA\_OUT1→MEM\_DATA  IR(7-0),PEN\_O →LU\_I  LU-O →IR(7-0) | MEM\_WR  IR\_WR |

**S20**

|  |  |
| --- | --- |
| **Operations** | **Control Signal** |
| T1 → ALU \_A  +1 → ALU\_B  IR(11-9) → RF\_AD\_IN  ALU\_C → RF\_DA\_IN | RF\_WR  IR\_E  ADD |

**Send to S22**

1. **BEQ**

**S1**

|  |  |
| --- | --- |
| **Operations** | **Control Signal** |
| RF\_7 → MEM\_ADD  MEM\_DATA → IR  RF\_7 → ALU \_A  +1 → ALU\_B  ALU\_C → RF\_7 | MEM\_RD  RF\_7  RF\_WR  IR\_E  ADD |

**S2**

|  |  |
| --- | --- |
| **Operations** | **Control Signal** |
| if(ins == 0001):  IR(8-6)→ RF\_AD\_OUT1  RF\_DA\_OUT1 → T1  elseif(ins == 0000 or ins == 0010 or ins == 1100):  IR(8-6)→ RF\_AD\_OUT\_1  RF\_DA\_OUT 1→ T1  IR(11-9) → RF\_AD\_OUT\_2  RF\_DA\_OUT\_2 → T2  elseif(ins==0100 or ins==0101)  IR(8-6) →RF\_AD\_OUT1  RD\_DA\_OUT1 → T1  IR(5-0) →SE16 \_6 → T2 | T1\_E  T2\_E |

**S11**

|  |  |
| --- | --- |
| **Operations** | **Control Signal** |
| T1→ALU.A  T2→ ALU.B  ALU.C →T1 | SUB |

**IF Z=1 THEN**

**S12**

|  |  |
| --- | --- |
| **Operations** | **Control Signal** |
| RF\_7→ALU A  +1→ALU.B  ALU.C →RF\_7 | SUB  RF\_WR |

**S13**

|  |  |
| --- | --- |
| **Operations** | **Control Signal** |
| IR(5-0)→SE16\_6→ALU B  RF\_7→ALU.A  ALU.C →RF\_7 | ADD  RF\_WR |

1. **JAL**

**S1**

|  |  |
| --- | --- |
| **Operations** | **Control Signal** |
| RF\_7 → MEM\_ADD  MEM\_DATA → IR  RF\_7 → ALU \_A  +1 → ALU\_B  ALU\_C → RF\_7 | MEM\_RD  RF\_7  RF\_WR  IR\_E  ADD |

**S12**

|  |  |
| --- | --- |
| **Operations** | **Control Signal** |
| RF\_7→ALU A  +1→ALU.B  ALU.C →RF\_7 | SUB  RF\_WR |

**S14**

|  |  |
| --- | --- |
| **Operations** | **Control Signal** |
| IR(11-9) →RF\_AD\_IN  RF\_7 → RF\_DA\_IN | RF\_W |

**S15**

|  |  |
| --- | --- |
| **Operations** | **Control Signal** |
| RF\_7 → ALU\_A  IR(0-8) →SE16\_9→ALU.B  ALU.C→ RF\_7 | RF\_W  RF\_S7  ADD |

1. **JLR**

**S1**

|  |  |
| --- | --- |
| **Operations** | **Control Signal** |
| RF\_7 → MEM\_ADD  MEM\_DATA → IR  RF\_7 → ALU \_A  +1 → ALU\_B  ALU\_C → RF\_7 | MEM\_RD  RF\_7  RF\_WR  IR\_E  ADD |

**S16**

|  |  |
| --- | --- |
| **Operations** | **Control Signal** |
| RF\_7→ALU A  +1→ALU.B  IR(11-9) →RF\_AD\_IN  ALU.C →RF\_DA\_IN | SUB  RF\_WR |

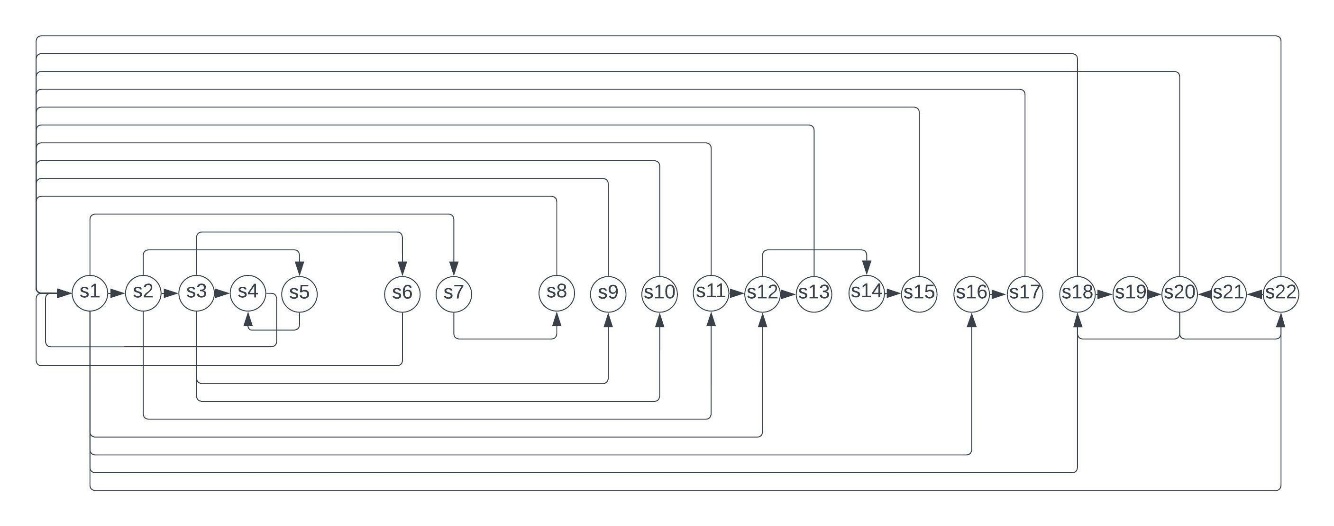
**S17**

|  |  |
| --- | --- |
| **Operations** | **Control Signal** |
| IR(8-6) → RF\_AD\_OUT  RF\_DA\_OUT → RF\_7\_IN | RF\_WR |

**State Transition Table**

|  |  |  |
| --- | --- | --- |
| Current | Next | Condition |
| S1 | S2 | (!IR15 and !IR14 and !IR13 and !IR12) or (!IR15 and !IR14 and !IR13 and IR12) or (!IR15 and !IR14 and IR13 and !IR12) or (!IR15 and IR14 and !IR13 and !IR12) or (!IR15 and IR14 and !IR13 and IR12) or (IR15 and IR14 and !IR13 and !IR12) |
| S1 | S7 | !IR15 and !IR14 and IR13 and IR12 |
| S1 | S12 | IR15 and !IR14 and !IR13 and !IR12 |
| S1 | S16 | IR15 and !IR14 and !IR13 and IR12 |
| S1 | S18 | !IR15 and IR14 and IR13 and !IR12 |
| S1 | S22 | !IR15 and IR14 and IR13 and IR12 |
| S2 | S3 | (!IR15 and !IR14 and !IR13 and !IR12) or (!IR15 and !IR14 and !IR13 and IR12) or (!IR15 and IR14 and !IR13 and !IR12) or (!IR15 and IR14 and !IR13 and IR12) |
| S2 | S5 | !IR15 and !IR14 and IR13 and !IR12 |
| S2 | S11 | IR15 and IR14 and !IR13 and !IR12 |
| S3 | S4 | !IR15 and !IR14 and !IR13 and !IR12 |
| S3 | S6 | !IR15 and !IR14 and !IR13 and IR12 |
| S3 | S9 | !IR15 and IR14 and !IR13 and !IR12 |
| S3 | S10 | !IR15 and IR14 and !IR13 and IR12 |
| S4 | S1 | unconditional |
| S5 | S4 | unconditional |
| S6 | S1 | unconditional |
| S7 | S8 | unconditional |
| S8 | S1 | unconditional |
| S9 | S1 | unconditional |
| S10 | S1 | unconditional |
| S11 | S1 | !Z |
| S11 | S12 | Z |
| S12 | S13 | IR15 and IR14 and !IR13 and !IR12 |
| S12 | S14 | IR15 and !IR14 and !IR13 and !IR12 |
| S13 | S1 | unconditional |
| S14 | S15 | unconditional |
| S15 | S1 | unconditional |
| S16 | S17 | unconditional |
| S17 | S1 | unconditional |
| S18 | S1 | Z |
| S18 | S19 | !Z |
| S19 | S20 | unconditional |
| S20 | S18 | !IR15 and IR14 and IR13 and !IR12 |
| S20 | S22 | !IR15 and IR14 and IR13 and IR12 |
| S22 | S1 | Z |
| S22 | S21 | !Z |
| S21 | S20 | unconditional |

**State Diagram**



**Datapath**

