Computer Architecture Research Proposal
"Bringing The Multicore Processor Up To Speed"

In 1943 Thomas Watson predicted, "I think there is a world market for maybe five computers". Today, that prediction falls short of the market for a single household. Early computers the size of warehouses once served the same purpose that today can be accomplished with a $10 Arduino chip that can fit in the palm of a hand. Many innovations have bridged that gap in the last few decades and one of the most prolific was the advent of the multicore processor. Unfortunately, while the multicore processor has alleviated the power consumption and overheating issues that accompany continuous frequency scaling in single core processors, they present a new set of challenges to surmount. The largest qualms with multicore design are interference problems that arise when cores try to access shared resources concurrently. In order to perform basic instruction sets, multicores have to share access to DRAM, memory buses, I/O resources and caches. Some potential solutions to these conflicts are: software applications that allocate memory and bandwidth to cores based on demand in real time, replacing traditional bus connections using routers and a hardware communication network between the cores, adjusting the communication hierarchy of routers. The implications of increased core utilization are significant gains in efficiency of throughput and energy usage. The incentive is straightforward; if we optimize multicore technology we get faster and more powerful computers.

References: (all accessed via IEEE xplore)

"Real-Time Computing on Multicore Processors"

"Predicting Cross-Core Performance Interference On Multicore Processors With Regression Analysis"

"Amdahl's Law For Lifetime Reliability Scaling In Heterogeneous Multicore Processors"

"Research On Topology And Policy For Low Power Consumption Of Network-On-Chip With Multicore Processors"