50 ps    20 ps       150 ps      20 ps     100 ps     20 ps

Comb. logic A

Reg

Comb. logic B
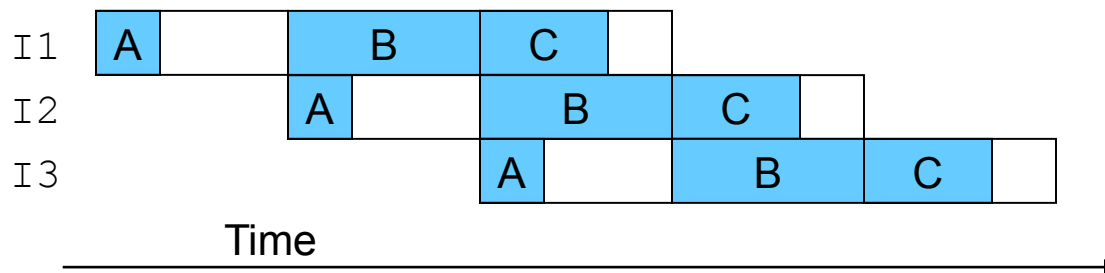
Reg

Comb. logic C

Reg

Delay = 510 ps
Throughput = 5.88 GIPS

Clock

(a) Hardware: Three-stage pipeline, nonuniform stage delays

I1   A   B   C
I2   A   B   C
I3   A   B   C

Time

(b) Pipeline diagram