Solder Void Impact on Power Device Thermal Impedance using Transient Thermal Analysis

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***Abstract*— This research explores the relationship between die-attach solder voids and the thermal impedance of high-power semiconductor packages. This is accomplished through an adapted transient system analysis technique, which aims to reduce the impact of extraneous variables in the thermal pathway. Using this method, it is shown that for 25 sample packages the thermal impedance has a high linear correlation with the void percentage (r-squared of 0.884), but that the voids alone contribute a relatively small proportion to the total thermal resistance of the package. In addition, the degradation of the solder layer is also observed through power cycling, where it was found that an increase of the void percentage from 3.8% to 20.5% cut the lifetime in half. These results are used to suggest that the main impact of voids is on the reliability of the module, rather than on the thermal performance.**

Keywords—solder voids, thermal resistance, thermal impedance, reliability

I. Introduction

When soldering a semiconductor chip to a package, small air gaps called voids can be generated. These voids are generated during the reflow process when the flux gasses are unable to escape before the solder re-solidifies [1]. One of the main methods to remove these process-induced voids is the use of a vacuum or pressurized soldering oven [2]. However, these machines are expensive to purchase and operate when compared to traditional convection ovens. This may present a significant barrier to entry for conducting R&D in academic environments, or in industrial settings if the volume of production is too low to justify the cost of advanced solder processes. Another possible area is the mass-production of discrete transistors, where the lower profit margins and the higher throughput rates reduce the desirability of a vacuum process. Thus, it must be understood exactly what impact voids have on power devices in order to accurately gauge whether or not it is worthwhile to invest in void reduction technologies.

There are many potential impacts that voids have on the performance of power devices. This paper primarily investigates how voids affect the thermal impedance of a package, with a secondary focus on assessing their impact on reliability. These two areas are of particular importance for high-power semiconductor packages due to the high amount of heat dissipation per unit volume (energy density) as well as their required operating lifetimes.

In this article, the term “thermal impedance” $Z_{th}(t)$ is used to describe the time-dependent obstruction to the flow of heat, whereas the term "thermal resistance” describes the steady-state settling point of $Z_{th}(t)$. Thermal resistance accounts for every layer from the point of heat generation to the point of heat removal. Conversely, the thermal impedance is disproportionately affected by the materials near the point of heat generation directly after a heating event occurs. This property of thermal impedance will be exploited to gain a better understanding of how the solder layer impacts the thermal performance without the variance caused by lower layers.

II. Experimental Procedure

A. Sample Module Construction

For this experiment, 25 sample modules consisting of a single power diode rated at 600V and 50A (VS-4FD198H06A6BC) were constructed (Fig. 1). Each module was soldered using a lead-free SAC305 solder paste. The solder paste was acquired from two different manufacturers in order to reduce bias from a single paste type. The *Manncorp MC 301* convection reflow oven was used, and three separate temperature profiles were employed in order to produce modules with a wide range of voiding levels.

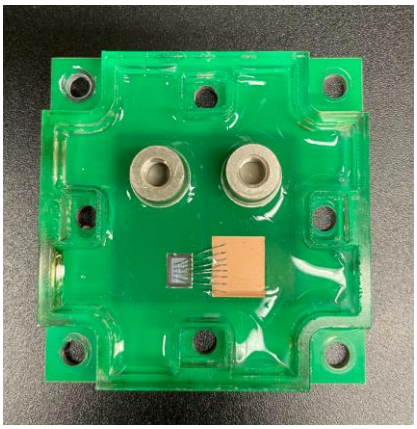

Fig. 1. Construction of the single-diode module.

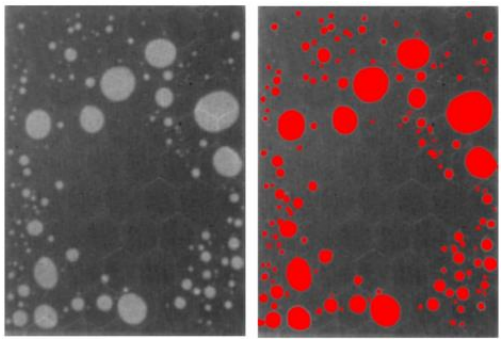

Fig. 2. Raw x-ray image of solder layer (left) and processed image (right).

An additional technique first introduced in [1] was also employed for 5 samples. This manufacturing method involves reflowing the die-attach solder without the chip mounted, then placing four small balls of solder paste on the corners of the mounting area and placing the chip, and then reflowing the device for a second time. This was done in order to obtain samples with a lowered void count, as well as to provide a second point of comparison for the results obtained in [3]. It was found that this method reduced voids by nearly half; the average void percentage following this method was 10.7% compared to the control group with 20.2% voids.

After the reflow process, the voids were imaged (Fig. 2) using the *Glenbrook RTX-113 HV* x-ray machine. In order to accurately map the voided areas of the solder layer and calculate the void percentage, the x-ray images were processed in *Photoshop* using the fill tool as a method to selectively highlight the voided areas. The "contiguous" mode was used on the fill tool, and the following threshold setting were used: 35, 27, 20, 13, 5. Higher threshold settings more easily fill large voids and voids with highly-contrasted edges, while low settings are optimal for areas with low contrast. The variance due to manual processing was also measured, with an average relative percent error of 5.6% for the fill tool method. This error metric was tested by re-processing four of the x-ray images several days after their initial completion, and comparing the void ratio to the original copies. After this process, the images were then cropped to include only the solder layer, and then a *Python* script was used to calculate the percentage of highlighted pixels.

The topside connections of the modules were made using either eight 250 μm diameter wire bonds or six 300 μm diameter wire bonds. Finally, a fiberglass enclosure was attached to the module using tacky glue, and the device was enclosed using silicone rubber.

B. Thermal Transient Test

This test was performed similarly to that of [3], with the modification that the main temperature sensitive electrical parameter used here is the forward voltage drop of the diode at I_f = 50 mA. For calibration, this voltage was measured across several diodes from 15°C to 90°C. During the calibration, a thermocouple was used to measure the temperature of the diode. From these measurements, a second-order polynomial fit was generated for the forward voltage relation with temperature.

Next, the samples were secured to a cold plate with a graphite film as the thermal interface material, and each corner of the module was secured using screws with 25 N-m of torque in an x-pattern. Next, a heating current was applied for a duration of 120 seconds. Each module was tested with a heating current of 5, 10, 15, 20, 22, and 24 A. After the heating current was disabled, a sensing current was applied, and the junction temperature was measured at logarithmically spaced time intervals from 200 μs to 200 s. The data before 200 μs was not included due to electrical transient effects of the diode, and instead data was fitted to this region through the assumption that the temperature is approximately linear with the square root of time during this period.

C. Power Cycling Setup

After performing the thermal transient tests, 10 of the samples were subjected to an accelerated lifetime test. In this test, a pulsed current of 24A was applied with an on-time of 1 second and an off-time of 1 second. The main failure criteria for this accelerated lifetime test was an increase in the junction temperature swing ΔT_j of 20% from the starting value. Initially, the average ΔT_j for the ten samples was 113 °C. The number of cycles to failure was then compared with the measured voiding percentages across the samples.

D. Electron Microscopy

Scanning electron microscopy was used to image a cross-section of the solder layers of two samples: one that had just been soldered and another that had been subjected to the power cycling test. For this imaging, a Thermo Scientific Axia ChemiSEM microscope was used. An accelerating voltage of 20 kV was used. The images were collected using a concentric backscatter detector (CBS), where the main focus was to gain insight into the topography of the solder layer. These images assist in determining what the failure mechanism was for the accelerated lifetime test.

III. Mathematical Analysis

To isolate the effects of voids on the thermal impedance of the solder layer, it is crucial to sample the thermal impedance curve $Z_{th}(t)$ at a correct time. Sampling too early would result in a measurement with minimal heat flux passing through the solder layer, while sampling too late would introduce additional variance due to more significant heat flux in the lower layers. In this paper, an adapted interpretation of the time constant intensity (TCS) method is used in order to adequately select the correct time to sample. The derivation for the TCS was first presented in [4].

The first step of the thermal impedance analysis was the transformation from the cooling curve data to the equivalent heating curve. This is mainly done as a way to interpret the results as a heat wave that propagates through the layers, which improves the intuitive understanding of thermal impedance. This transformation requires the assumption that the thermal

system is linear and time-invariant (LTI). The property of linearity approximately holds in this case, as the total change in the thermal impedance from the 5A test to the 24A test was always less than 10% for all modules and all sampling times. Time-invariance also holds because the thermal system does not undergo any substantial change during the thermal testing procedure.

Next, the TCS was calculated using the *T3ster Master* software, which uses the method outlined by V. Széleky in [4]. The TCS describes how the system responds to the heating current in terms of a sum of exponential terms. Peaks in the TCS roughly correspond to points in time where the heat flux reaches a layer with higher thermal impedance. The first peak in Fig. 3 corresponds to the thermal response of the solder layer. These peaks were detected using the *detect_peaks()* function from the *Scipy* library in *Python*. A prominence of 0.003 was used along with the requirement that all peaks had to be greater than the nearest *n* neighbors, where *n* is equal to 1/20th of the total size of the dataset.

In order to most precisely measure the thermal impedance of the solder layer, the optimal time of sampling should occur at some point after the first peak. This is because at exactly one time constant, the heat flux through the solder layer is still well below its maximum value, and so the measurement will be more sensitive to noise. Instead, the measurement should more accurately be taken in the range of 2-5 multiples of the time constant. At this point, the heat flux will be near its steady-state value in the solder layer, while still not fully conducting through the lower unwanted layers.

In [5], the authors found that for their test sample, the authors used a time of 5-10 ms for the solder layer. This value was selected using an alternative method, and it corresponds to the aforementioned 2-5 multiples of the time constant. Additionally, the value of 10 ms was selected in [6]. Different module geometries will generate slightly different thermal responses of the solder layer, although the general correspondence between the results obtained here and those in the aforementioned sources provide reinforcement for the utility of the chosen method of analysis.

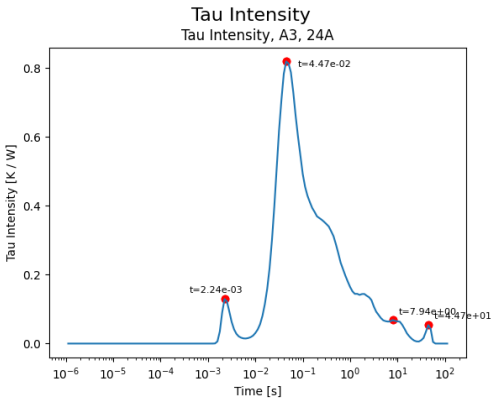

Fig. 3. Time constant spectrum (TCS) with peaks identified.

IV. Results

A. Thermal Impedance Data

By generating the TCS (Fig. 3) for all samples and detecting the generated peaks, a graph of the cumulative total of all peaks is plotted in Fig. 4. From this measure, it can be seen that there is a prominent cluster of peaks at about 2.5 ms. This peak can also be seen in Fig. 3. This first peak corresponds to the first thermal interface that the heat flow encounters, which is the solder layer.

Next, the relationship between the thermal impedance and the void percentage was analyzed as shown in Fig. 5. The time of the thermal impedance measurement was taken at a value of approximately three time constants away from the response of the solder layer, however any time sample between 2.5 ms and 10 ms shows a similar pattern. This indicates that there is a strong correlation between the void percentage and the thermal impedance. In addition, it was found that a linear fit was sufficient for modeling the relationship.

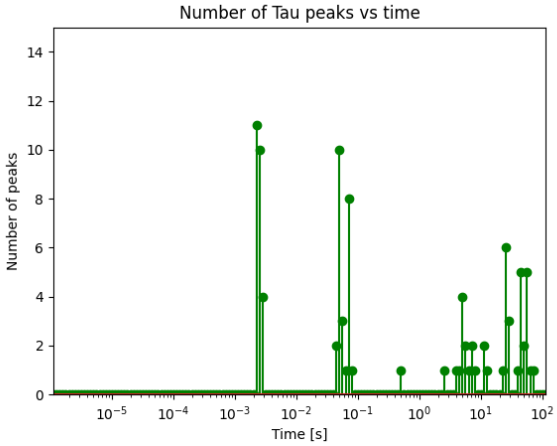

Fig. 4. Cumulative total number of tau peaks across all samples, indicating a collection of peaks near 2.5 ms.

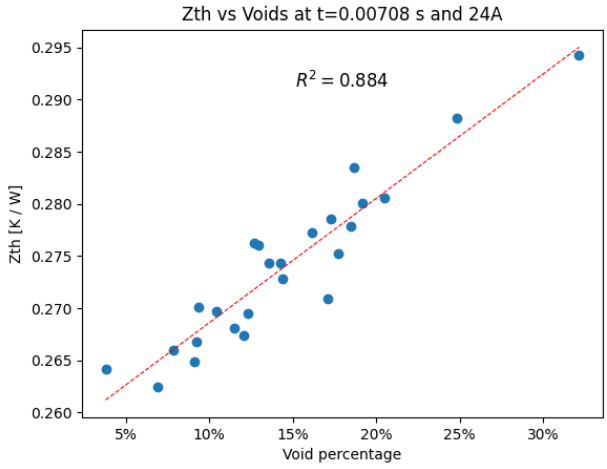

Fig. 5. Thermal impedance vs void percentage at 7 ms, showing a strong linear correlation.

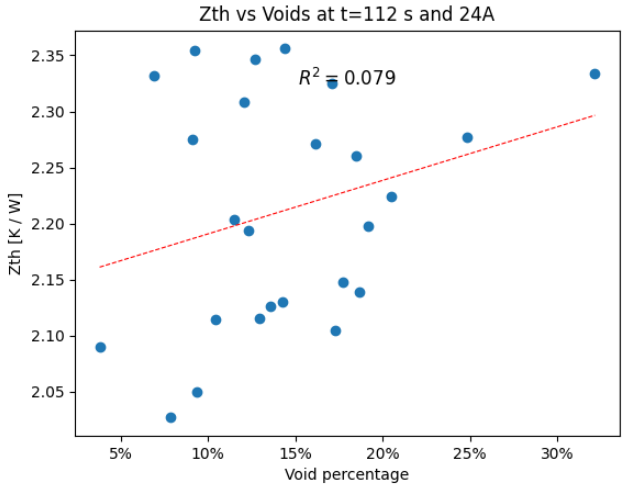

Fig. 6. Total thermal resistance vs void percentage in steady-state, demonstrating a lack of correlation.

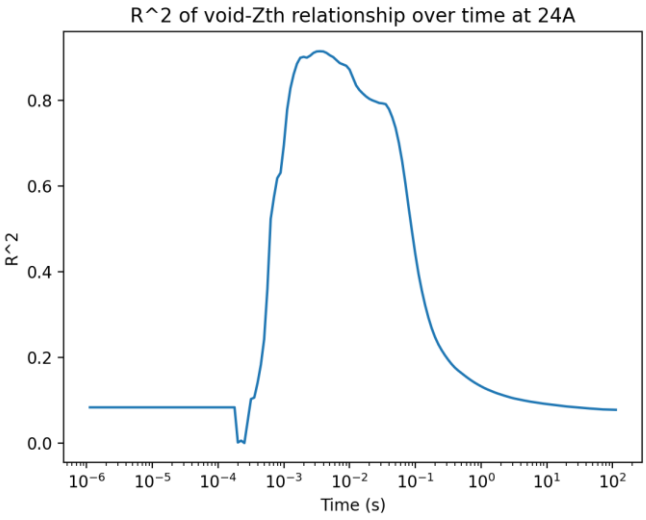

Fig. 7. R-squared value of the linear fit between thermal impedance and void percentage over time, showcasing a strong level of correlation approximately in the range of 2-5 time constants.

This is contrasted by Fig. 6, which shows that for the samples tested, the voids have almost no correlation with the thermal resistance. Comparing Fig. 5 and Fig. 6, it is apparent that there is a relatively large source of variance caused by a lower layer of the thermal stack. This is also confirmed by Fig 7. The heatsink connection is likely a large contributor to the thermal variance, as even with a consistent screw torque and tightening pattern there may still be inconsistent pressure across the samples.

Although the correlation in Fig. 5 is high, it remains to be determined what the absolute impact of voids is on thermal impedance. For example, all samples in Fig. 5 range from about 0.263 K/W to 0.294 K/W. To examine this concept further, observe that the thermal impedance of any package can be approximated using the linear fit as:

$$Z_{total}(t) = Z_0(t) + m(t)v \quad (1)$$

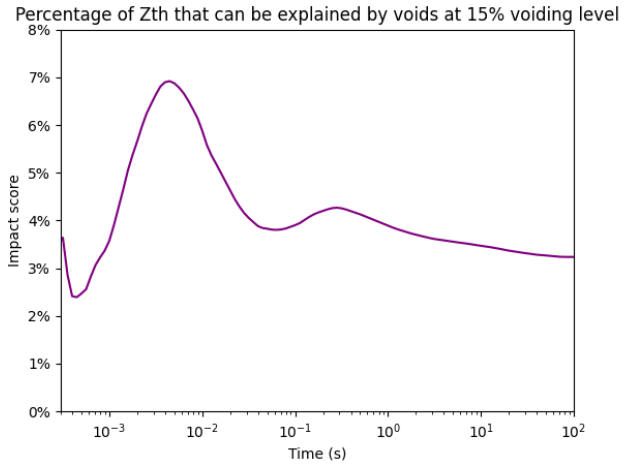

Fig. 8. Percentage of thermal impedance that can be explained by voids alone at a 15% voiding level (values of time after 0.1 seconds are less accurate due to higher variance generated by lower layers).

Where Z_{total} is the total thermal impedance at time t, Z_0 is the impedance of the module originating from sources other than voids (equivalent to the y-intercept of Fig. 5), $m(t)$ is the slope of the line of best fit, and v is the void percentage. Then, a new metric termed the "impact score" $I(t)$ can be used to quantify the percentage of thermal impedance at time t that can be attributed to voids as in:

$$I(t) = m(t)v / Z_{total}(t) \quad (2)$$

Fig. 8 shows this quantity over time for a voiding level of 15%. This demonstrates that even at the 4 ms peak, only about 7% of the thermal impedance can be attributed to voids. The impact score at a specified time also scales nearly linearly with the voiding percentage, so for a module with a voiding level of 7.5%, the impact score would be approximately half of what is depicted below. It is also important to note that the measurements much beyond 0.1 seconds are less accurate due to the added amount of variance of thermal impedance that is encountered at those extended times.

B. Accelerated Lifetime Test Results

In Fig. 9, it is shown that the void percentage has a strong correlation with the number of cycles to failure. Notably, the module with the lowest void percentage at 3.8% demonstrated nearly twice the lifespan of the highest voided sample with 20.5% voids. This effect is much more pronounced than the relatively small impact that the voids demonstrated on thermal impedance (Fig. 8). In addition, the main failure mechanism was determined to be fatigue of the solder layer. This was evidenced by Fig. 10, where the forward of the package did not exhibit any sharp increases due to bond wire liftoff, as were seen in [7]. It was also verified that delamination of the PCB was not a cause of failure, because no delamination effects were observed in the electron microscope images.

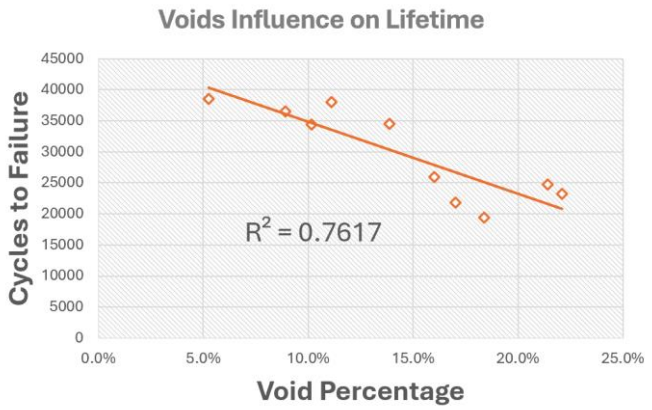

Fig. 9. Relationship between the voiding percentage and the number of cycles to failure.

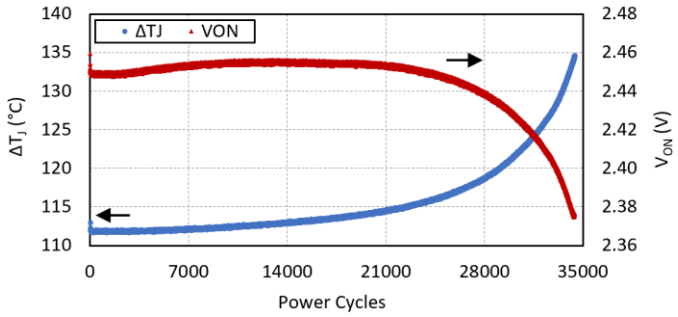

Fig. 10. Evolution of the forward voltage over time, showing that there are no sudden jumps due to bond wire liftoff.

C. *Electron Microscopy*

One of the considerations of the electron microscope images was the determination of whether or not the voids occupied the full height of the solder layer, as this could potentially have some effect on the thermal impedance results. In Fig. 11, the non-cycled die is pictured as having two voids which fill most of the solder layer's height, but do not fill the height entirely. Thus, there may be some impact on the shape of the void on the thermal impedance; verification of this relationship would require the use of an imaging system which can image voids in three dimensions such as an acoustic microscope.

From Fig. 12, it can be seen that the power cycling process caused significant deterioration of the solder layer. The voids both expanded and took on a more jagged appearance. It also can be seen that several cracks propagated outward from the voids as they expanded. In addition, it can also be seen that both the cycled and non-cycled chips are noticeably tilted. This tilting was visually observed in many of the other samples as well. Through the observation of both the x-ray images as well as the SEM photographs, the voids tend to accumulate on the side of the chip where the solder layer is the thickest. This indicates that the voids may have some role in causing the chips to tilt.

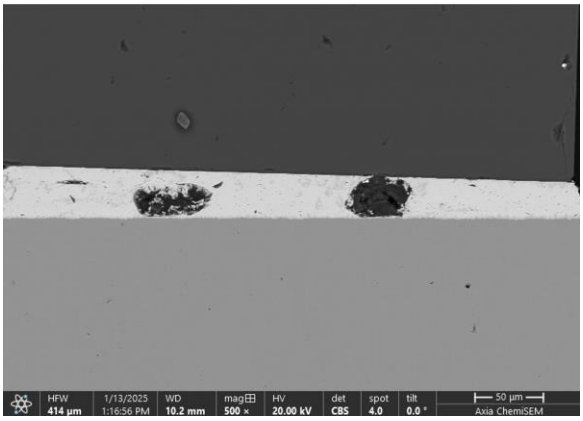

Fig. 11. SEM image of the solder layer of the non-cycled die

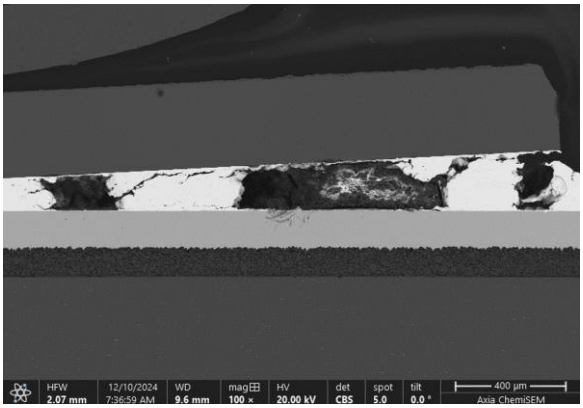

Fig. 12. SEM image of the solder layer of the cycled die.

V. Discussion

The first insight into the role that voids play can be found by comparing Fig. 5 and Fig. 8. These graphs indicate that while voids have a strong relationship with thermal impedance, the actual numerical effect is rather minor. Notably, the test setup described here is less optimized for thermal impedance when compared to commercial power devices, so a higher proportion of the total thermal resistance originates from sources other than the solder layer. This means that an optimized package would likely see an increased impact from voids compared to the results presented in this paper.

Additionally, the power cycling data in Fig. 8 shows that the voids have a significant impact on the lifetime of the samples. There are two potential explanations for this. The first is that the small increase in thermal impedance caused by the voids is magnified due to the inverse-exponential dependence that the module lifetime has on the maximum junction temperature [8]. This temperature is directly proportional to the thermal impedance of the module, and so perhaps due to the very strong decay behavior exhibited by the inverse-exponential relationship, the small change in thermal impedance could cause a large change in the sample's lifetime.

The second possible explanation is that the voids lowered the lifetime primarily due to the effect that they have on the formation and propagation of cracks in the solder layer. In this hypothesis, the voids act as a facilitator for the mechanical damage to the solder layer. This idea is supported by the results

obtained in [9]. In addition, Fig. 12 also demonstrates some level of support for this claim because the most severe cracks span between the voids, and that the area with lower voiding has fewer cracks.

In reality, the actual cause of the power cycling results is probably a combination of the two ideas, however it is likely the case that the second hypothesis plays a much greater role. To demonstrate why, it must be recognized that the total thermal resistance of each sample was influenced by more factors than just the solder layer. These external factors also influence the maximum junction temperature. If the lifetime results were to be primarily influenced by the thermal impedance of each module, the correlation between the lifetime and the void percentage would have been much lower. This demonstrates that the increase in thermal impedance caused by voids is not the main cause of the reduced lifetime seen in the power cycling tests.

VI. Conclusion

This study has explored how voids in the die-attach solder impact the thermal impedance of high-power semiconductor packages. Through this examination, it is determined that while there is a strong correlation between the void percentage and the thermal impedance when sampled at 2-5 multiples of the associated time constant, the actual numerical change is relatively minor. The more significant impact of voids is on the reliability of the device, where a change from 5% to 20% voids cut the lifetime of the device in half. This is also reflected in the electron microscope images, where the thermally stressed sample shows significant cracking between the voided areas but minimal cracking in other locations.

These results indicate that in most cases, semiconductor package manufacturers should focus on lifetime reliability when deciding whether to reduce voids. However, there are some circumstances where the thermal effects of voids may still be relevant. For example, in designs that must tolerate rapid transitions in power dissipation, the thermal impedance of the solder layer is more relevant because the low thermal impedance near the die assists in heat spreading, which slows the rate of temperature rise. Another scenario in which it might be thermally beneficial to remove voids is in specialty packages that are designed to have ultra-low thermal resistance. In this case, even a small reduction of the thermal impedance becomes significant, making void minimization more worthwhile.

To further validate these findings, future studies should explore different semiconductor chips and package constructions. These changes would alter the heat flow path and ensure that the same trends hold true across different device configurations.

Acknowledgments

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