Solder Void Impact on Power Module Thermal Resistance using Transient Thermal Analysis

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Abstract

This research explores the relationship between die-attach solder voids and the thermal resistance of power modules. This is accomplished through transient system analysis in order to reduce the impact of extraneous variables. The data gained through this experiment can be used to guide power module manufacturers on whether void reduction procedures are necessary.

Introduction

In the continual effort to improve the thermal fatigue resistance of power modules, manufacturers have placed a heavy emphasis on the removal of voids in the chip-attach solder layer. However, void reduction procedures often involve a vacuum or pressurized soldering oven, thus increasing the cost of production. Therefore, it is important to gain an accurate understanding of how voids impact the thermal performance of power modules.

In order to address this question, the relationship between the voids and the thermal resistance of the module must be measured. However, one difficulty in this measurement process is the variance in thermal resistance caused by other layers in the power module, such as the heatsink interface. These unwanted effects introduce significant errors to steady-state thermal resistance measurements. Because of this issue, the thermal resistance impact of the solder layer is measured shortly after applying a heating current to the device. This is often described as a transient thermal measurement, and it aims to select a point in time where there is significant heat flux through the solder layer, but minimal flux through the lower layers.

Several authors have examined voids through thermal transient measurements using both finite-element means [1][2][3] as well as through experimental measurements [4][5][6]. However, many sources utilize the structure function method, first introduced in [7]. This method is one of the ways that can be used to select an optimal point in time to perform the thermal resistance measurement. One of the major shortcomings of this method is that it assumes a 1-D Cauer network heat flow model. This does not account for the effect of thermal spreading. Li et. al. showed in [2] that there are significant differences between the behavior predicted by the traditional Cauer network and a 3-D simulation of a voided power module.

This work seeks to improve upon this issue through the use of a thermal transient interpretation which does not rely upon a 1-D assumption of heat flow.

Experimental Procedure

For this experiment, ten sample modules consisting of a single power diode (VS-4FD198H06A6BC) were constructed. Each module was soldered using a SAC305 solder paste. The *Manncorp MC 301* convection reflow oven was used, and two separate temperature profiles were employed in order to produce modules with both low and high void amounts.

First, the voids were imaged using the *Glenbrook RTX-113 HV* X-ray machine. In order to accurately map the voided areas of the solder layer and calculate the void percentage, the X-ray images were processed in

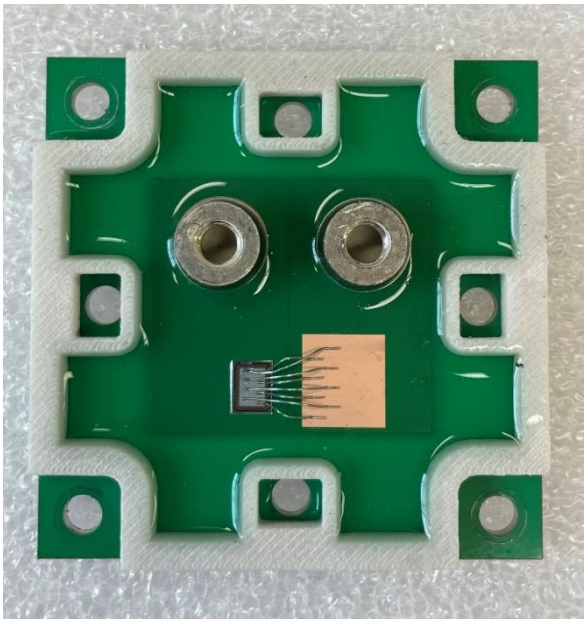

Figure 1. Test module construction.

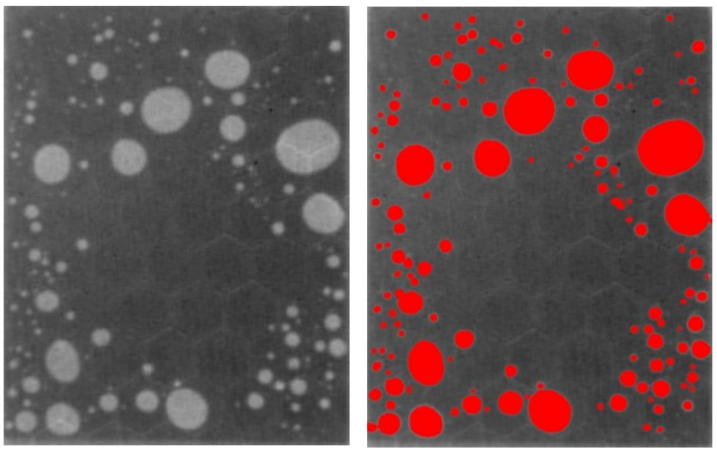

Figure 2. Raw X-ray image of module (left) and processed image (right).

Photoshop using the fill tool with the following threshold settings: 35, 27, 20, 13, 5. Higher thresholds were used for large voids with sharply contrasted edges, and lower settings were used for voids with blurred edges and lower contrast. The variance due to manual processing was also measured, with an average percent error of 5.6%. This metric was tested by re-processing four of the X-ray images several days after their initial completion, and comparing the void ratio to the original copies.

Next, the forward voltage drop at I_f = 50 mA was measured across several diodes from 15°C to 90°C. From these measurements, a second-order polynomial fit was generated. This allowed the junction temperature to me measured by sending a 50 mA sensing current through the diode.

After this, the transient thermal behavior of the diode was measured. The samples were secured to a cold plate, and a large heating current was applied for a duration of 200 seconds. Each module was tested with a heating current of 5, 10, 15, 20, 22, and 24 A. After the heating current was disabled, a sensing current was applied, and the junction temperature was measured through the forward voltage at logarithmically spaced time intervals from 200 µs to 200 s. The data before 200 µs was not included due to electrical transient effects of the diode, and instead data was fitted to this region through the assumption that the temperature is approximately linear with the square root of time during the first 500 µs.

Mathematical Analysis

The first step of the analysis was the transformation from the cooling curve data to a heating curve. This requires the assumption that the thermal system is linear and time-invariant (LTI). The property of linearity approximately holds in this case, as the total change in the thermal resistance from the 5A test to the 24A test was always less than 10% for all modules and all sampling times. Time-invariance also holds because the thermal system does not undergo any substantial change during the thermal testing procedure. The transformation itself is simply a reversal of the data points, so that the lowest temperature occurs first.

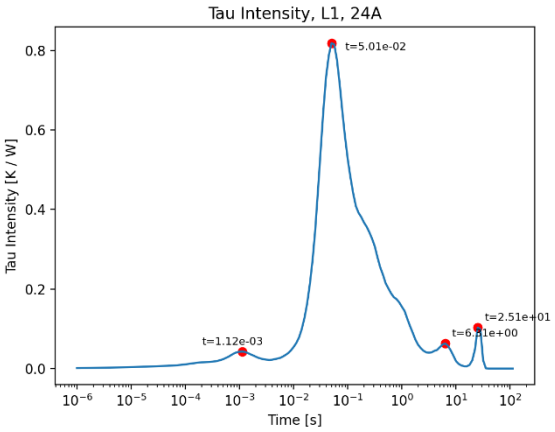

Figure 3. Time constant spectrum with peaks identified.

Next, the time constant spectrum was calculated using the *T3ster Master* software, which uses the method outlined by V. Széleky in [7]. This is the first step of the calculation of the structure function, however the time constant intensity spectrum does not require the assumption of a 1-D model of heat flow, and so can be used with greater validity. The time-constant spectrum describes how the system responds to the heating current in terms of a sum of exponential terms. Peaks in the time constant spectrum roughly correspond to points in time where the heat flux reaches a layer with higher thermal resistance. The first peak in Figure 3 corresponds to the thermal response of the solder layer. Notably, the heat flux does not pass through a layer uniformly as would be the case in 1-D heat flow, which can be seen by the fact that the peaks are not sharp points but are rounded in nature.

In order to most precisely measure the thermal resistance of the solder layer, the optimal time of sampling should occur at some point after the first peak. This is because at exactly one time constant, the heat flux through the solder layer is still well below its maximum value, and so the measurement will be more sensitive to noise. Instead, the measurement should more accurately be taken in the range of

3-5 multiples of the time constant. At this point, the heat flux will be near its steady-state value in the solder layer, while still not fully conducting through the lower unwanted layers.

In order to pin down exactly when the thermal resistance should be measured, the derivative of the cooling curves are used. This method is an adapted version of the The theoretical justification for this method is that, if the voids in the solder layer were to have any impact on the thermal resistance, the Zth curves should begin to deviate from the average once the heat flux reaches the solder layer. In order to clearly see when the curves begin to deviate, the time derivative can be used. As shown in Figure 4, the curves begin to significantly deviate around the 1-2 ms mark, matching the previous analysis from the time constant spectrum plot. Thus, in order to get a full picture of the total thermal resistance of the solder layer, the sampling should occur when the graphs re-converge at approximately 10 ms. The convergence of the graphs indicates that the heat flux has nearly reached its steady-state value within the solder layer but has not yet fully reached the other sources of thermal variance such as the cold plate interface.

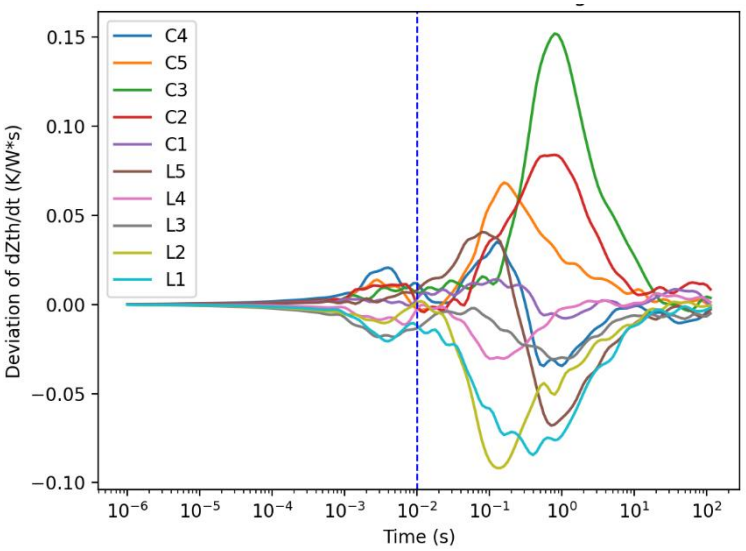

Figure 4. Graph of $\frac{dZ_{th}}{dt}$ of each sample, filtered and normalized with respect to the average of $\frac{dZ_{th}}{dt}$ across all samples.

In combination, the time constant spectrum and the derivative deviation paint a clear picture of what time the solder layer is able to be measured most accurately. Neither of these methods rely on a 1-D assumption of heat flow, and so they are more broadly applicable to

Results

After performing the operations outlined, the relationship between the void percentage and the thermal resistance is taken at t=2 ms, 5 ms, and 10 ms, and is shown in Figure 5.

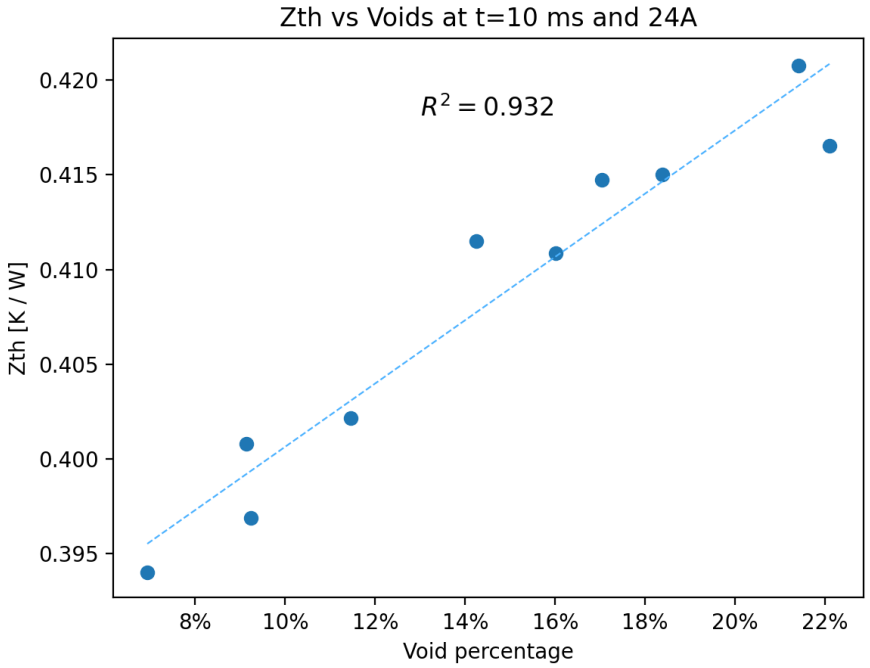

Figure 5. Correlation between voids and thermal resistance at 10 ms.

This result confirms the fact that there is a strong positive correlation between thermal resistance and void percentage. This is in agreement with the majority of published literature [2][3][4]. Over the range of void percentages tested, it was found that a linear fit provided an adequate model for the relationship between thermal resistance and the void percentage. However, modules with extreme void percentages would likely deviate from this linear trend, as shown in [5]. It is also important to note that the total change of

thermal resistance was observed to be about 0.025 K/W.

Conclusion

Based on the data presented above, it appears that while there is a strong correlation between thermal resistance and the void percentage, the relatively small absolute change of about 0.025 K/W indicates that from a thermal perspective, it may not be worthwhile to minimize voids at all costs. In general, void minimization will cause a greater proportional improvement to thermal performance when the other layers of a power module are already optimized for very low thermal resistance. This work also demonstrates the usefulness of a thermal transient interpretation that does not rely upon a 1-D heat flow assumption. Further work on this topic will consist of additional samples with more reflow profiles and solder types, as well as a measurement of the relationship between thermomechanical fatigue and voids through the use of an accelerated lifetime test.

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