Impact of Solder Voids on Power Module Thermal Resistance Using Transient System Analysis

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Why do we care about Thermal Resistance?

High thermal resistance = large temperature difference needed to conduct losses

$$R_{th} = \frac{\Delta T}{P}$$

Excess heat leads to semiconductor or package failure

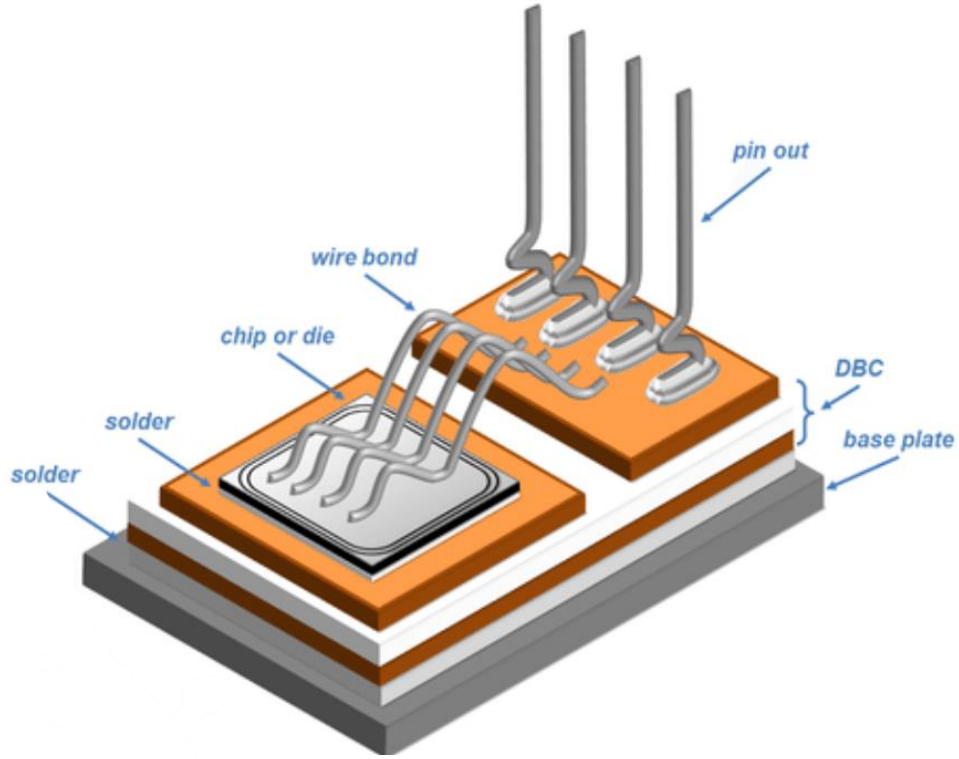


Fig 1. General Layout of Power Module. [1]

Lowering Rth allows for…

Cheaper / smaller cooling equipment

OR

Higher power output

OR

Higher reliability and lifetime

Void Percentage Calculation

Fill Tool Method

1. Capture Xray image of solder
2. Import into Photoshop
3. Use the fill tool to select voided areas*
4. Calculate the number of red pixels vs total pixels

*Fill Tool Threshold settings: 35, 27, 20, 13, 5. Use high settings for large voids and voids with highly contrasted edges.

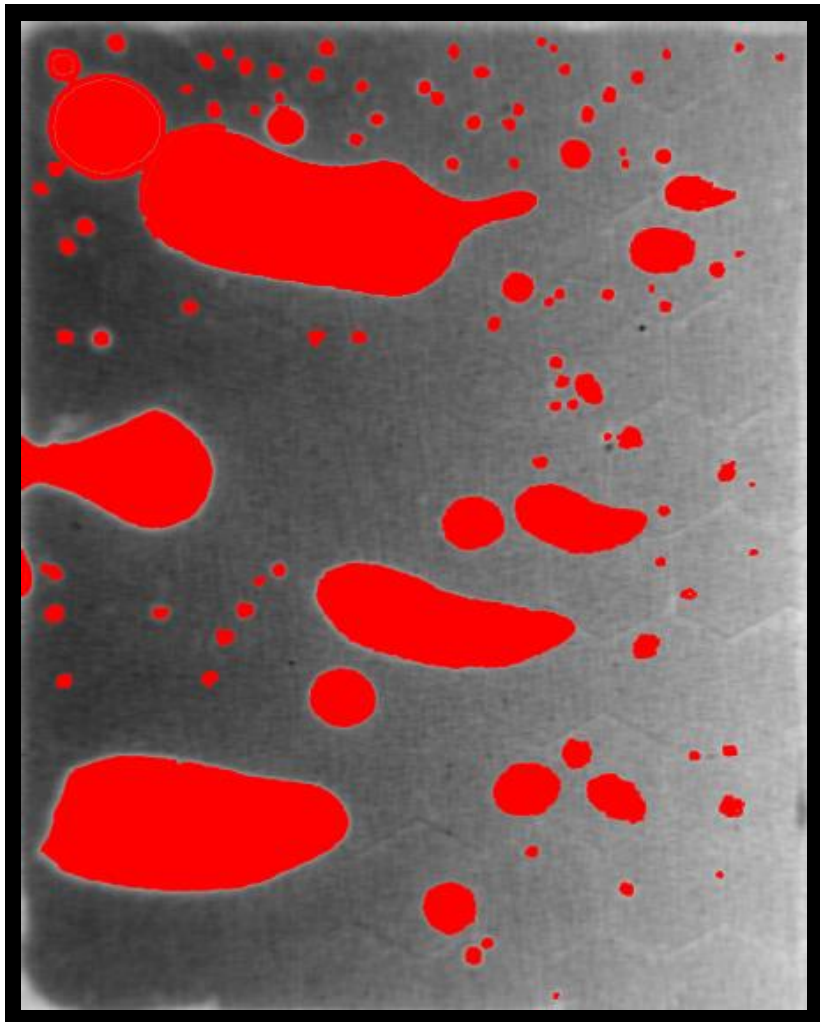


Fig 3. Selection of voided areas using Fill Tool method.

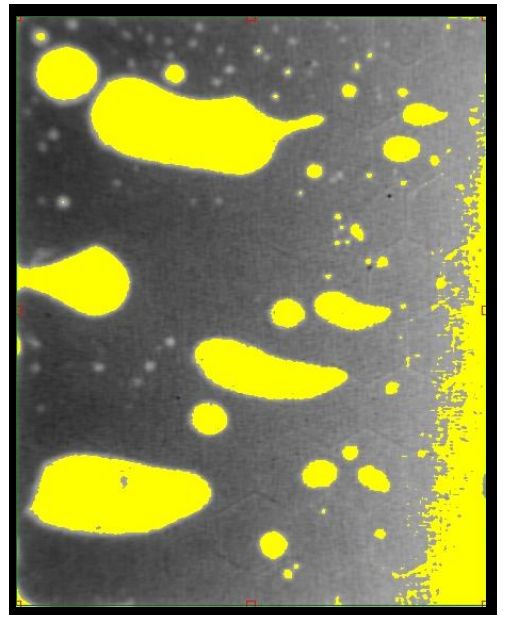


Fig 4. Void selection with Threshold method.

Traditional threshold method susceptible to chip tilt errors

The Experiment

Hypothesis

Voids cause an increase in the thermal resistance of a power module.

Should be predicted by the equation:

$$R_{th} = \beta \cdot \frac{1 - \alpha v}{(1 - v)^2} + R_{ext}$$

α, β, R_{ext}:	Model parameters
v:	Void percentage
R_{th}:	Predicted thermal resistance

Should be able to be modeled as an LTI system:

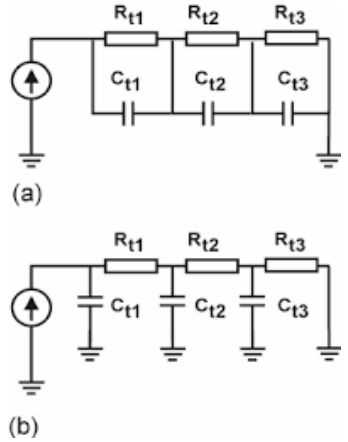


Fig 5. Foster network (a) and Cauer network (b) can be used as representations of LTI thermal systems [2].

Sample Creation

10 Samples

- SAC 305 solder paste
- ‘X’ shaped stencil with 100um thickness
- Reflow in convection oven: Manncorp MC 301
- Two reflow profiles used (see appendix)
- PCB surface metallization: bare Cu

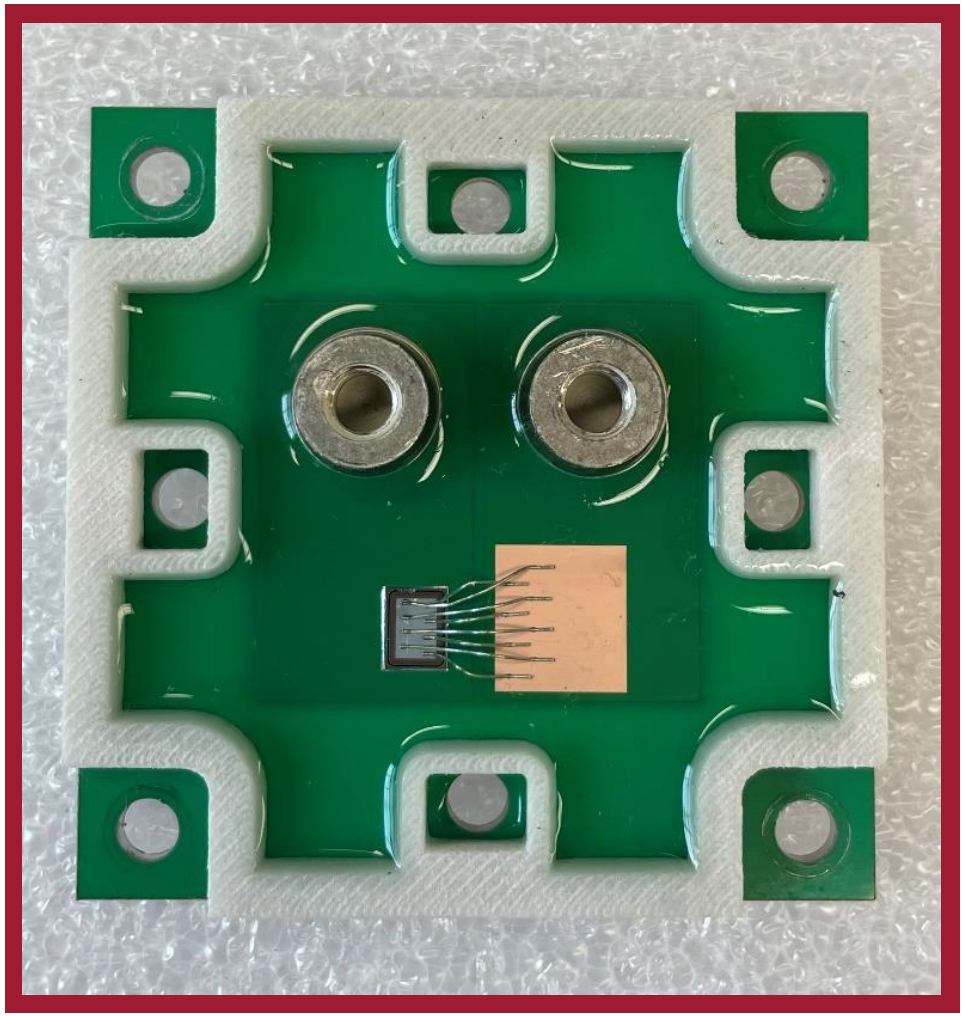
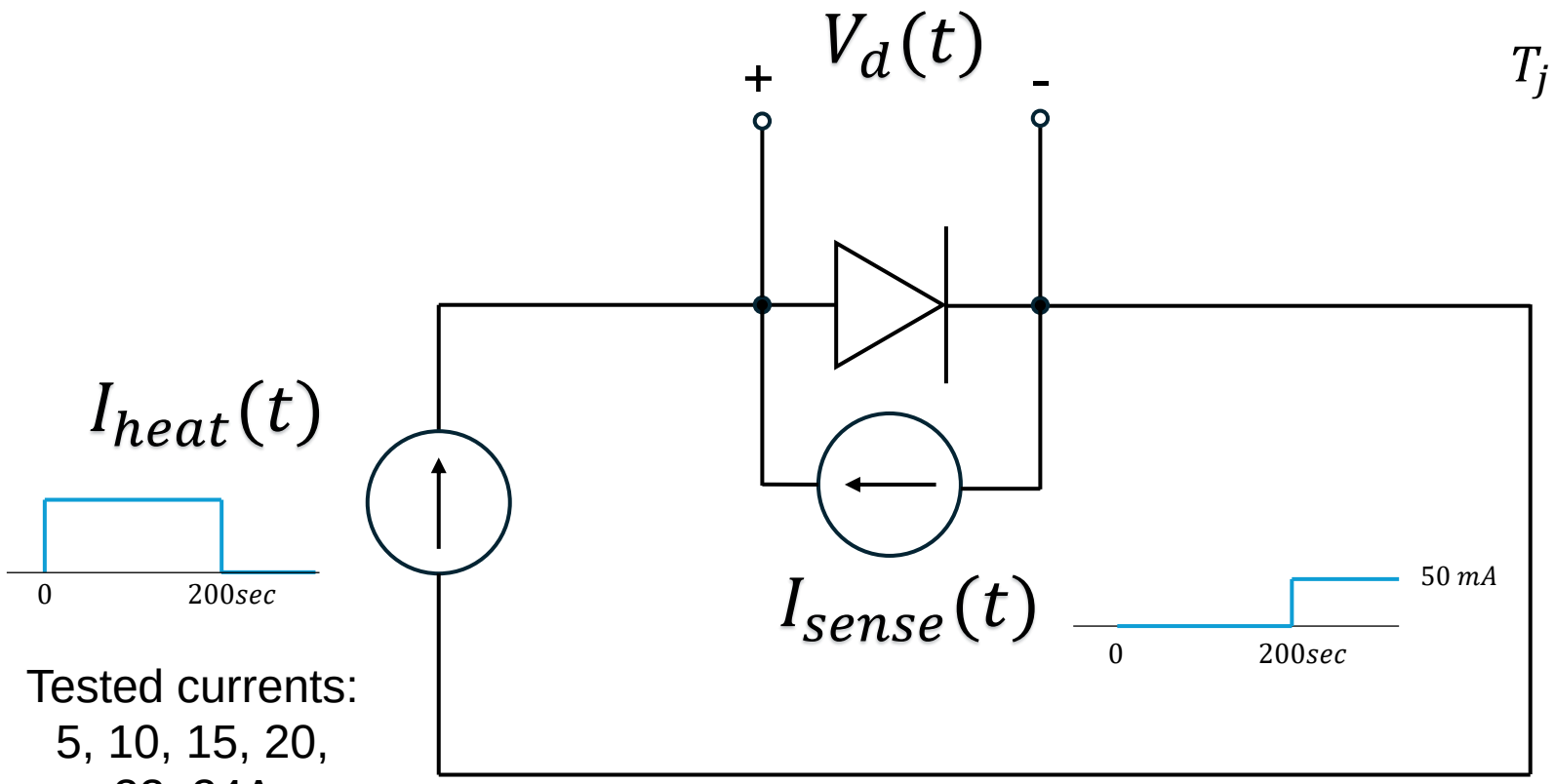


Fig 6. Test sample construction.

Diode Information:

- Model: VS-4FD198H06A6BC
- Size: 5.03mm X 3.35mm
- Rated current: 50A

Rth Test Setup

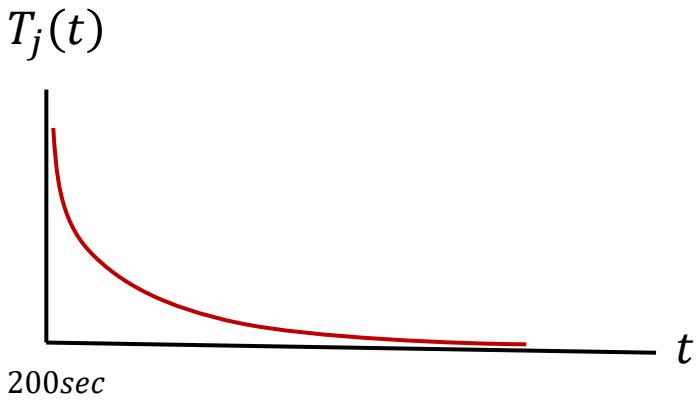


Tested currents:
5, 10, 15, 20,
22, 24A

Diode Junction Temperature Calculation

$$T_j(t) = -227V_d(t)^2 - 241V_d(t) + 247$$

Example Cooling Curve



Postprocessing: Extraction of Heating Curve

Goal: Given a cooling curve, calculate the heating curve

Assumption 1

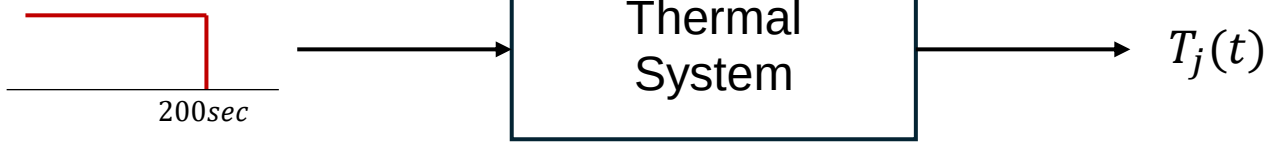
Thermal system is linear and time-invariant (LTI)

Assumption 2

System reaches steady-state within 200 seconds

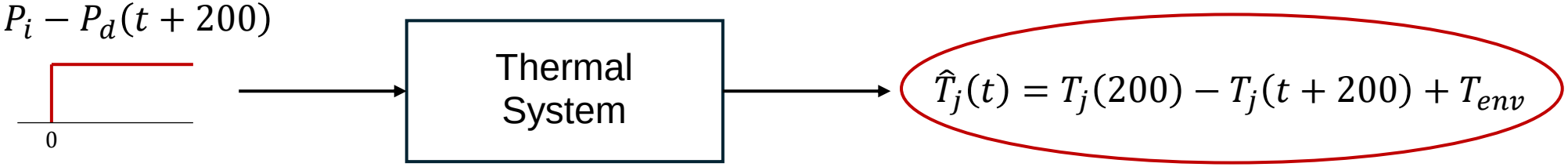
Cooling

$$P_d(t) = I_{heat}(t) * V_d\ (t)$$



Heating

$$\hat{P}_d(t) = P_i - P_d(t + 200)$$



Postprocessing: Tau Intensity Calculation

Increasing Accuracy

Single Element

Step response

$$T(t) = R * (1 - e^{-\frac{t}{\tau}})$$

Equivalent circuit

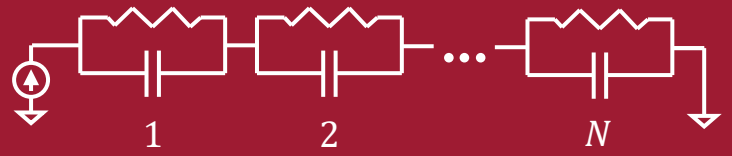
$$\tau = RC$$

Lumped Element

Step response

$$T(t) = \sum_{n=1}^{N} R_n * (1 - e^{-\frac{t}{\tau_n}})$$

Equivalent circuit



Continuous

Step response

$$T(t) = \int_0^{\infty} R(\tau) * \left(1 - e^{-\frac{t}{\tau}}\right) d\tau$$

Equivalent circuit

← Using $\hat{T}_j(t)$, solve for the continuous Tau Intensity function $R(\tau)$ using the method shown in [4].

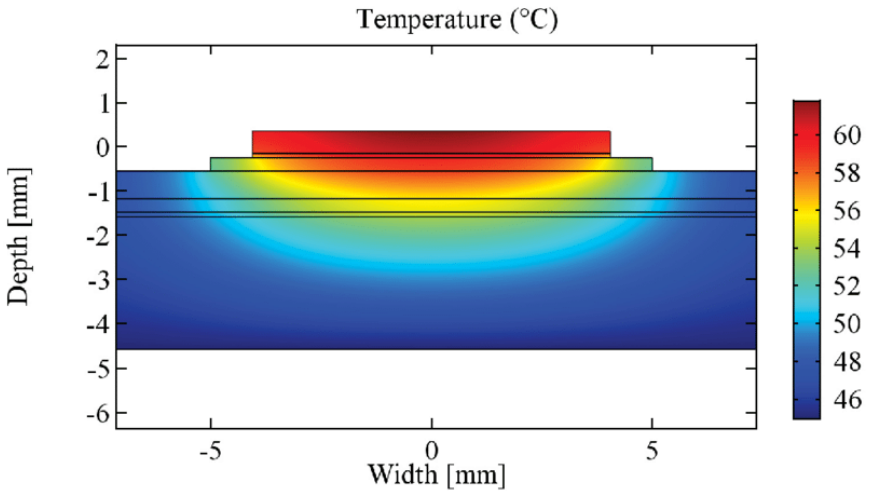


Fig 7. Example diagram of heat flow through a power device [3].

Postprocessing: Tau Peak Identification

Purpose of Tau Intensity

- Peaks of the tau intensity plot correspond to high R and low C relative to the surrounding region
- The first tau peak (1.12 ms) corresponds to the first material junction from the chip to the solder layer
- Thus, measuring Zth at ~1.12 ms should give more accurate measurements than in steady-state

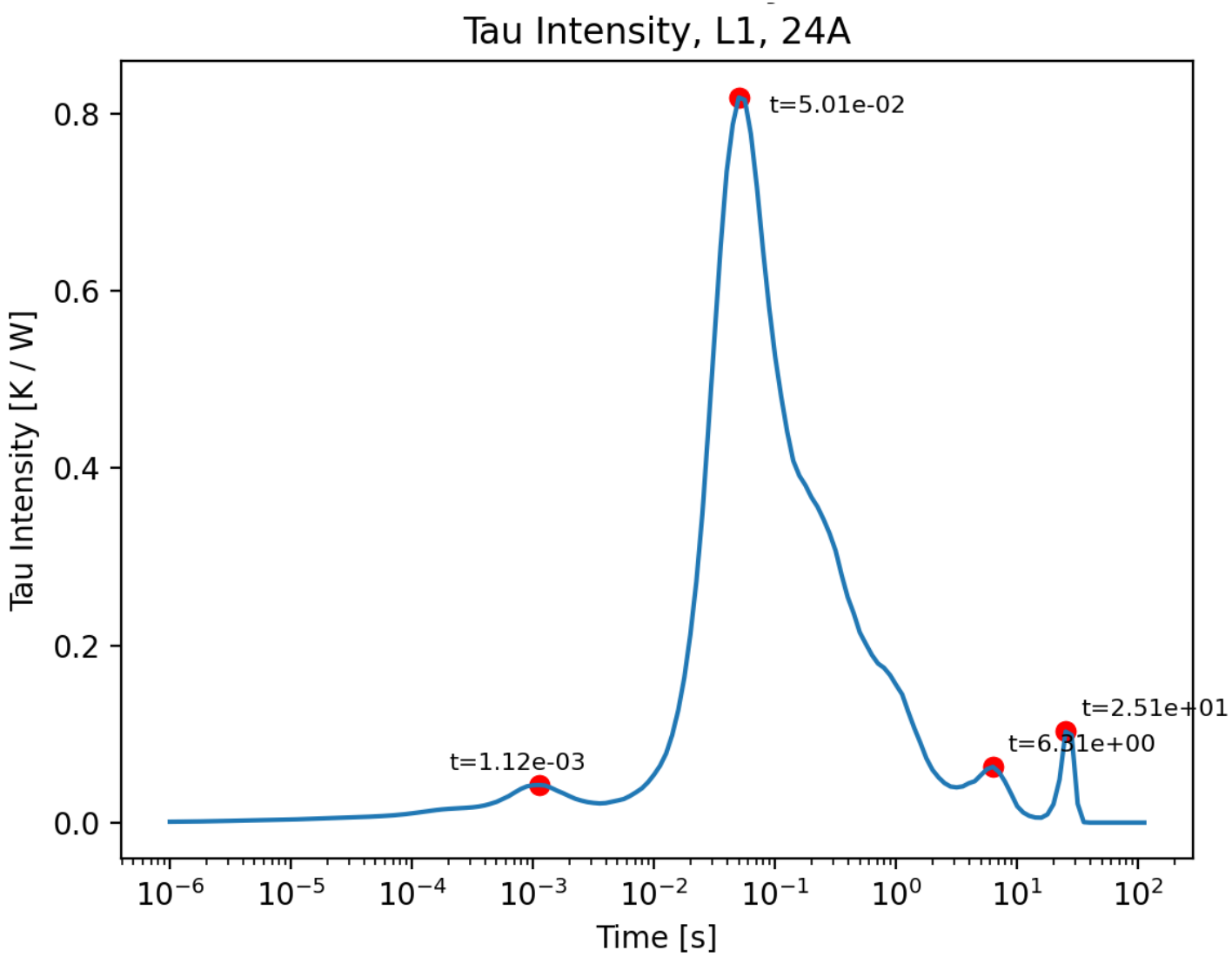


Fig 8. Plot of Tau Intensity vs time, with peaks identified.

Results: First Tau Peak Distribution

Where does the first peak occur most often?

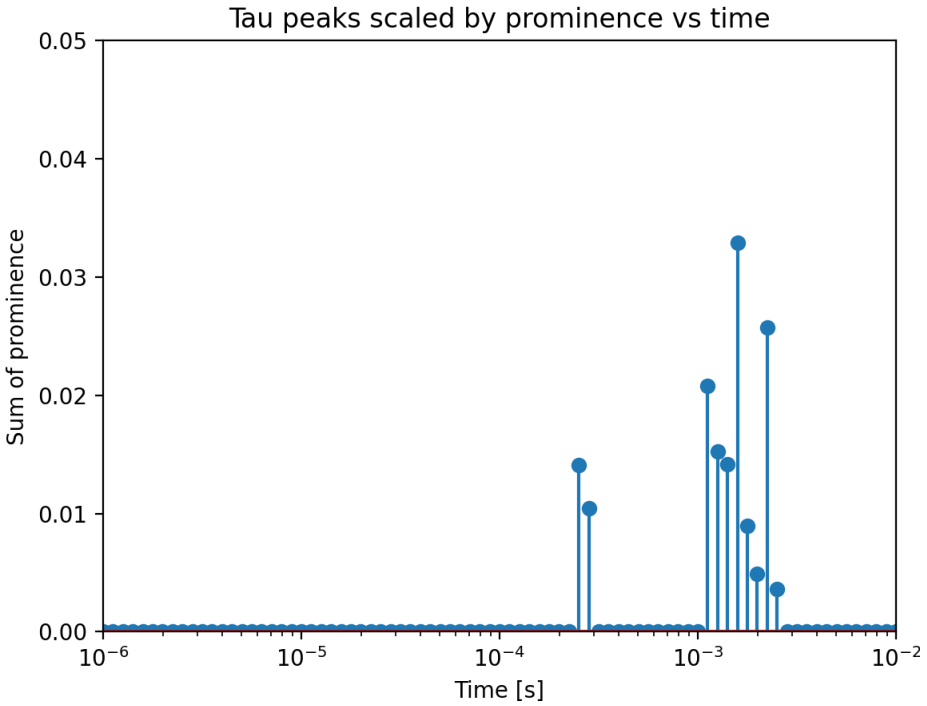


Fig 9. Histogram of all first tau peak times, scaled by how prominent the peak is.

Does the time of the first peak have a correlation with the void percentage?

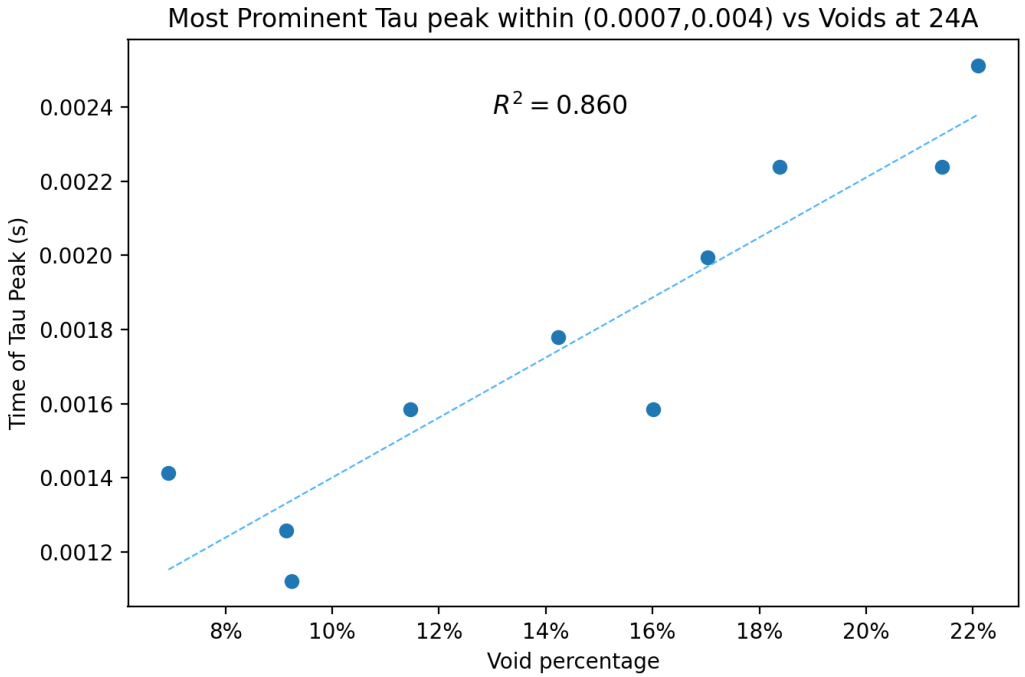


Fig 10. Linear correlation of the time of the tau peak to the void percentage

Results: Zth(t) for t = 1.5 ms

Model fit ($\alpha = 1.51, \beta = 0.138, R_o = 0$)

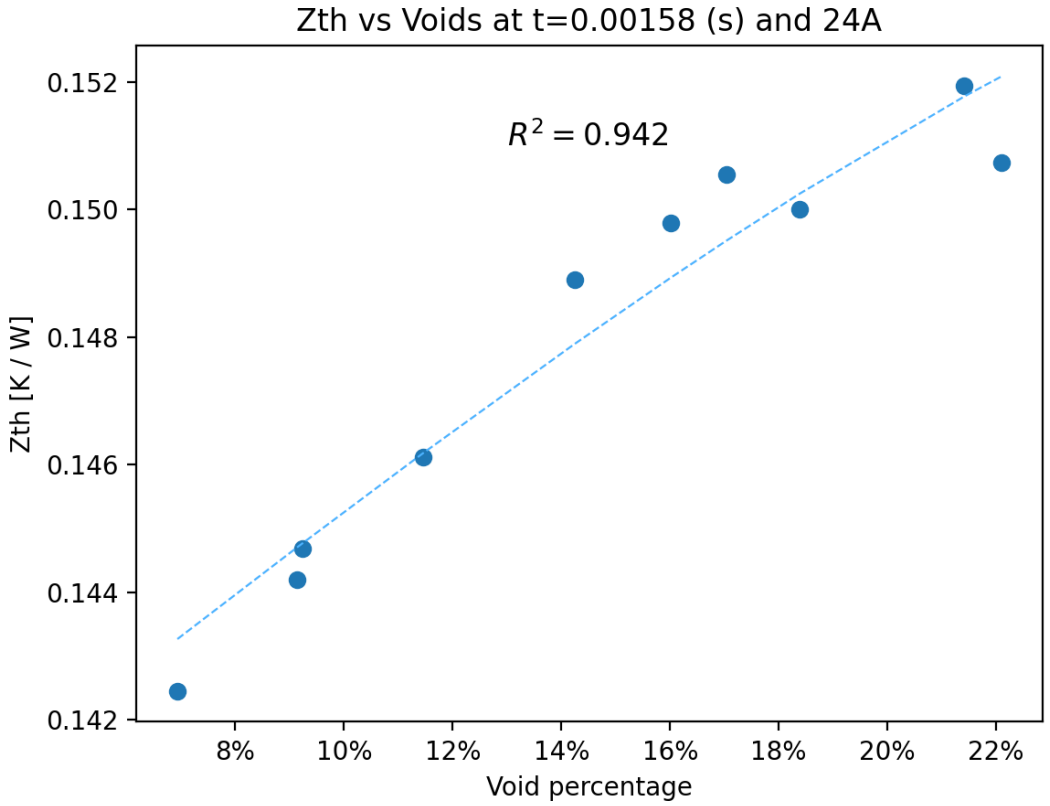


Fig 11. Zth vs Voids at 1.58 ms with model fit

Linear fit

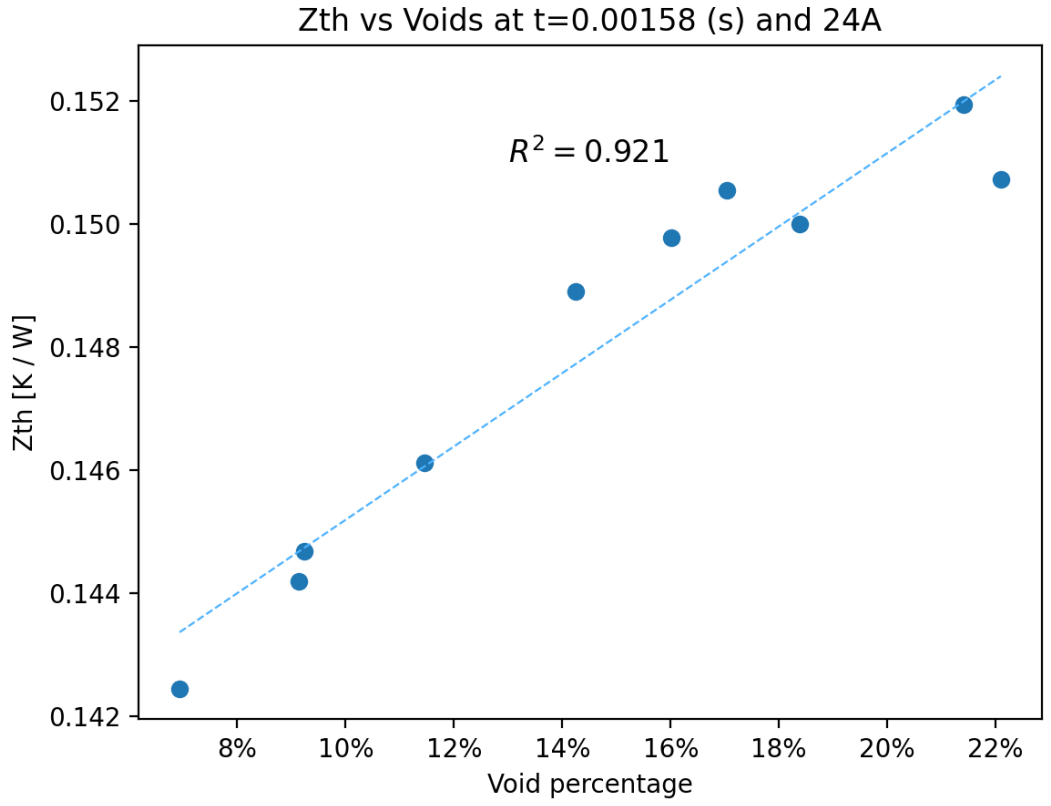
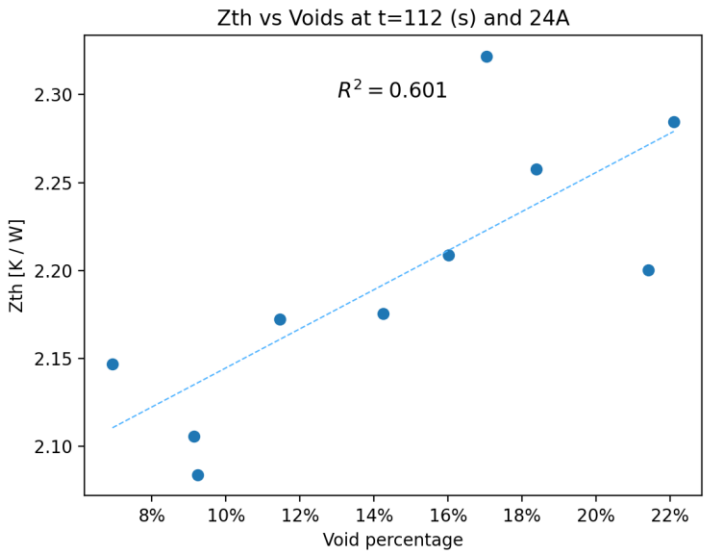


Fig 12. Zth vs Voids at 1.58 ms with linear fit

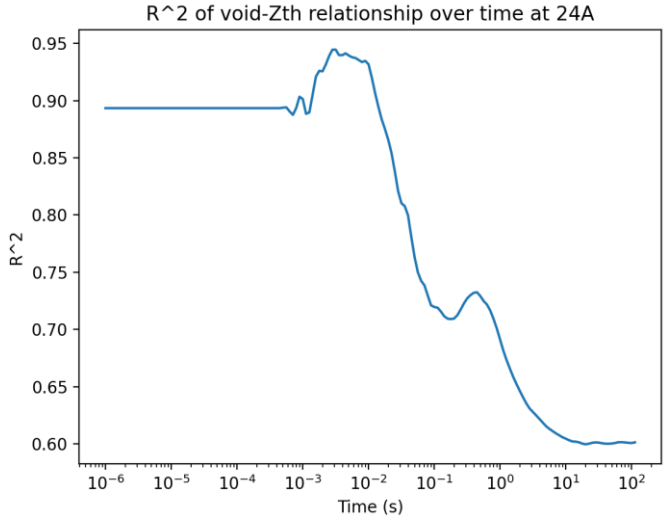
Results: Zth(t) Correlation at Non-Peak Times

What does Zth look like near steady-state?



Much weaker correlation due to variable thermal resistance of layers between the solder and heat sink

At what time does the void percentage have the highest correlation with Zth?



Peaks at ~3 ms, close to the predicted time constant associated with the chip-to-solder interface!

Results: Is the Thermal System Truly Linear?

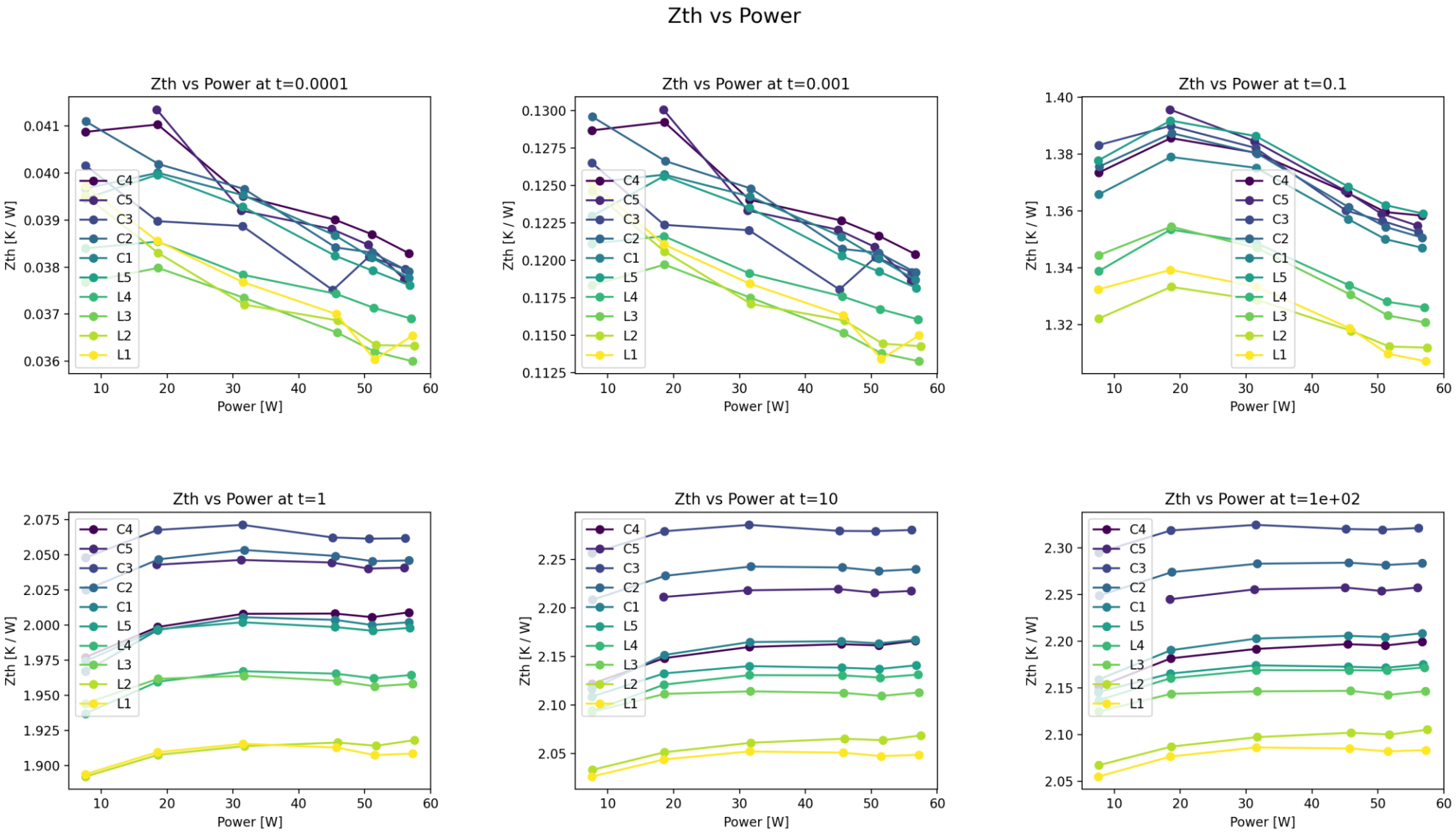


Fig 14. System linearity check by measuring Zth at several values of applied power, as well as at various times.

Results: Power Cycling

Cycling Conditions:

- Heating current: 24A
- Failure mode: $\Delta T + 20\%$ OR $\frac{\Delta T}{\Delta P} + 10\%$
- Cause of failure: solder layer fatigue
- Initial ΔT: 109-116 °C
- On-time: 1 sec
- Off-time: 1 sec

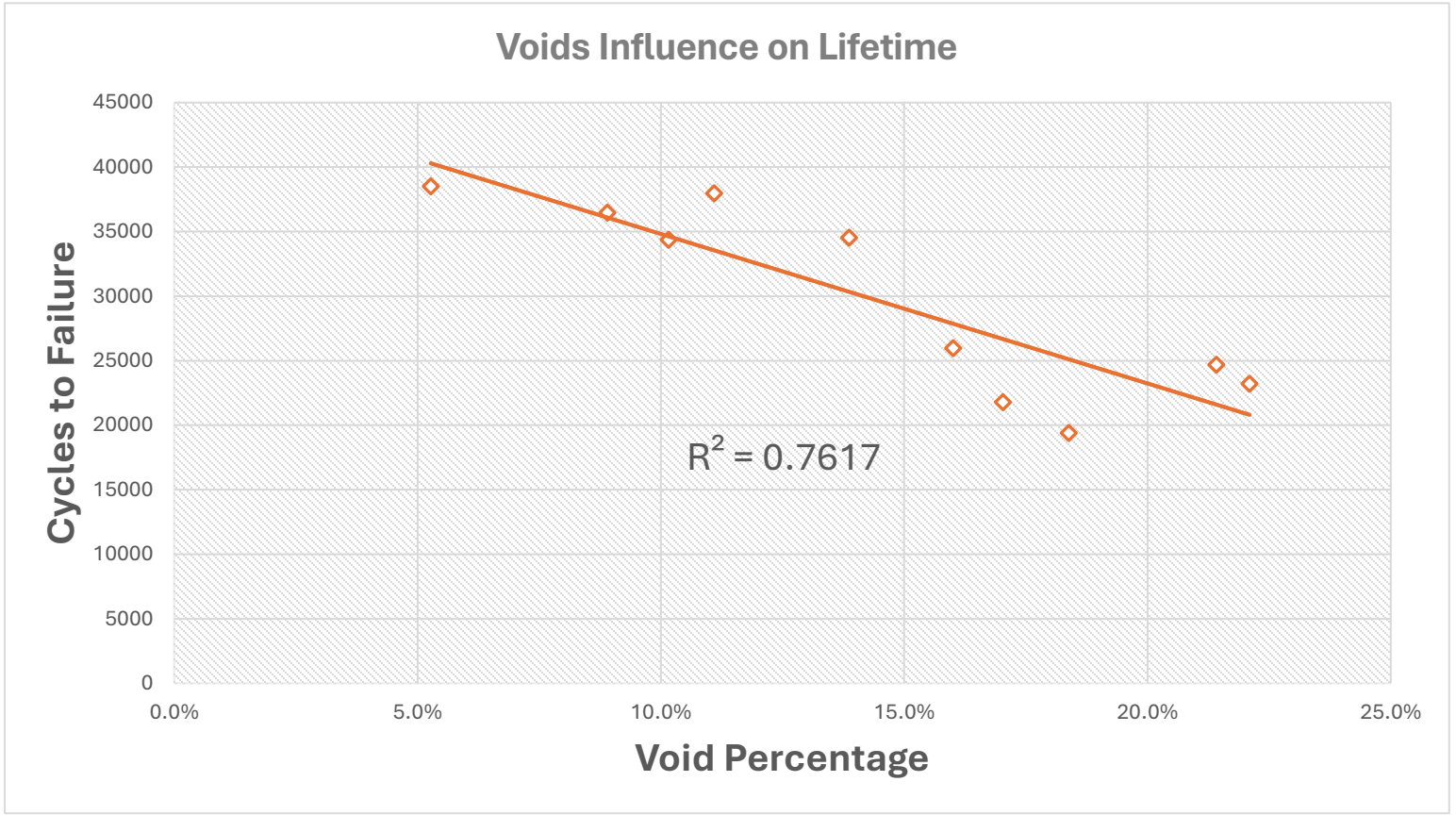
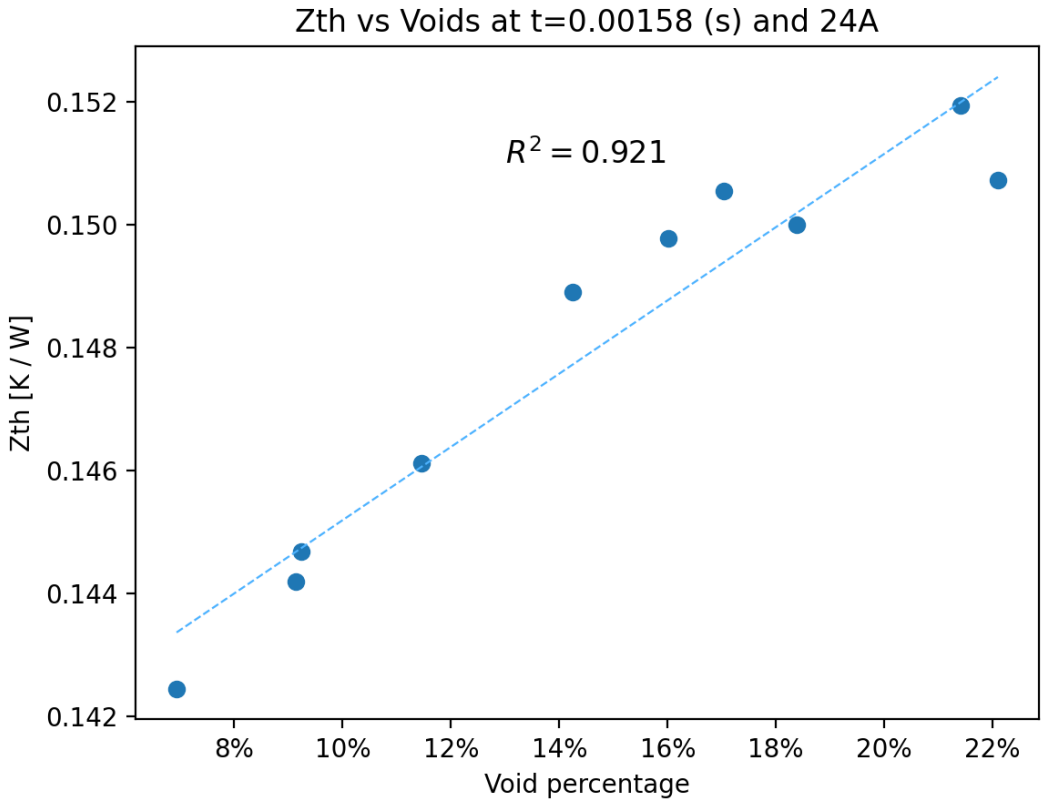


Fig 15. Power cycling results, showing a negative correlation with void percentage.

Important Results and Discussion

Voids have a distinct effect on thermal resistance, but the absolute change in Rth of the whole package is relatively small.



Voids cause a significant decrease in the lifetime of the solder layer during power cycling.

While our model is able to capture the data trends, it is unclear whether it is truly a good indicator of thermal resistance.

The methodology used for postprocessing appears to be able to accurately measure the thermal resistance of the solder with minimal influence from other layers.

Future Work

Processing / Computational

- Finite Element Simulation as a third point of verification for the time constant associated with the chip-to-solder interface
- Accurate implementation of structure function method and comparison to the method presented here
- Generalization of postprocessing to include arbitrary / pulsed heating current waveforms
- Create a general tool / metric to analyze the effect of void size and position

Experimental

- More samples! See if the model is truly accurate, and also examine results for different solder alloys, surface metallizations, and chip types.
- Test increased PCB thickness to determine if this causes the first tau peak to increase in prominence

Acknowledgements

- Dr. Nicholas Baker

References

[1] Cosiansi, Fernando. (2016). ISPET: Interface Sintering Process Enhanced Technology. 10.6092/polito/porto/2643767.
[2] Zhou, Zhongfu & Holland, Paul & Igic, Petar. (2008). Compact thermal model of a three-phase IGBT inverter power module. 167-170. 10.1109/ICMEL.2008.4559249.
[3] Bjørn Jørgensen, Asger & Christensen, Nicklas & Dalal, Dipen & Sønderskov, Simon & Bęczkowski, Szymon & Uhrenfeldt, Christian & Munk-Nielsen, Stig. (2017). Reduction of parasitic capacitance in 10 kV SiC MOSFET power modules using 3D FEM. 10.23919/EPE17ECCEEurope.2017.8098962.
[4] Vladimir Székely, Tran Van Bien, Fine structure of heat flow path in semiconductor devices: A measurement and identification method, Solid-State Electronics, Volume 31, Issue 9,1988, Pages 1363-1368, ISSN 0038-1101, https://doi.org/10.1016/0038-1101(88)90099-8. (https://www.sciencedirect.com/science/article/pii/0038110188900998)

Questions?