Solder Void Impact on Power Device Thermal Impedance using Transient Thermal Analysis

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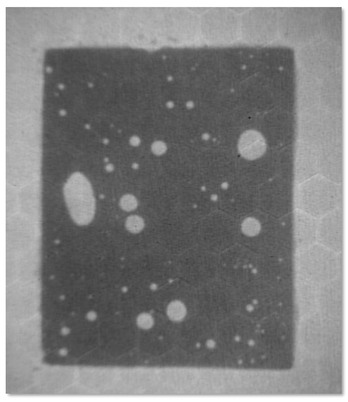
Nathan Carlson | Nick Baker | The University of Alabama
ncarlson@crimson.ua.edu, nbaker2@ua.edu

Motivation

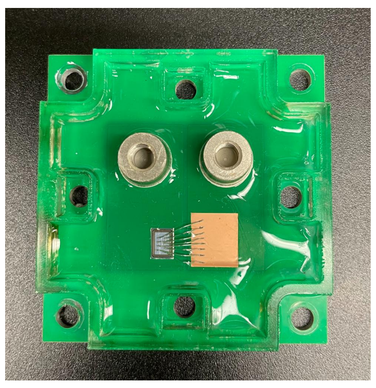
Solder voids underneath the chip require expensive equipment to remove. This is especially true for mass production and research labs.

Thermal impedance and **lifetime** are two key metrics of a power device.

At present, there is a relative scarcity of direct experimental evidence between voids and these key metrics.



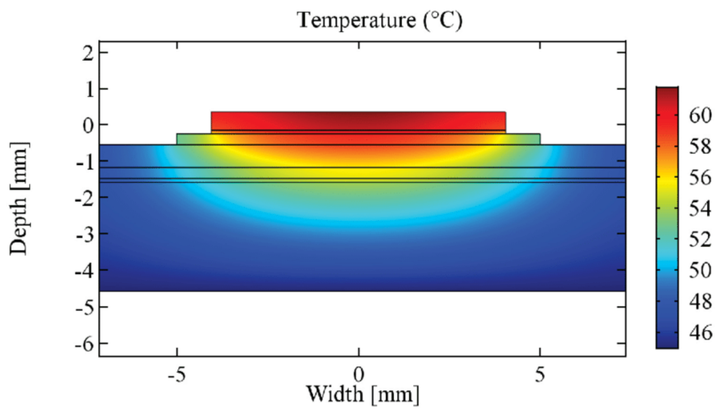
Void percentage = 100% * voided area / total area



Diode test module

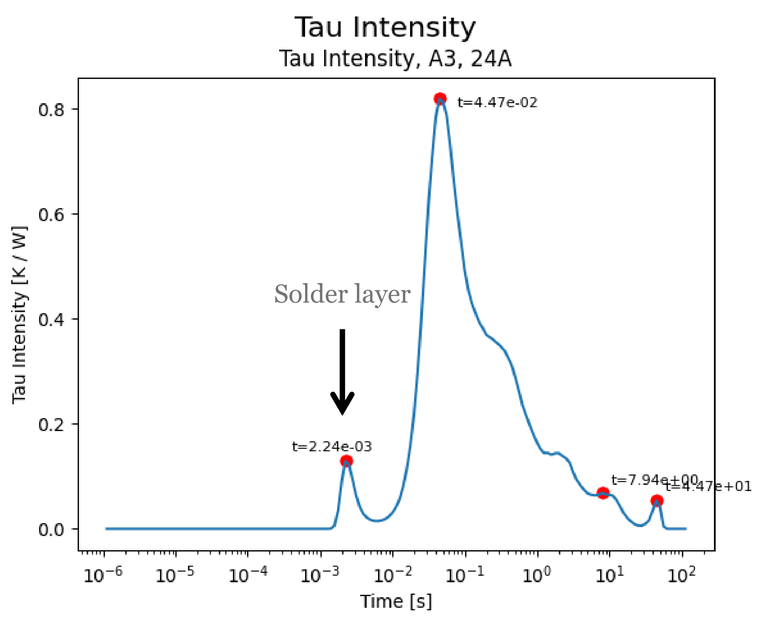
Tau Intensity Technique

Problem: The thermal resistance of the solder layer is difficult to isolate due to the variable resistance of other layers.

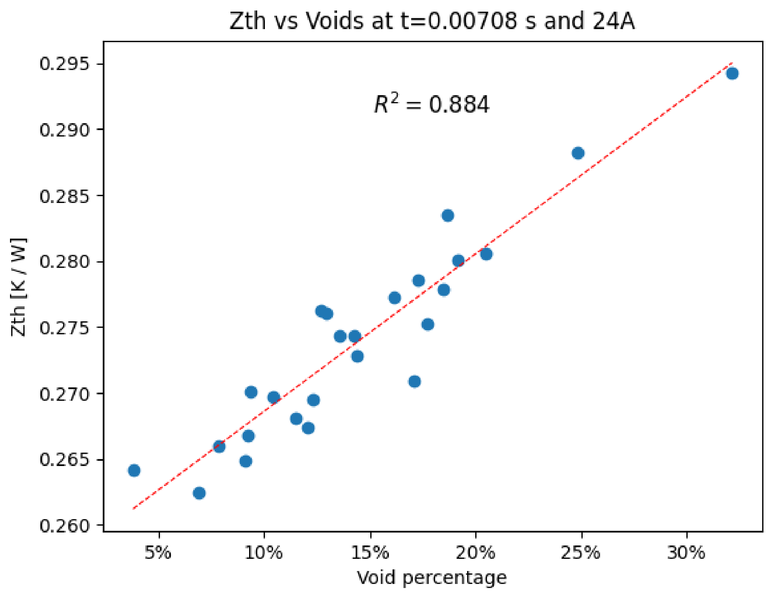


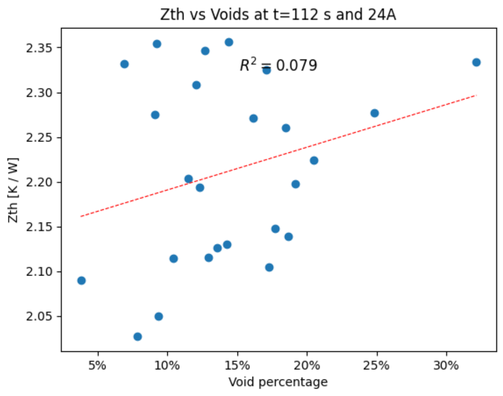
COMSOL simulated image from [1].

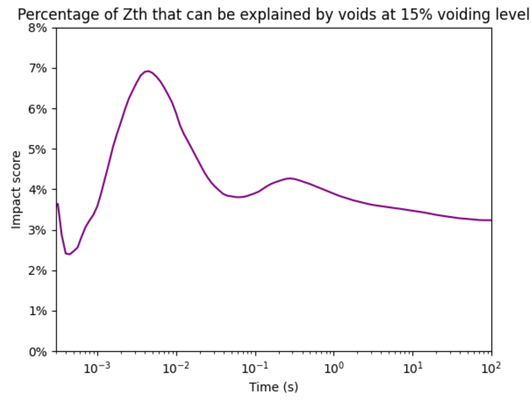
Solution: The impedance can be measured a short time after applying a heating current. This time should be a point when the heat flux through the solder is high but has not fully reached the lower layers. The Tau Intensity plot can help to select this time (about 2-5 multiples of the solder layer's time constant).



Thermal Impedance Results

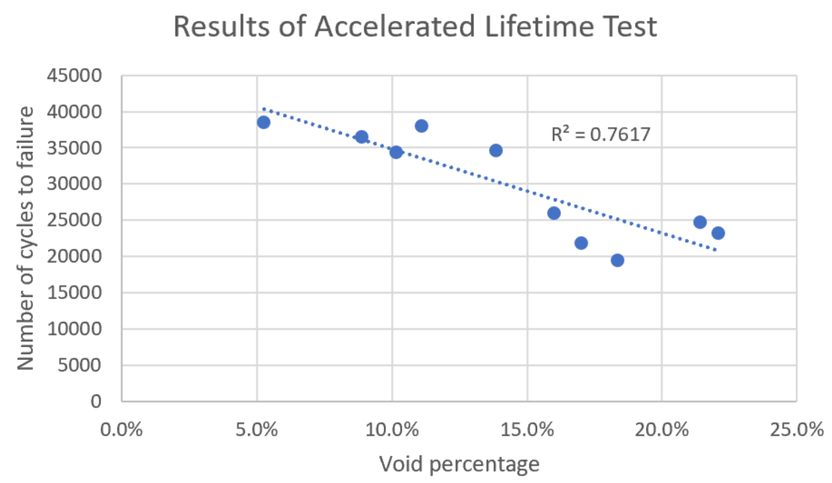




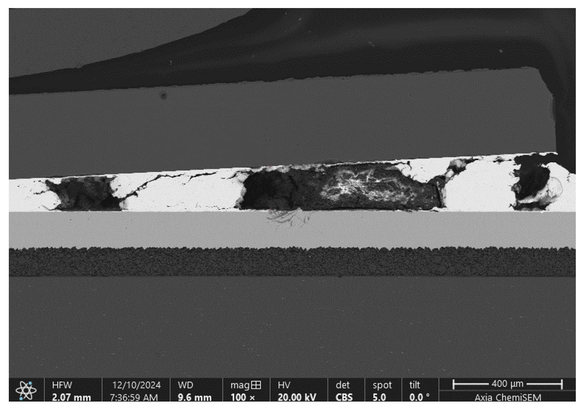


Voids have the most significant impact on thermal impedance on **short timescales**. This indicates that from a thermal perspective, void removal would help to protect against thermal transient conditions such as a temporary short circuit, but that voids do not have a strong impact on the steady-state thermal resistance.

Lifetime Results



Voids accelerate the growth of solder cracks. Modules with low voids showed much longer lifetimes.



References

[1] Bjørn Jørgensen, Asger & Christensen, Nicklas & Dalal, Dipen & Sønderskov, Simon & Bęczkowski, Szymon & Uhrenfeldt, Christian & Munk-Nielsen, Stig. (2017). Reduction of parasitic capacitance in 10 kV SiC MOSFET power modules using 3D FEM. 10.23919/EPE17ECCEEurope.2017.8098962.