Solder Void Impact on Power Module Thermal Resistance using Transient Thermal Analysis

Nathan Carlson, Nick Baker
The University of Alabama, Tuscaloosa, USA, ncarlson@crimson.ua.edu

Summary

This research utilizes a customized thermal transient analysis method for the purpose of identifying the thermal impact of solder voids in power modules. At present, most of the existing experimental transient thermal analysis techniques focus on developing a 1-dimensional Cauer network thermal model. However, this model neglects to consider the effects of heat spreading, which is a highly relevant effect when considering heat flow from the solder layer to the DBC. Because of this, models based upon a 1-D assumption of heat flow have been shown to have significant error when compared to a 3-D finite element simulation[1].

In order to address this issue, the research presented here utilizes an adapted interpretation of the time constant spectrum technique[2]. In addition, we also provide a secondary source of understanding through a derivative deviation technique, which provides a measure of the point in time where the thermal impedance is not consistent across the samples[3]. Both of these methods are applicable to a 3-D heat flow model, which includes the effects of thermal spreading. These methods are used to more accurately measure the thermal effects of the voids in the die-attach solder layer.

Motivation

In the continual effort to improve the thermal performance of modern power modules, manufacturers have placed a heavy emphasis on the removal of voids in the chip-attach solder layer. However, void reduction procedures often involve a vacuum or pressurized soldering oven, thus increasing the cost of production. Therefore, it is important to gain an accurate understanding of how voids impact the thermal performance of power modules in order to give insight into the optimal level of investment that should be placed into void reduction equipment.

Results

The first piece of data collected were X-ray images of the solder layers of each module, which were subsequently processed and the void content of each was calculated (Fig. 1). Next, thermal data was collected by monitoring the temperature of the modules over time as a heating current was applied. This was used to generate the time constant spectrum, and the peaks were located using a custom script. Peaks in the time constant spectrum roughly correspond to points in time where the heat flux reaches a layer with higher thermal resistance. The first peak in Figure 2 corresponds to the thermal response of the solder layer. Notably, the heat flux does not pass through a layer uniformly as would be the case in 1-D heat flow, which can be seen by the fact that the peaks are not sharp points but are rounded in nature.

In addition, the graph of the deviation of $\frac{dZ_{th}}{dt}$ in Figure 3 shows that the thermal resistance of the modules begins to deviate near the 1-2 ms mark, which agrees with the location of the first peak in Figure 2. This deviation is due to the differing thermal resistances of the solder layers between each module, and so the total difference can be measured by sampling a point in time near 10 ms (dotted blue line in Fig. 3), where the curves re-converge.

The thermal resistance measurement at 10 ms shows a strong correlation between thermal resistance and void count (Fig. 4). At this measurement point, there is approximately a 0.027 K/W difference between the best and worst module.

[1] Q. Li, F. Zhang, Y. Chen, T. Fu, and Z. Zheng, "A junction temperature model based on heat flow distribution in an IGBT module with solder layer voids," *Heliyon*, vol. 10, no. 13, Jul. 2024, doi: 10.1016/j.heliyon.2024.e33625.

[2] V. Székely and T. Van Bien, "FINE STRUCTURE OF HEAT FLOW PATH IN SEMICONDUCTOR DEVICES: A MEASUREMENT AND IDENTIFICATION METHOD," *Solid State Electron*, vol. 31, no. 9, pp. 1363–1368, 1988.

[3] D. Schweitzer, H. Pape, and L. Chen, "Transient Measurement of the Junction-To-Case Thermal Resistance Using Structure Functions: Chances and Limits," in *2008 Twenty-fourth Annual IEEE Semiconductor Thermal Measurement and Management Symposium*, San Jose: IEEE Xplore, 2008, pp. 191–197.

Figures

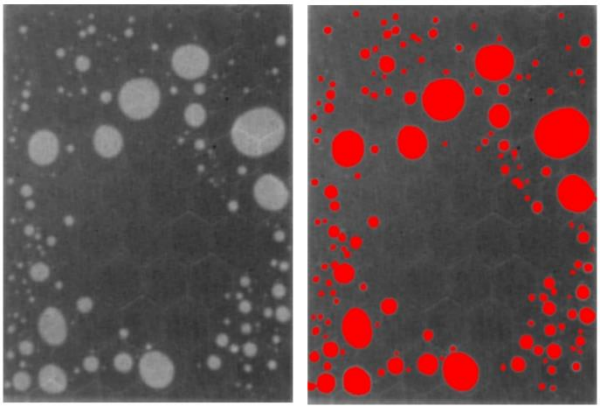

Fig. 1: Raw X-ray image of solder layer (left) and processed image (right)

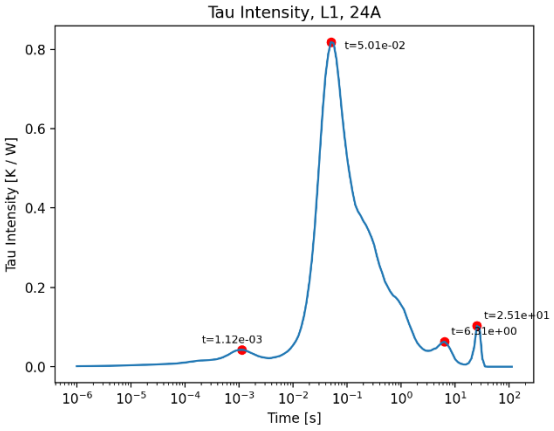

Fig. 2: Time constant spectrum with peaks identified

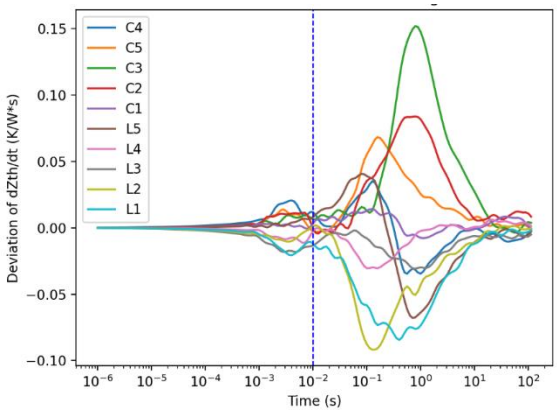

Fig. 3: Graph of $\frac{dZ_{th}}{dt}$ of each sample, filtered and normalized with respect to the average of $\frac{dZ_{th}}{dt}$ across all samples.

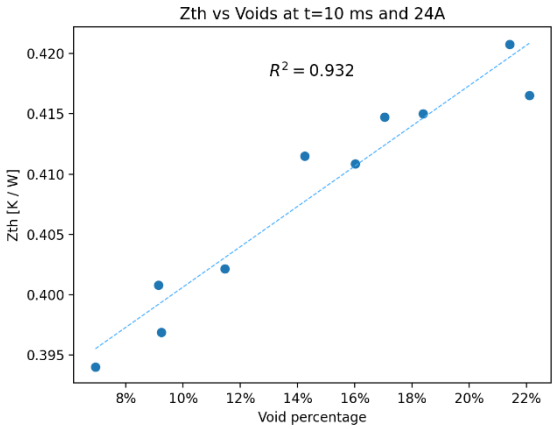

Fig. 2: Correlation between voids and thermal resistance at 10 ms