Solder Void Impact on Power Module Thermal Resistance using Transient Thermal Analysis

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Summary

This research utilizes a customized thermal transient analysis method for the purpose of identifying the thermal impact of solder voids in power modules. At present, most of the existing experimental transient thermal analysis techniques focus on developing a one-dimensional (1-D) Cauer network thermal model. However, this model neglects to consider the effects of heat spreading, which is a highly relevant effect when considering heat flow through the solder layer. Because of this, models based on a 1-D assumption of heat flow have been shown to have significant errors when compared to 3-D finite element simulations[1].

To address this issue, the research presented here utilizes an adapted interpretation of the time constant spectrum technique[2] as well as a derivative deviation method[3]. These methods are used to analyze experimental data on the thermal resistance of sample modules consisting of a single diode. Both methods are applicable to a 3-D heat flow model, which includes the effects of thermal spreading.

Motivation

One of the main methods of void removal is the use of a vacuum or pressurized soldering oven. However, for cost-sensitive applications or low-volume production, these machines can significantly drive up the cost of production. Therefore, it is necessary to accurately quantify the impact of voids on the performance and reliability of power modules. The thermal impact of voids is one such concern; however, most current experimental measurement methods have some level of inaccuracy. An improved method will allow for upgraded decision-making capability when designing solder processes.

Results

The chip used is a 600V/50A power diode, and it was soldered to an aluminum clad PCB with SAC 305 solder and wire bonded using eight 250 μm wire bonds. The first data collected consisted of X-ray images of the solder layers of each module, which were subsequently processed to calculate the void content of each (Fig. 1). Next, thermal data was collected by monitoring the temperature of the modules over time while a 24 A heating current was applied over 120 seconds. The temperature was monitored using the forward voltage of the diode at 50 mA, and the first 200 μs of data was replaced with an estimation that the actual temperature decreases linearly with the square root of time during this period. This was used to generate the time constant spectrum, and the peaks were located using a custom script. Peaks in the time constant spectrum roughly correspond to points in time where the heat flux reaches a layer with higher thermal resistance. The first peak in Figure 2 corresponds to the thermal response of the solder layer. Notably, the heat flux does not pass through a layer uniformly as would be the case in 1-D heat flow, which can be seen by the fact that the peaks are not sharp points but are rounded in nature.

In addition, the graph of the deviation of $\frac{dZ_{th}}{dt}$ in Figure 3 shows that the thermal resistance of the modules begins to deviate near the 1-2 ms mark, which aligns with the location of the first peak in Figure 2. This deviation is due to the differing thermal resistances of the solder layers between each module, and so the total difference can be measured by sampling a point in time near 10 ms (dotted blue line in Fig. 3), where the curves re-converge.

The measurement at 10 ms shows a strong correlation between thermal resistance and void count (Fig. 4). This relationship is much stronger than the correlation at steady state (Fig 6). This serves as an indicator that the transient method allowed the isolation of the solder layer from unwanted variance.

[1] Q. Li, F. Zhang, Y. Chen, T. Fu, and Z. Zheng, "A junction temperature model based on heat flow distribution in an IGBT module with solder layer voids," *Heliyon*, vol. 10, no. 13, Jul. 2024, doi: 10.1016/j.heliyon.2024.e33625.

[2] V. Székely and T. Van Bien, "FINE STRUCTURE OF HEAT FLOW PATH IN SEMICONDUCTOR DEVICES: A MEASUREMENT AND IDENTIFICATION METHOD," *Solid State Electron*, vol. 31, no. 9, pp. 1363–1368, 1988.

[3] D. Schweitzer, H. Pape, and L. Chen, "Transient Measurement of the Junction-To-Case Thermal Resistance Using Structure Functions: Chances and Limits," in *2008 Twenty-fourth Annual IEEE Semiconductor Thermal Measurement and Management Symposium*, San Jose: IEEE Xplore, 2008, pp. 191–197.

Figures

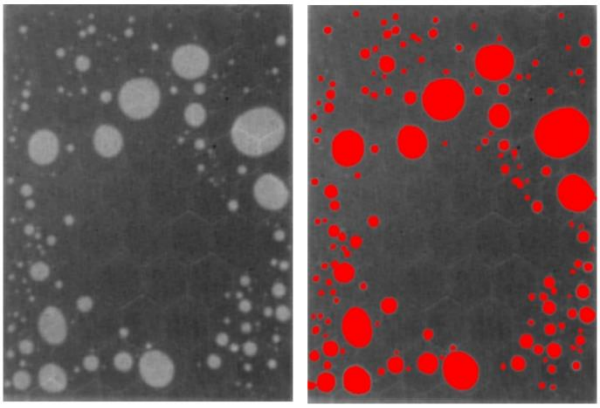

Fig. 1: Raw X-ray image of solder layer (left) and processed image (right)

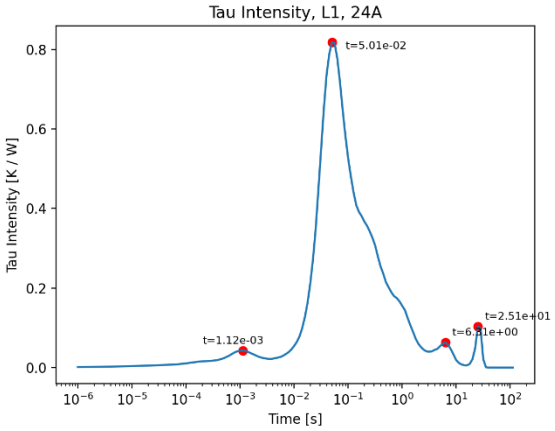

Fig. 2: Time constant spectrum with peaks identified

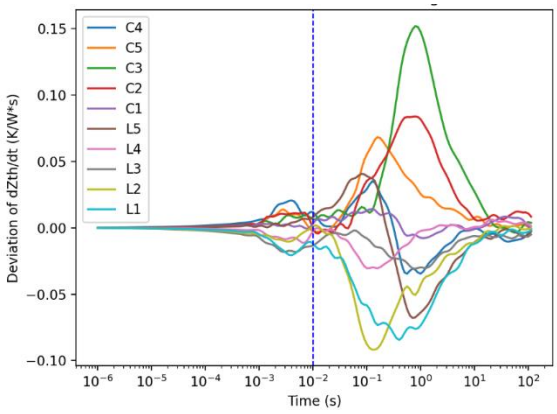

Fig. 3: Graph of $\frac{dZ_{th}}{dt}$ of each sample, filtered and normalized with respect to the average of $\frac{dZ_{th}}{dt}$ across all samples

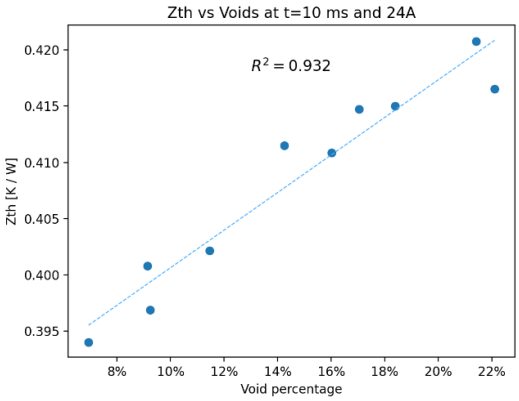

Fig. 4: Correlation between voids and thermal resistance at 10 ms

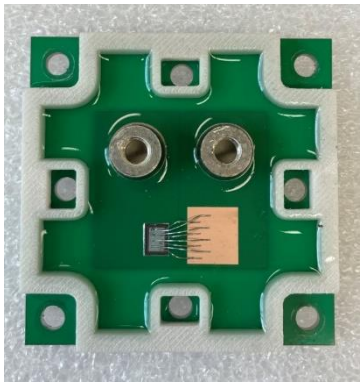

Fig. 5: Test module construction

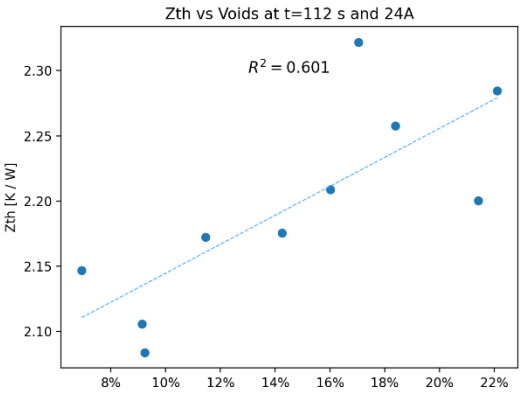

Fig. 6: Correlation between voids and thermal resistance at 112 sec