Multi-Chip Temperature Imbalance of SiC MOSFETs in MOSFET vs. Body-Diode Conduction

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***Abstract*— We use on-chip NTC thermistors to observe the impact of the operating condition on the thermal resistance and chip temperature distribution in a multi-chip SiC MOSFET power module. We find that operating in MOSFET or Body-Diode mode impacts both the thermal resistance and the chip temperature distribution. In one example, Body-Diode operation increases the minimum to maximum chip temperature imbalance from 14.5°C to 30.1°C for the same power dissipation in comparison to MOSFET operation. The junction-to-ambient thermal resistance is also estimated to be 5% higher when measured under Body-Diode operation. The paper describes the on-chip NTC thermistors and provides additional thermal data from various operating conditions.**

Keywords—Temperature measurement, Power MOSFETs, Thermal management, Reliability.

I. Introduction

A. Junction Temperature and Thermal Resistance

The junction temperature (T_J) of a power semiconductor is one of the major design considerations in a power electronic converter. It is directly related to reliability, lifetime, and safe operation. At a minimum, the T_J of a power semiconductor must remain below a maximum temperature to avoid thermal runaway. Secondly, the power semiconductor lifetime is directly linked to the thermo-mechanical fatigue induced by T_J fluctuations during operation [1]. In fact, the T_J fluctuation is by far the most influential parameter in power semiconductor lifetime, with coefficients to the power of between 3.5 to 5.0 depending on the semiconductor type and materials [2, 3] (i.e., doubling the junction temperature swing from 50°C to 100°C can lead to a 32x decrease in lifetime).

The T_J of a power semiconductor is often estimated using electro-thermal models. The semiconductor power loss is combined with the thermal impedance to estimate the T_J. Some manufacturers may provide software to help perform this estimation [4]. In addition, almost all datasheets will provide a Junction-to-Case thermal resistance, and in some cases (particularly in discrete devices) a Junction-to-Ambient resistance when using a standardized heatsink. Electro-thermal models however are prone to errors of up to or greater than ±20% [5]. When using manufacturer models to estimate the maximum junction temperature in multi-chip SiC MOSFET modules, absolute errors have been estimated to be between 25°C to 35°C [4]. This uncertainty leads to oversizing of power electronic systems, which increases weight, volume, and cost.

While the electrical behaviour of a power semiconductor is quantified in the datasheet with respect to temperature and operating condition, the thermal resistance on the other hand is most often provided as a single value. This is despite thermal conductivity being dependent on temperature which can impact the accuracy of thermal models [6]-[8].

In addition, the T_J in power semiconductors is often described as a singular 'virtual' junction temperature which represents a temperature related to the mean temperature of the chip(s) inside the module [9]-[11]. No data is typically provided providing the temperature distribution in a multi-chip module. This leaves further uncertainty if a system designer is concerned with respecting the maximum temperature on the hottest chip within a multi-chip module.

B. Multi-Chip Power Modules

To increase the power capacity of a power semiconductor module, the simplest option is to increase the overall semiconductor chip area. This can be done in two ways. The first is to increase the area of an individual chip. The second is to place multiple smaller chips in parallel. While it may seem simple to use a chip with larger area, it is not always the best choice for efficient and economic modules.

In fact, using multiple smaller chips in parallel has distinct advantages. Firstly, smaller chips benefit from thermal spreading if the chips are placed sufficiently apart, which effectively lowers the thermal resistance of the module [12]. In addition, wafer yield is improved with smaller chip size. For example, [13] shows a case where decreasing the chip area from 10 mm x 10 mm to 4 mm x 4 mm results in yields of 49% and 87% respectively [13]. As a result, the number of chips obtained from each wafer can be drastically increased by reducing the chip size. Since the cost of a power semiconductor module is highly dependent on the semiconductor chip cost, higher yield generally results in lower module costs.

Wafer yield is particularly pertinent for SiC semiconductor devices since the defect density in SiC wafers has been reported to be up to 3 orders of magnitude higher than Silicon [14]. Today, the size of SiC chips appears to be limited in comparison to Si devices. For example, in 2022 the maximum size of a commercially available 1.7 kV SiC MOSFET chip was reported to be 7.35 mm x 4.08 mm with a 48A current rating, whereas the largest 1.7 kV Si IGBT chip was 15.93 mm x 16.88 mm with 225A current rating [15].

As a result, high power SiC MOSFET modules are generally constructed with a higher number of paralleled chips in comparison to Si IGBTs. Since the maximum junction temperature must be respected on all chips, derating is applied to reduce the probability that one chip exceeds the maximum junction temperature [16][17]. The magnitude of derating increases as the number of chips in parallel

increases. Consequently, multi-chip temperature data in SiC MOSFET modules is desirable to ensure reliable operation.

In paralleled IGBTs, temperature imbalances of up to 50°C for 6 paralleled chips have been measured and can be normalized through individual gate drivers for each chip [12]. For SiC MOSFETs, an imbalance of up to 10°C is reported in [18] for 5 chips in parallel, and over 20°C in [12]. It has also been shown that the temperature imbalance between paralleled chips is affected by the degradation of the module [19][20]. Nevertheless, as far as the authors are aware, the impact of the operating condition on the temperature distribution between chips has not been reported. In [21], a single SiC MOSFET operating in Body-Diode mode demonstrates a higher thermal resistance than in MOSFET mode. However, this is attributed to measurement error due to threshold voltage shift.

This paper therefore will investigate the chip temperature imbalance of a multichip SiC MOSFET module when it is operated in different operating conditions. The investigation uses on-chip NTC thermistors that are retrofitted to the surface of each SiC MOSFET chip. The module is a Wolfspeed WAB400M12BM3 with 4 paralleled chips per switch position. The module is operated with Silicone potting gel and operated in both MOSFET and Body-Diode mode.

II. On-Chip Thermistor Overview

A. Multi-Chip Temperature Measurement Methods

A few options exist for multi-chip temperature measurements in power modules. Temperature Sensitive Electrical Parameters (TSEPs) are a popular way to measure T_J. Specifically, the $V_{SD}(T)$ (or $V_{CE}(T)$ in IGBTs) method is the most common way to estimate T_J for thermal characterization of power modules. This method delivers a single temperature associated with the mean temperature of the device [9][11]. Although there are some investigations to expand this method to approximate the temperature distribution across a single chip [22], it cannot be applied to extract multi-chip data. Alternative TSEP methods also provide averaged temperature data and have varying performance when applied to multi-chip modules [23].

Methods for multi-chip temperature measurement generally involve direct measurements such as IR cameras or optical fibres. In the case of IR cameras, the silicone gel or potting compound must be removed to provide vision of the chips. The chips must also be black painted with high emissivity paint if repeatable and accurate measurements are desired [24]. Optical fibres can allow measurements to be performed with the potting compound present, however the mechanical placement and positioning of each fibre is a challenge [25][26]. A fibre optic tip may be in the region of 100µm in diameter, and small errors in placement will impact the repeatability of measurements.

In this paper, we use on-chip NTC thermistors to monitor the temperature of each individual chip. Implementation of on-chip sensors has often been proposed and several patents exist [27]-[35]. Many of these proposals require additional packaging terminals or form an intrinsic part of the semiconductor chip and thus are generally installed during the manufacturing process. For example, the use of an on-chip "Kelvin-Emitter" sensor is shown in [35][36]. Although this sensor does not require additional packaging terminals and is placed only on the surface of the chip, it is designed to be electrically integrated into the Kelvin-Emitter path of an IGBT and therefore forms an intrinsic part of the chip's electrical operation – i.e., it cannot be retrofitted.

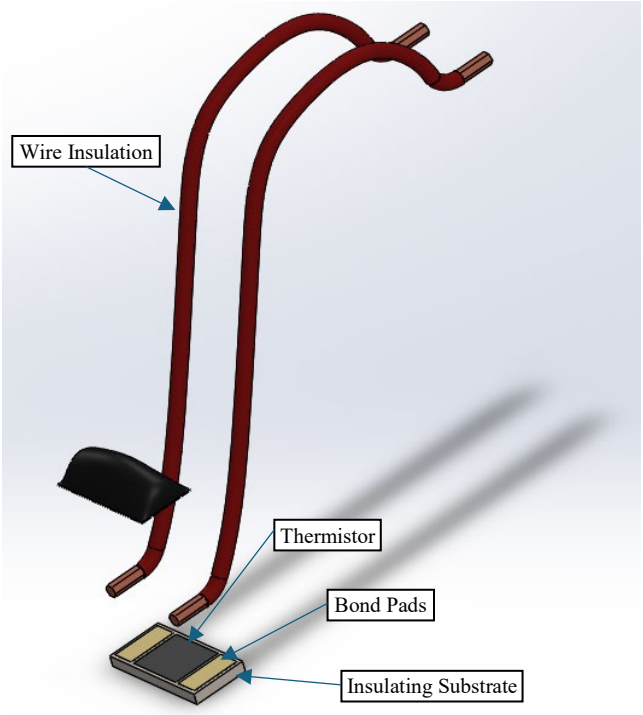

Fig. 1. Exploded 3D model view of the on-chip NTC thermistor.

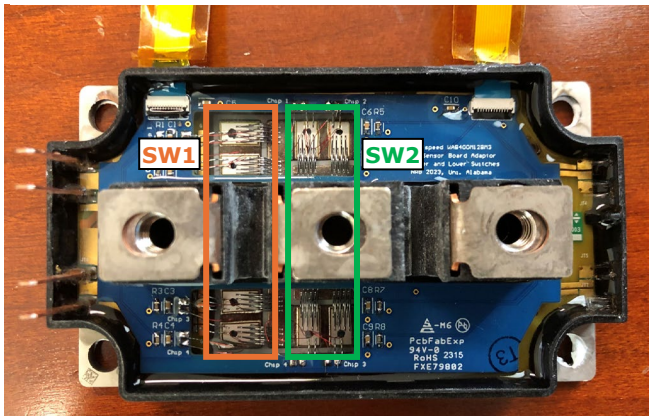

Fig. 2. WAB400M12BM3 with on-chip NTC thermistors and retrofitted PCB. FFC cables are used to connect to an external measurement device (NI-9205) and are covered in Kapton tape for electrical insulation. The module is potted with Wacker SilGel 612.

In this paper, however, we use on-chip NTC thermistors that are retrofitted to the chip surface of a commercial module (Wolfspeed WAB400M12BM3). Although a measurement PCB is required inside the module, the thermistors and PCB are electrically isolated from the chips, and the module can be operated with Silicone dielectric gel.

B. On-Chip Thermistor Description

Fig. 1 displays an exploded 3D view of the on-chip NTC thermistor. The thermistor is manufactured on a 100 µm thick Aluminium Oxide substrate and has dimensions of 1 mm x 0.5 mm. The temperature sensitive thermistor material is on the topside of the substrate, along with two contact pads which have pre-attached measurement leads. The

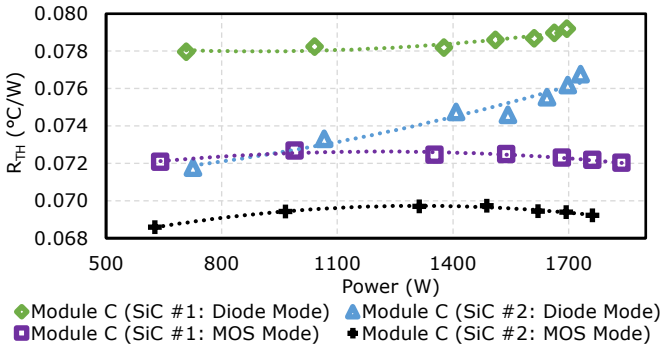

Fig. 3. Junction-to-Ambient Thermal Resistance of 1.7 kV / 1000 A SiC MOSFET modules in MOSFET and Body-Diode operation [38].

measurement leads are 80 µm in diameter and are coated with insulation material. The insulation prevents electrical contact to bondwires and thus allows for more flexible placement of the thermistor. For example, the thermistor could be placed underneath the loop of a bondwire if desired. The terminations of the measurement leads are exposed which allows solder connection to a PCB located and retrofitted inside the power module. Fig. 2 shows a photo of the WAB400M12BM3 with PCB and NTC thermistors mounted inside the module.

In initial prototypes for this research, the measurement leads were not pre-attached. This limited the placement of the sensor and placed additional design requirements on the PCB dimensions. A wirebonder was required to connect to the contact pads and PCB, which introduced mechanical constraints within the module. The pre-attached leads and insulation allowed greater freedom to position the thermistor and use on a larger number of modules.

A further detail of the thermistor is that the substrate contains no bottom-side metallization. The thermistor is mounted using a thermally conductive epoxy which is not electrically conductive. Therefore, the bottom-side of the sensor is non-conductive. This allows the thermistor to be placed across the gate or source pads. However, if this position is chosen, the mounting pressure must be limited since there is a possibility of damaging the gate finger. At present, placement of the thermistor is performed by hand.

Table I. Error across 20 NTC thermistors at increasing temperatures. Difference between minimum and maximum measured NTC temperature is 0.68°C at 152°C.

Mean NTC Measurement (°C)	Difference between Minimum and Maximum NTC Measurement (°C)
15.5	0.14
24.9	0.14
34.4	0.17
44.0	0.20
53.8	0.25
63.4	0.27
73.1	0.26
82.8	0.36
87.7	0.34
97.0	0.40
106.5	0.47
116.0	0.44
125.4	0.50
135.1	0.54
144.4	0.66
152.2	0.68

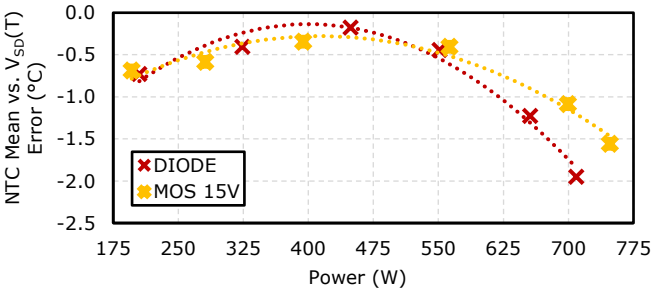

Fig. 4. Error of On-Chip NTC Thermistor Mean Junction Temperature Estimation vs. V_{SD}(T) method. All measurements are within -3°C.

Therefore, controlling the pressure during placement is difficult. Out of approximately 220 chips mounted across a variety of chip types during development of this research, we have experienced 6 chip failures – all of which occurred when mounting across a gate finger.

Electrical measurement of the NTC thermistor is made using a 4-wire measurement where the thermistor is excited using a potential divider with a supply voltage of 3.3 V. The R25 of the thermistors is 10 kΩ with a 1% tolerance on the R25 and B-value. The additional resistor (referred to as R1 in [37]) in the potential divider was chosen to be 806 Ω so that measurement sensitivity was increased in the desired operating range of a power semiconductor chip (between 100°C to 175°C). This resistor was purchased with a 0.1% tolerance and a temperature coefficient of 10 ppm/°C, and is located on the measurement PCB installed in the module. Thus, R1 is located away from the main areas of heat dissipation. The thermistor temperature is calculated using the R25, B-value, and R1 [37].

Table 1 shows measurement results from 20 NTC thermistors when placed on hotplate at various temperatures. The table shows both the mean temperature measured across all 20 NTC thermistors, as well as the difference between the Minimum and Maximum measured temperatures. The results show that measurements from all thermistors are within ±0.35°C up to approximately 150°C. At lower temperatures, the error is within ±0.10°C.

In Fig. 2, two FFC cables exit the module and are covered by Kapton tape. The PCB contains separate planes for both the upper and lower side switch position. This is designed so that in the future, temperatures can be measured during high voltage operation. However, in this paper, experimental results are shown from DC conduction and the FFC cables are connected to a National Instruments NI-9205 voltage input module and recorded without safety electrical isolation.

III. Experimental Results

A. Motivation from Prior Work

Motivation for this work stems from results found in [37], which includes an investigation into 1.7 kV / 1000 A SiC MOSFET and Si IGBT modules. The work presented evidence that the thermal resistance of these modules was dependent on the operating condition. This included whether the module was operated in DC current mode, body-diode mode, or at differing gate voltages.

Since the work in this paper involves a multi-chip SiC MOSFET module, a set of results pertaining to the thermal resistance of the SiC MOSFET modules has been reproduced

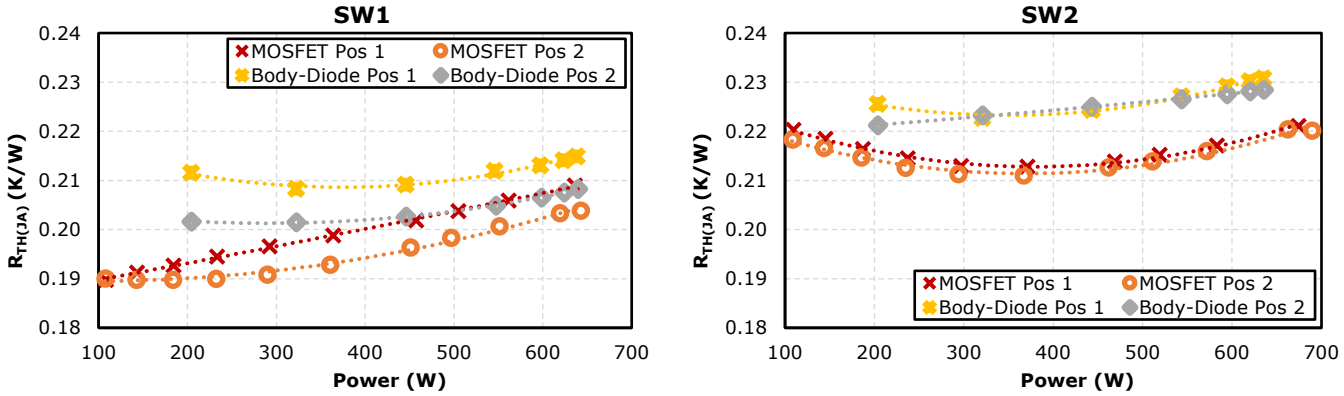

Fig. 5. Junction-to-Ambient Thermal Resistance estimated from mean temperature of on-chip NTC thermistors under differing operating modes, power dissipation, and heatsink position. Thermal resistance in Body-Diode mode is higher than in MOSFET mode.

in Fig. 3 [38]. The figure displays the Junction-Ambient thermal resistance, measured via the $V_{SD}(T)$ method, for 2 samples of a 1.7 kV / 1000 A SiC MOSFET module. It shows that in both samples, the estimated thermal resistance is up to 10% higher when the module is operated in Body-Diode mode compared to MOSFET mode.

This paper will provide further investigation into this phenomenon in multi-chip modules by providing individual chip temperatures on a Wolfspeed WAB400M12BM3.

B. Experimental Conditions

This Wolfspeed WAB400M12BM3 thermal resistance is investigated in the following operating modes:

- MOSFET mode with 15V Gate Voltage
- Body-Diode mode with -5V Gate Voltage
- Two different heatsink orientations

The module is operated continuously in the above conditions with increasing current up until the point it is observed that 1 chip within the module reaches a temperature of 175°C (measured via the on-chip NTC thermistors). With each current increase, chip temperatures are recorded after a period of 300 seconds to allow the module to reach steady state. The module was operated with Silicone Gel (Wacker SilGel 612), and both switch positions were operated simultaneously. The coolant fluid to the heatsink was 20°C, and a Graphite TIM of 200 µm thickness was used.

The highest current level assessed was 358 A in MOSFET mode, and 138 A in Body-Diode mode. Due to the discrepancy in current levels between modes, the following sections display the results with respect to the overall power dissipation induced. A Mentor Graphics PowerTester 2400A was used to provide the DC current as well as record the power dissipation.

C. Error Assessment vs. $V_{SD}(T)$

Junction temperature estimation via the $V_{SD}(T)$ method is only possible during the cooling phase of the module (i.e., when the heating current is removed) [9][39]. Since this investigation was performed with a continuous DC current, the $V_{SD}(T)$ measurement was not recorded for every data point. However, a preliminary assessment of the error of on-chip NTC thermistors vs. the $V_{SD}(T)$ method was performed on SW1. The results are shown in Fig. 4 and show that the

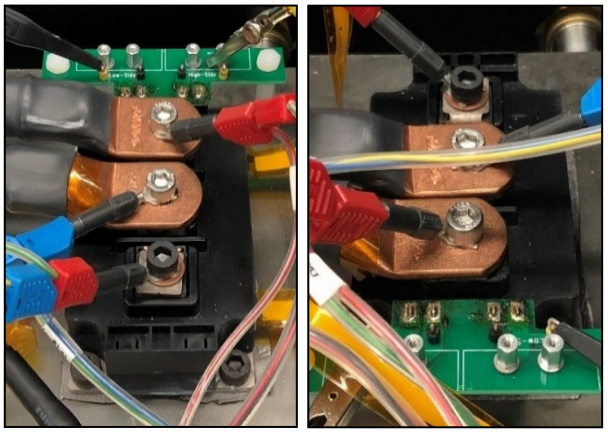

Fig. 6. Heatsink position 1 (left) and Heatsink position 2 (right). The power module is rotated 180°.

mean temperature via the NTC thermistors is within 0°C to -2°C of the T_J estimated via $V_{SD}(T)$ from 200 W to 800 W of power dissipation in both MOSFET and Body-Diode mode.

D. Thermal Resistance and Chip Temperature Distribution measured via On-Chip NTC Thermistors

Fig. 5 displays the estimated thermal resistance (Junction-to-Ambient) calculated from the mean chip temperature measured via the on-chip NTC thermistors. All tested conditions are shown. For reference, the upper switch position is denoted as SW1, and the lower switch position is denoted as SW2. The module position for heatsink position 1 and heatsink position 2 is depicted in Fig. 6.

In all operating conditions, the thermal resistance of SW2 is higher than SW1. For SW2, the thermal resistance in Body-Diode mode is approximately 5% higher than when operating in MOSFET mode. This is also observed in SW1; however, the increase is between 2% - 3%. A dependency on power is observed, with the thermal resistance increasing towards the higher power levels above 500 W. It can also be noted that heatsink position 1 induces a slightly higher thermal resistance compared to position 2 – particularly for SW1.

Fig. 7 shows the chip temperature imbalance for all tested conditions. This is calculated from the difference between the maximum and minimum chip temperature. In SW1, the temperature imbalance remains below 5°C when operating in MOSFET mode. However, in Body-Diode operation the imbalance exceeds 16°C above 600 W of power dissipation.

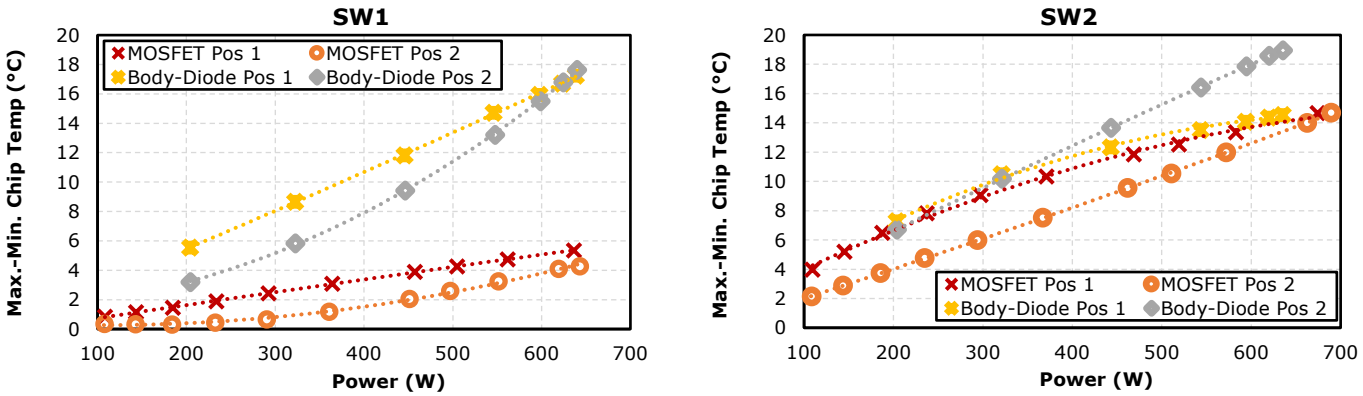

Fig. 7. Difference between the Maximum and Minimum chip temperatures under differing operating modes, power dissipation, and heatsink position. For SW1, this increases from 5°C to almost 18°C when moving to Body-Diode mode at 620 W and above.

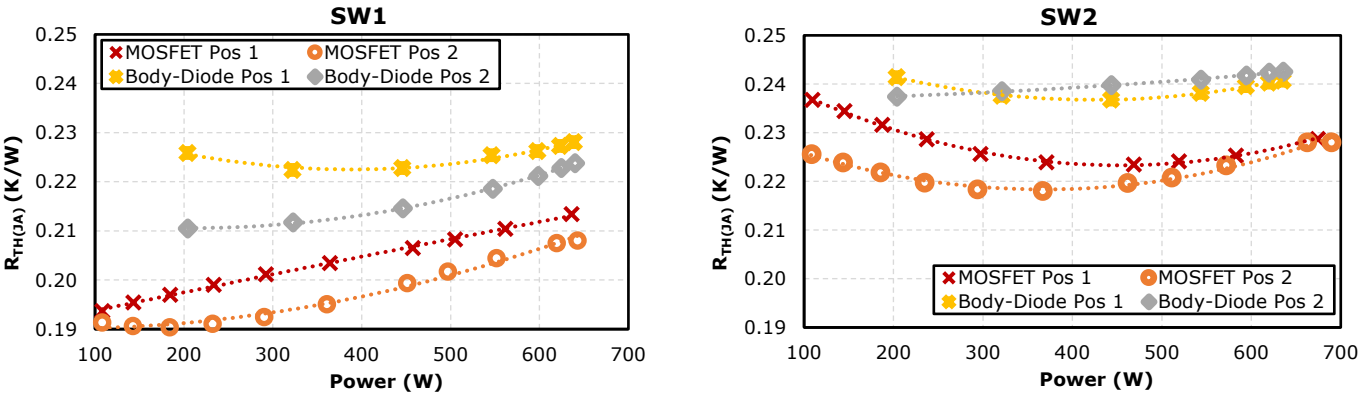

Fig. 8. Junction-to-Ambient Thermal Resistance estimated from on-chip NTC thermistors. The thermal resistance is calculated with respect to the maximum chip temperature.

Heatsink position 1 also induces a slightly higher chip temperature imbalance than heatsink position 2.

For SW2 on the other hand, the chip temperature imbalance is similar in both MOSFET and Body-Diode operation. The imbalance exceeds 14°C above 600 W. The imbalance increases linearly with power in heatsink position 2. In position 1, a clear polynomial trend is observed. Since tests were stopped when 1 chip exceeded the datasheet maximum junction temperature of 175°C, the extent of this trend beyond 700 W was not investigated.

Fig. 8 displays the estimated thermal resistances calculated with respect the maximum chip temperature within each switch position. The trends observed in Fig. 5 are present to a greater degree. The thermal resistance increase from MOSFET to Body-Diode mode now exceeds 5%.

E. Chip Temperature Locations

Fig. 9 shows all chip temperatures within the module when operating in MOSFET mode in heatsink position 1, and Body-Diode mode in heatsink position 2. These operating conditions were observed to have the most pronounced difference in temperature distribution. The chip temperatures shown are normalized to a power loss of 650 W in each switch position. This is performed using a 3rd order polynomial fit from power loss and individual chip temperature data.

In MOSFET mode in heatsink position 1 (Fig. 9b), the location of the hottest chip(s) is shared between Chip 3 and 4 in SW2 at 168.2°C. In Body-Diode mode in heatsink position 2 (Fig. 9c), Chip 3 in SW2 becomes the hottest chip by 5.2°C. The chip temperature spread throughout the module increases from 14.5°C to 30.1°C. In both examples in Fig. 9 (and in all measured conditions), Chip 2 in SW1 saw the minimum temperature within the module temperature.

From Fig. 9c, SW1's minimum chip temperature decreases by 5.8°C, while the maximum chip temperature increases by 6.9°C. The SW1 mean chip temperature remains within 0.5°C. For SW2, all chip temperatures are increased, and the mean temperature increases by 5.6°C.

IV. Discussion and Future Work

The experimental results in Section III provide evidence that the thermal resistance and chip temperature distribution of a multi-chip SiC MOSFET module is altered by operating mode. Reasons for this phenomenon may involve several factors.

1) Paralleling of SiC MOSFETs in MOSFET mode is sometimes described as "self-balancing" due the positive temperature coefficient of the on-resistance [40]. However, in Body-Diode mode, the impedance of the chips has a negative coefficient with temperature and may contribute to the increased chip temperature distribution. Nevertheless, large temperature imbalances can still occur in MOSFET mode, as evidenced by the temperature distribution in SW2.

2) The maximum current tested in MOSFET mode was 358 A, whereas in Body-Diode mode it was 138 A. The package resistance stated in the WAB400M12BM3 datasheet is between 0.51 mΩ to 0.6 mΩ per switch position. At 358 A, this represents a power loss of approximately 70 W. At 138 A, the power loss is 10 W. These losses are spread across the lead terminals and

	SW1	
	MOSFET Heatsink 1	Body-Diode Heatsink 2
Minimum	153.7°C	147.9°C
Maximum	159.1°C	166.0°C
Mean	156.3°C	155.8°C
	SW2	
Minimum	154.0°C	158.8°C
Maximum	168.2°C	178.1°C
Mean	163.3°C	168.9°C

(a)

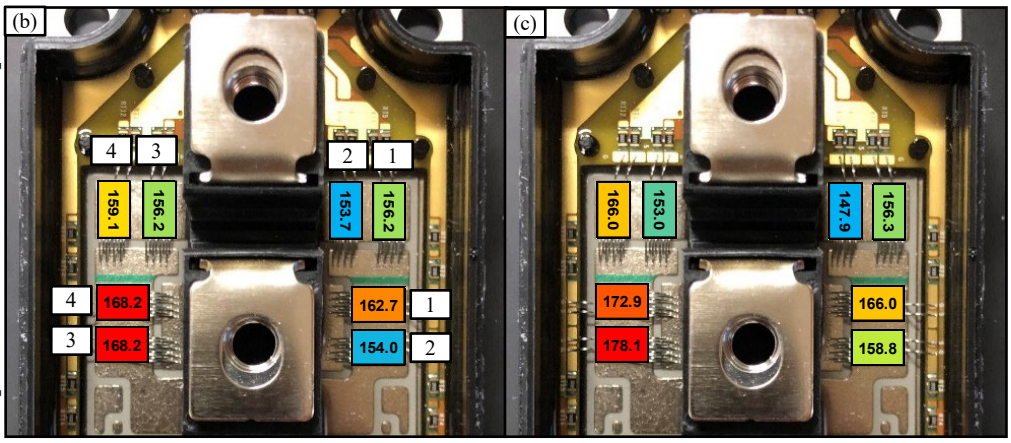

Fig. 9. Individual chip temperatures in MOSFET mode (heatsink position 1) and Body-Diode mode (heatsink position 2). Temperatures are normalized to a power loss of 650 W per switch position.
a) Table showing Minimum, Maximum, and Mean temperatures of both switch positions in each mode
b) Graphical representation of individual chip temperatures in MOSFET mode (heatsink position 1). Chip numbers are labelled.
c) Graphical representation of individual chip temperatures in Body-Diode mode (heatsink position 2)

copper substrate as well as the wirebonds. Therefore, the proportion of power losses produced directly in the chip (i.e., losses contributing directly to junction temperature) compared to the overall measured power dissipation is lower in MOSFET mode.

3) The elevated maximum temperature in Body-Diode mode may contribute to reduced thermal conductivity of the actual SiC material, as well as increasing thermal coupling to neighbouring chips.

The power losses in a real power electronic converter are comprised of conduction loss, switching loss, and body-diode losses. Given these results, it may be supposed that the temperature distribution and thermal resistance of a power module could be altered depending on the relative proportion of each of these losses.

Future work will involve operating a SiC MOSFET module under actual switching operation and observing whether the thermal resistance and temperature distribution will alter depending on switching frequency or deadtime. However, high voltage operation with the on-chip NTC sensors requires further work. EMI issues during switching are a severe hinderance to acquiring data during high voltage operation. Custom measurement circuits must be developed to avoid switching noise. Alternatively, EMI immune measurement methods such as optical fibres or Fiber Bragg Grating sensors [33] could be used to perform these experiments. In addition, monitoring the electrical power losses during high voltage operation may present a challenge.

Future work on single chips could also be conducted to discover whether the thermal resistance trends in this paper are only relevant to multi-chip modules or are also observed in single chip devices.

V. Conclusion

The thermal resistance and temperature distribution of a multi-chip SiC MOSFET power module rated for 1200 V and 400 A is investigated under multiple operating modes. Evidence is provided to show that both parameters are influenced by operating mode. Individual chip temperatures are recorded using on-chip NTC thermistors. The junction-to-ambient thermal resistance of the module increases up to 5% when operating in Body-Diode mode. In addition, the chip temperature distribution also increases. Within 4 paralleled chips, this imbalance can increase from less than 5°C to almost 18°C. It is also observed that the location of the maximum chip temperature can be altered by the operating mode. This investigation is conducted using DC current injection, and future work will involve operating at high voltage and varying the switching frequency and dead-time to alter the proportion of power losses from conduction, switching, and body-diode.

VII. Acknowledgements

The authors would like to thank Robin Savin from ATC Semitec for sourcing of the NTC thermistors.

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