Study on solder void for PiP large solder area ultrathin die in solder reflow

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***Abstract*—Solder print and reflow is one important process for package assembly, especially for some advanced packages. In Package in Package (PiP) module, the solder void formed between the die and the die attach pad of substrate during solder reflow is very common but difficult to eliminate for large solder area die, it is not only detrimental for package thermal dissipation, power dissipation and signal transmission, but also easy to induce serious assembly issue of die crack, especially for ultrathin die.**

In this study , the root cause of die crack is identified by failure analysis, and the safe margin of solder void percentage for crack is found out by die stress simulation. By analyzing the mechanism of solder void for both Quad Flat No-lead (QFN) and die with large solder area in PiP, the root cause of solder void is understood. By experiment of solder void, the main effect factors of solder void are found out. By experiment of design(DOE), the process conditions are optimized, the solder void of QFN and die are improved. To further improve the solder void underneath ultrathin die, the secondary print and reflow process is introduced and combined with optimized process conditions by DOE, reduced the solder void coverage to less than 3%, which can solve the die crack issue.

Key words: solder paste; solder void; reflow; Package in Package.

I. INTRODUCTION

In semiconductor package assembling, solder paste print and reflow is adopted extensively as good solderability, better thermal dissipation and higher reliability, especially for some advanced packages, such as Package in Package(PiP) which the various packages or die are soldered with substrate as one package.

In solder paste print and reflow process, solder paste is printed first on Die Attach Pad(DAP) of the substrate, packages or sawed dies are then placed on printed solder paste. The hamburger structure is formed by substrate ,solder paste and die, very limited lateral space along the die periphery is provided for the solder paste to touch out side. It is more difficult for the air in the solder paste to discharge out. The solder void is generated because the wrapped air and volatile gas can not escape completely through the molten liquid tin which melt during reflow.

The effects of solder void underneath the die, package, and in the solder ball of Ball Grid Array (BGA) package have been studied extensively. Different effects on package thermal dissipation, power dissipation and signal transmission depend on the size and percentage of solder void[1][2].Most of studies are focused on the solder void in solder ball, and some of them successfully found out the root causes and solutions[3][4], however very few of the investigations involve the package or die with solder area larger than 6mm^2 .

This study is based on a PiP package , one QFN and one ultrathin die along with other components are soldered in it together, the QFN solder area is 4.4mm×4.1mm,the ultrathin die solder area is 3mm×2.3mm,the thickness is 60μm. During wire bonding and molding, the crack is occurred on the die where excessive solder voids exist down below, It was validated by experiment in previous work, no die crack happened when the solder void coverage was less than 10%, So in this work, it is aimed at optimizing the soldering parameters, and introducing new process to meet this void coverage expectation, and thus to solve the die crack issue.

II. SOLDER VOID MECHANISM AND VALIDATION

The PiP package dimension is 10mm×8mm×2mm, there are one QFN and one die are soldered in it except other components, the PiP structure is shown as Fig. 1.

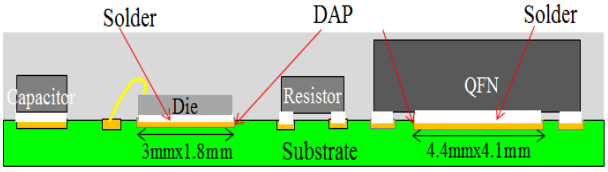
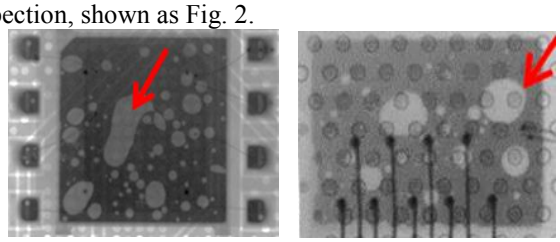


Figure 1 PiP cross section picture

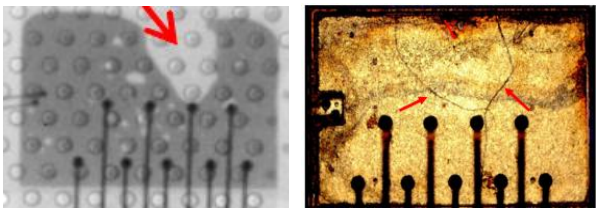
After solder reflow, the solder void generates between die and substrate DAP, it is shown as lighter color compares around darker area in the solder color under X-ray inspection, shown as Fig. 2.



(a) QFN solder void (b) Die solder void

Figure 2 Typical solder void picture under X-ray

High percentage defect is detected by the function test in this PiP package, the failure analysis shows almost all crack occur in the die with excessive solder void underneath it, and the crack caused in molding process, it is also identified that the die with larger void is easier to crack as the worse strength is unable to withstand the molding transfer pressure, shown as Fig. 3.



(a) Die solder void (b) Die crack over the void

Figure 3 Failure analysis decap shows the die crack over the solder void

Comparing the QFN package, the ultrathin die has worse strength even though there is less solder void under it, so reducing the solder void and void coverage is the most effective solution to solve the die crack issue. To find the solder void safe margin of the crack for ultrathin die, the die stress simulation for different solder void percentages and locations has been done, it shows this 60μm thickness die has no crack risk when the solder void coverage is less than 10% in current molding transfer pressure, so the less solder void than 10% is expected to solve die crack issue, the die stress simulation shown as Fig. 4

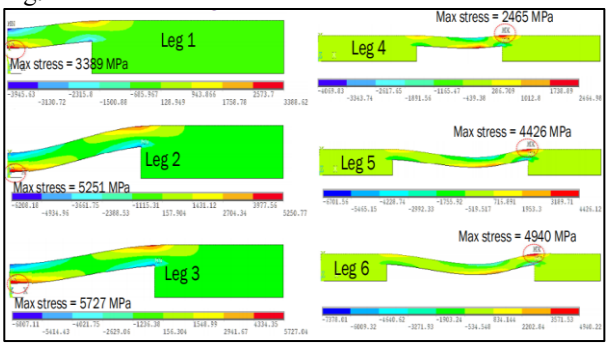


Figure 4 Die stress simulation of different solder void percentages and locations

A. Solder void mechanism

The solder paste used for QFN and die soldering is SAC305(tin96.5%,silver3.0%,copper0.5% by content). The composition includes tin(small solder ball) and flux (rosin, adhesive, active agent, solvent), and the flux wraps the solder balls together and fills the gap among them. The PiP package passes through reflow owen after solder paste printing and QFN and die mounting, the solder paste undergoes four stages of preheating, activation, reflow and cooling. The temperature is different in four different stages, and the state of solder paste is changed as the different reflow temperature in different stages.

During the preheating and activation stages, on one hand, the volatile components in solder paste changes to gas to escape out when heated, then the solder balls gather more tightly, on other hand, the hollow gap formed among the solder balls as the volatilization of flux is occupied by air.

During the reflow stage, the flux remaining in the solder paste evaporates quickly, then the solder balls rapidly melt and change to liquid tin in high temperature, after that the air partially change from the volatile components of flux and other fill in the hollow gap among solder balls fail to escape out from liquid tin timely, the air wrapped by liquid tin is also more difficult to escape out just from very small lateral space along die periphery as covered under die, a little wrapped air escapes out by buoyancy in short time of reflowing, but other air is trapped and remained by liquid tin, and it forms solder void during cooling stage, the solder void forms procedure is shown as Fig. 5.

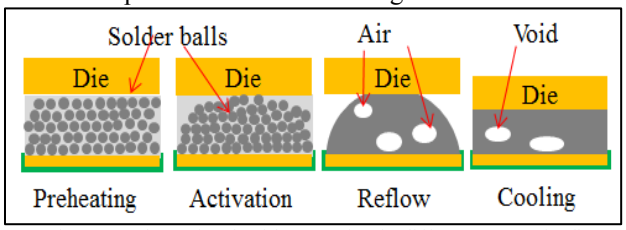


Figure 5 Schematic of void generation in different stage of reflow

B. Effect factors validation

Based on the mechanism of solder void generated in reflow, the solder void caused as the air is trapped in melted tin and incompletely discharged, there are many factors during reflow, such as solder paste type, stencil opening shape, paste amount, reflow temperature and reflow time. In addition, the different soldering sizes and structures also effect it. Takes this PiP package to do experiment and compares the result to find out the main effect factors of solder void as below

Fig. 6 shows the solder void percentage with two different type of solder paste, type 3 solder ball size is 25μm-45μm, type 4 solder ball size is 20μm-38μm, both QFN and die show there is no significant difference for two type solder paste in solder void percentage, concludes solder paste type is not main effect factor for solder void.

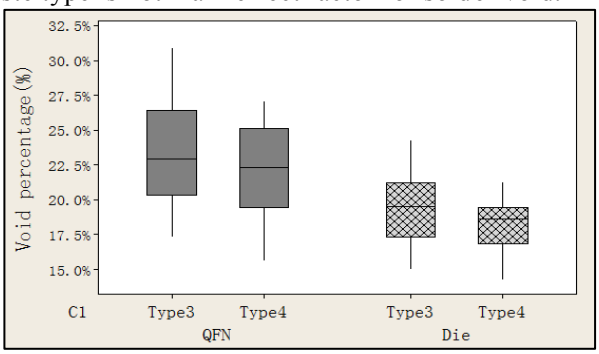


Figure 6 T-test compares the solder void percentage with different type solder paste

Fig. 7 shows the solder void percentage in the different reflow times(60s,70s,80s,90s).It is found that it is significant difference in the different reflow times for both QFN and die in solder void percentage, concludes solder paste type reflow times is a main effect factor for solder void.

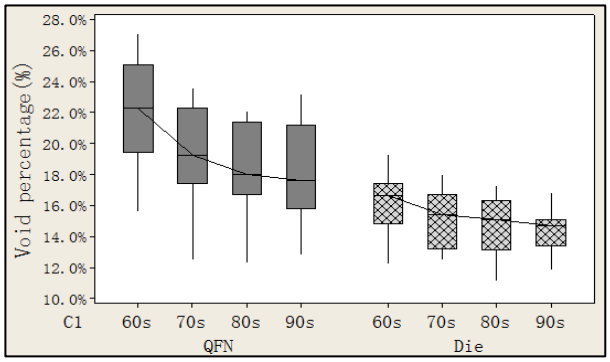


Figure 7 T-test compares the solder void percentage in different reflow time

Fig. 8 shows the solder void percentage in different reflow peak temperature(240C,250C,260C). No significant difference is found in different reflow peak temperature

for both QFN and die in solder void percentage, concludes reflow peak temperature is not main effect factor for solder void.

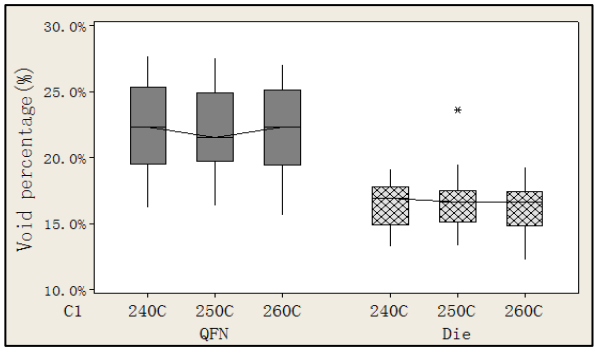


Figure 8 T-test compares the solder void percentage in different reflow peak temperature

Fig. 9 shows the solder void percentage in different stencil opening shape(a square, b long grid, c oblique grid, d circular),the yellow color shows the aperture of different stencil opening. No significant difference is found in different stencil opening shape for both QFN and die in solder void percentage, compares other stencils, the circular shape stencil has higher percentage of void which caused by insufficient paste as very smaller opening of stencil, concludes stencil opening shape is not main effect factor for solder void.

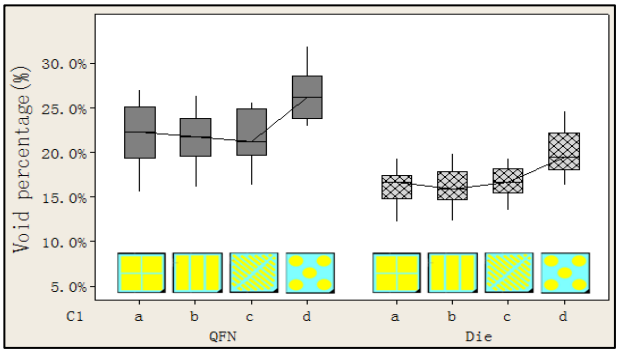


Figure 9 T-test compares the solder void percentage with different stencil opening shape

Fig. 10 shows the solder void percentage in different stencil thickness (50μm,75μm,100μm, 125μm). Significant difference is found in different stencil thickness for both QFN and die in solder void percentage, concludes stencil thickness is not main effect factor for solder void.

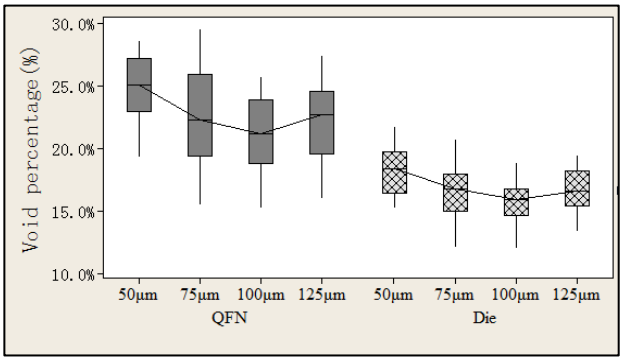


Figure 10 T-test compares the solder void percentage with different stencil thickness

By the experiment validation, it is found that reflow time, stencil thickness(solder paste amount) are the main effect factors for solder void, and the stencil opening shape which obviously reduce the solder paste amount also cause higher percentage of solder void.

III. SOLDER VOID IMPROVEMENT AND VERIFICATION

A. DOE improve solder void

Base on the preliminary experiment result, the main effect factors reflow time and stencil thickness are optimized by DOE to find the best process conditions for solder void improvement, the other factors are defined directly as below, the solder paste is type 4, the stencil opening is grid and the reflow peak temperature is 260C. The DOE result is shown as Fig. 11, the 100μm thickness stencil and 80s reflow time is the best process condition for solder void performance.

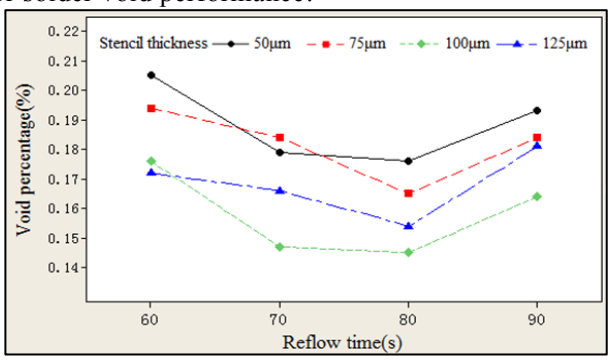


Figure 11 Interaction of reflow time and stencil thickness for solder void percentage

Run the 1000pcs pilot with DOE optimized process conditions to validate the solder void performance, the result shows the solder void percentage reduces to 16.4% from 27% for QFN and it reduces to 14.7% from 21% for the ultrathin die, but it still does not meet the safe margin less 10% even though it is much lower than before for die. It is necessary to find out other solutions which can meet the expectation of solder void.

B. New process improve solder void

As the air wrapped by liquid tin is difficult to escape out from very small lateral space along die periphery, it is may very helpful to removes the die which covers on the liquid tin to keeps the sufficient space for wrapped air discharging by buoyancy, so the secondary solder print and reflow process is developed and introduced based on it. The new process flow includes the first solder print and reflow without QFN and die, the second solder print and reflow with QFN and die, shown as Fig. 12.

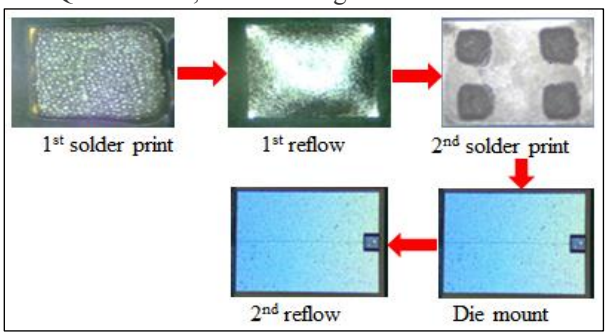


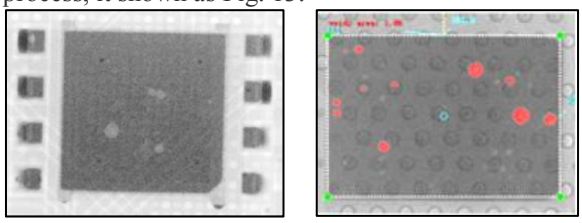
Figure 12 Schematic of secondary solder print and reflow procedure

The solder thickness reduces to about 50μm after reflow for 75μm thickness printed solder paste normally. 75μm thickness solder paste is printed first and passes through

reflow without die, almost all air wrapped by liquid tin escapes out during reflow as no die cover it, and then 50μm thickness solder paste is printed upon the first solder, the total thickness of solder paste after the second solder printing is kept about 100μm, which is best thickness condition validated in previous DOE.

As the less solder paste the less air in it, the special stencil is used to print solder paste as less as possible but still make sure the good soldering performance, so the 4 dots small square opening stencil is developed and used for the second solder paste printing.

One small sample is run to validate the solution, the result shows the solder void performance is very good both for QFN and die with the secondary solder print and reflow process, it shown as Fig. 13.

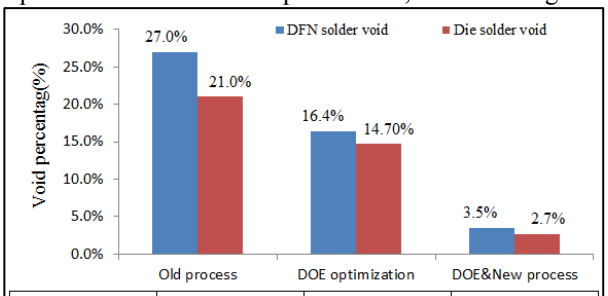


(a)Solder void under QFN (b) Solder void under Die

Figure 13 X-ray photo of solder void with secondary solder print and reflow process

C. Solution verification

Run one pilot of 2000pcs PiP to further verify the new process of secondary solder print and reflow with DOE optimized conditions, the solder void percentage is measured for all PiP by X-ray machine, the result shows the QFN solder void percentage reduce to 3.5% and the die solder void percentage reduce to 2.7% which is much less than the expectation of 10%, the secondary solder print and reflow process has significant improvement compares with old process and even DOE optimization, shown as Fig. 14.



	Old process	DOE optimization	DOE&New process
DFN solder void	27.0%	16.4%	3.5%
Die solder void	21.0%	14.70%	2.7%

Figure 14 The solder void percentage in different processes

The test yield and reliability are also compared for further verification, takes good units to do reliability test include Moisture Sensitive Level 3 (MSL3), Moisture Sensitive Level 2(MSL2) and Thermal Cycle Test 500 cycle(TCT500), the result is shown as Table 1, 99.8% test yield of the new secondary solder reflow is much higher than the old process test yield which does not reach 80%, and no die crack and excessive solder void are found in the test failure of new process. The PiP package assembled with the new process passes MLS2, but the PiP package assembled with the old process fail to pass MSL3 as the defects which caused by excessive solder void .

Table 1 Comparison of yield and reliability for old process and new process

	Yield	**Reliability**		
	Test	***MSL3***	***MSL2***	***TCT500***
Old process	<80%	Pass	Fail	Fail
New process	99.8%	Pass	Pass	Pass

Base on the comprehensive comparison of solder void, yield and reliability, the new secondary solder reflow process is effective not only to reduce the solder void for large solder area die of PiP package , but also can improve the PiP package yield and reliability.

IV. SUMMARY

For the QFN and die with large solder area in PiP package, the solder void is formed as the air is wrapped in liquid tin and incompletely escapes during reflow. The void percentage is reduced even though optimizing the process conditions ,especially for solder paste volume and reflow time which are the main effect factors, but it still can not meet the safe margin of 10% for ultrathin die with large solder area. The new process secondary solder paste print and reflow is developed and combined with optimized process conditions, the solder void of ultrathin die is reduced effectively and the percentage is controlled below 3%, the yield and reliability of the PiP package is also improved significantly. This study is of instructive to improve solder void for ultrathin die with large solder area.

It needs to be pointed out that this study just focus on the conventional solder reflow process, and develops the new secondary solder reflow process, but for some other new technologies have been developed to improve solder void, such as the vacuum reflow[5] and the preform solder[6], are not involved in this paper, and will be another study topic of solder void improvement.

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