Name:	Balkir, Arda
SRN:	19040531
Module:	4COM1042
Session:	wt06 (G12, nodate from unknown time to unknown time (unknown location))
Submitted:	09/03/2021 17:47:44 (unknown location) time left: N/A
Logged in:	[time unknown]
Logged out:	[time unknown]

1. Which **one** of the following instruction sequences loads the numbers 58 and 14 into two registers and leaves the result of the calculation 58 - 14 in register r0?

   ❑
   ```
   ldi r3, 58
   ldi r0, 14
   sub r0, r3
   halt
   ```

   ❑
   ```
   ldi r3, 14
   ldi r0, 58
   sub r0, r3
   halt
   ```

   ❑
   ```
   ldi r3, 14
   ldi r0, 58
   sub r3, r0
   halt
   ```

   ★ **[expected answer]**
   ```
   ldi r3, 58
   ldi r0, 14
   sub r3, r0
   halt
   ```

   Points given: 10/10

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2. Which of the following instruction sequences swaps the contents of registers r2and r1? (Tick all that apply)

★ **[expected answer]**

```
move r2, r3
move r1, r2
move r3, r1
```

❑

```
move r2, r1
move r1, r2
```

❑

```
ld r2, r3
ld r1, r2
ld r3, r1
```

★ **[expected answer]**

```
move r1, r3
move r2, r1
move r3, r2
```

❑

```
st r1, r3
st r2, r1
st r3, r2
```

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3. Which of the following instruction sequences leave the number −81 in register r1? (Tick all that apply)

❑
```
ldi r1, 81
dec r1
halt
```

❑
```
ldi r2, 81
not r2
move r2, r1
halt
```

❑
```
ldi r1, 81
not r1
dec r1
halt
```

❑ **[expected answer]**
```
ldi r1, 81
not r1
inc r1
halt
```

★ **[expected answer]**
```
ldi r1, 81
neg r1
halt
```

Points given: 5/10

---

4. What is the bit-wise AND of the following two 6-bit strings? Make sure you give all 6 bits in your answer

```
101100
101101
```

supplied answer: 101100

expected answer: `0b101100`

Points given: 10/10

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5. Which **one** of the following instructions **has no effect on** any of the CVZN flags in the Processor Status (PS) register?

   ❑ `shr r2`

   ★ **[expected answer]**

   `st r0,r1`

   ❑ `and r0, r3`

   ❑ `cmp r2, r1`

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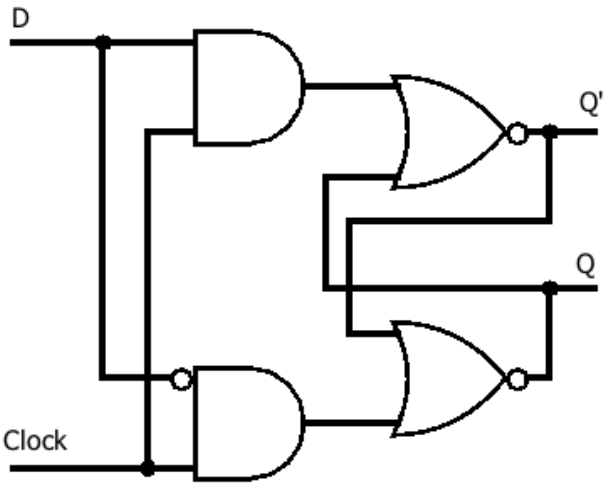
6. Below is the circuit diagram of the D-latch.



At the moment the clock is high. What will be the value of the data output Q when the clock falls? (choose one)

- ❑ It will follow the changing value of D with some delay until the clock rises.
- ❑ It will be the same as the value of D whether the clock is high or low.
- ★ **[expected answer]**It will not change as long as the clock is low but will follow the changing value of D with some delay when the clock rises again.
- ❑ It depends on what Q′ was before the clock went up.
- ❑ Q will rise if it is down and fall if it is up.

Points given: 10/10

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7. What is the purpose of the Master-Slave D-latch? (tick one)

   - ❑ To provide two separate D-latches, one called Master and the other Slave, the Master outputting during the high-clock period and the Slave during the low-clock period.
   - ❑ To provide two separate D-latches, one called Master and the other Slave, the Master outputting during the low-clock period and the Slave during the high-clock period.
   - ❑ To maintain the output before the falling edge of the clock; to copy the input to the output during the low-clock period.
   - ❑ **[expected answer]**To maintain the output Q before and after the falling edge of the clock; to change it according to the input D at the moment the clock falls.
   - ★ To copy the input to the output during the high-clock period; to maintain the output after the falling edge of the clock.

   Points given: 0/10

---

8. Below are some statements about buses. For the avoidance of doubt, in reading these statements, assume that a 'register' is nothing more than an arrayed D-latch
   Tick all statements that are correct

   - ❑ **[expected answer]**Only one user of a bus can assert a value on it in any given clock cycle
   - ★ The output of a register is wired directly to the bus
   - ❑ A bus is a wire bunch connecting a single output to a single input
   - ★ A controlled buffer is a device that has a data input, a control input and a single output. If the control input is high, the output copies the data input; if it is low, the output is zero
   - ❑ **[expected answer]**The purpose of the controlled buffer is to sit between a bus-user output (for example, the register pin Q) and the bus; when the control input is high the register drives the bus, otherwise it is disconnected allowing other bus-users to assert their values.

   Points given: 0/10

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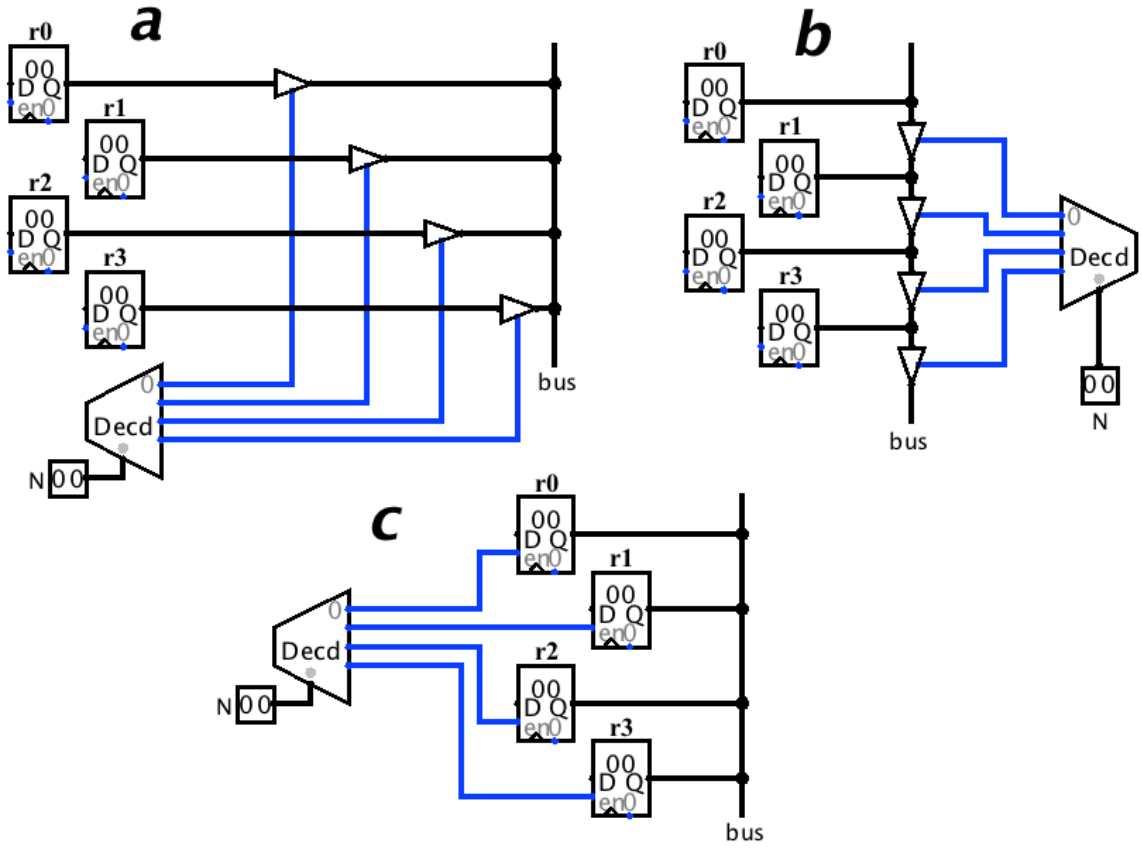
9. Below are three diagrams that show how the *outputs* of the registers in a register file may be connected to a bus. Recall that registers have the output port Q on the east side, the input port D on the west side, and the enable pin right under D.



Only one of the above diagrams is correct. Which one?

- ❑ **[expected answer]** *a*
- ❑ *b*
- ★ *c*

Points given: 0/10

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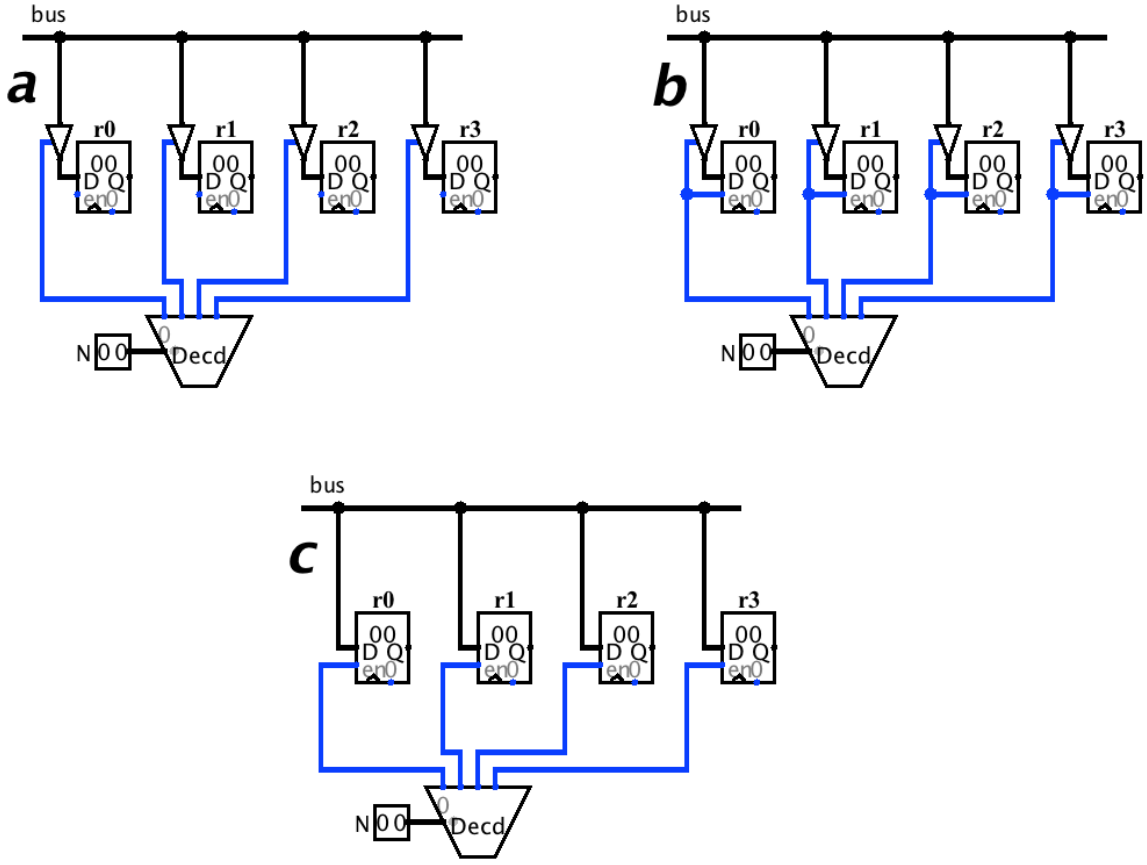
10. Below are three diagrams that show how the *inputs* of the registers in a register file may be connected to a bus. Recall that registers have the output port Q on the east side, the input port D on the west side, and the enable pin right under D.



Only one of the above diagrams is correct. Which one?

- ❑ *a*
- ★ *b*
- ❑ **[expected answer]***c*

Points given: 0/10

***** TOTAL POINTS GIVEN: 55 OUT OF 100 *****