MIPS Datapath Group Project

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2. **Verilog Model**

   The Verilog code we selected is from Zybooks 12.9.1, it is attached in file verilog.v

3. **Datapath**

   We implemented a pipelined datatpath in our verilog code.

4. **Memory**

   Single level memory implementation

5. **Simulation**

   Sample MIPS program

```
add $s1,$s2,$s3
add $s4,$s1,$s3
j dest
```

```
Contents of each instruction
r-type instructions
line    opcode[31:26]   rs[25:11]   rt[20:16]   rd[15:11]   shAmt[10:6] funct[5:0]
1       000000          10010 (s2)  10011 (s3)  10001 (s1)  X           100000
2       000000          10001 (s1)  10011 (s3)  10100 (s4)  X           100000

i-type instruction
line    opcode[31:26]   address[25:0]
3       000010          dest
```

Verilog Processor Execution: () **Cycle 1 (Instruction Fetch):**

In cycle 1 of execution, PC, Instruction, and the Add ALU is used

PC: Input: 0, Output = 0

Instruction Memory: Input: 0,

Cycle 2 (Instruction Decode):

In cycle 2 of execution, WriteReg, our Control Unit, Register File, and Sign Extend are used.

Execution

Cycle 3 (Execution):

Cycle 4 (Memory):

Cycle 5 (Write Back):

6. **References**

https://bellerofonte.diism.unisi.it/index.php

Computer Organization and Design - Interative Version (MIPS)

FOR REFERENCE AMIGOS:

Single-level memory is organizing memory with processor and (slow) main memory (DRAM)

Compare with multilevel memory, which has at least one (quick) cache between the processor and main memory.

7. **Contributions**

Jose Idrovo:

Adrian Rodriguez:

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