VLSI DESIGN FLOW: RTL TO GDS

Lecture 24
Static Timing Analysis – Part III

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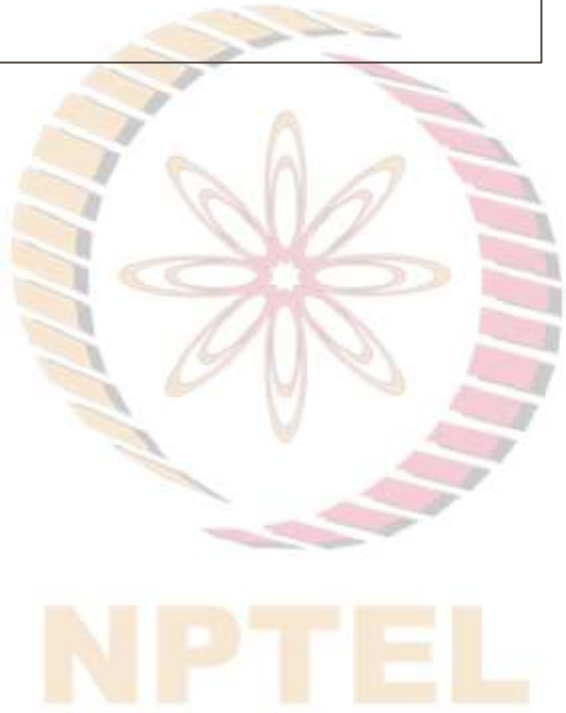
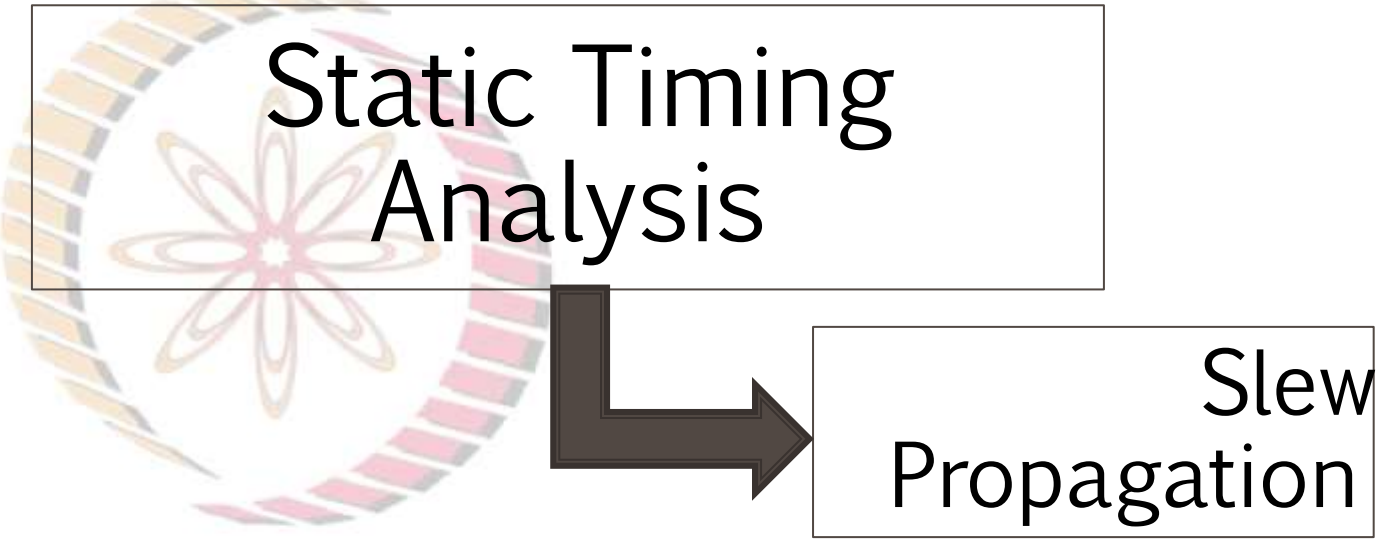
Lecture Plan

- Slew Propagation
- Accounting for Variations





Need for Slew Propagation

- For computing delays for a given stage, the slews at its inputs must be known.
  - An STA tool must also propagate the slews in the timing graph

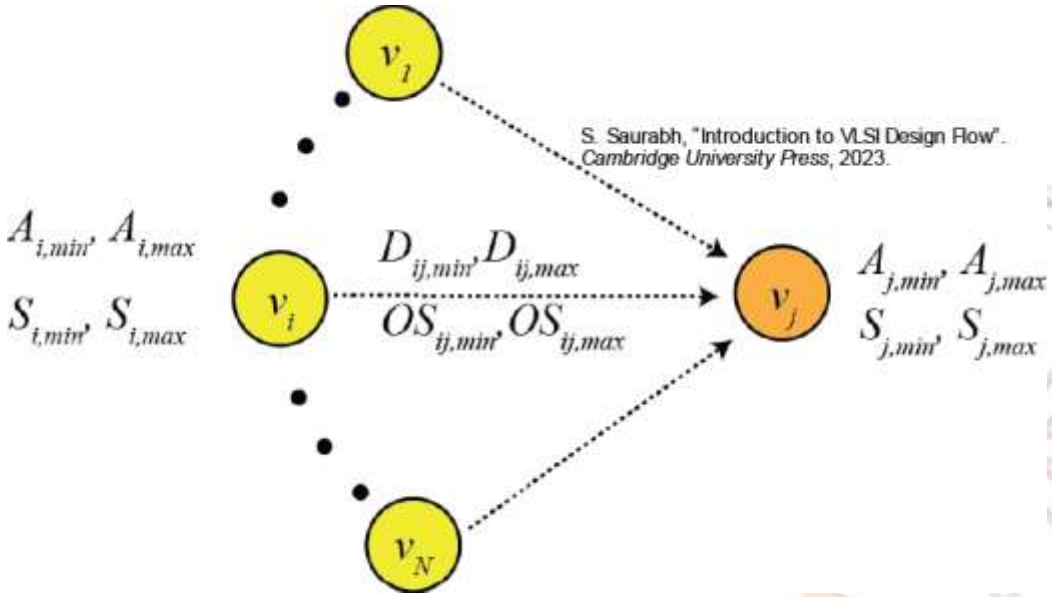
- The propagated slews can be different through different combinational paths.

Relationship between Slew and Delay

- Delay and the output slew are typically monotonically nondecreasing functions of the input slew

- Allows computing, storing, and propagating only the minimum/maximum slews
  - Can obtain the bounds on the delay and the output slews using the bounds on the input slews.

Slew Propagation: Bound on Slew



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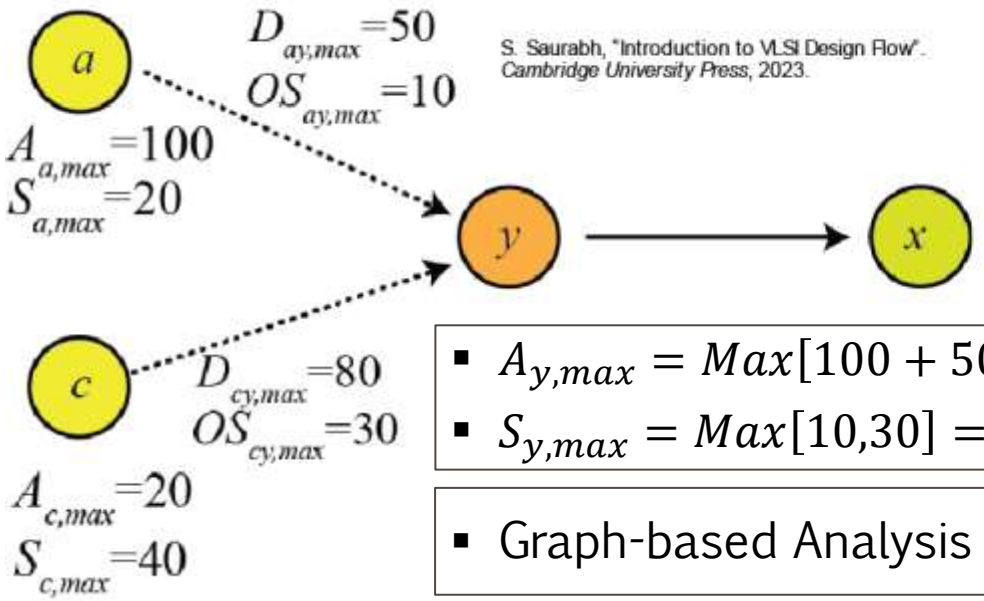
- $A_{j,min} = Min[A_{i,min} + D_{ij,min}]$
- $A_{j,max} = Max[A_{i,max} + D_{ij,max}]$

- $S_{j,min} = Min[OS_{ij,min}]$
- $S_{j,max} = Max[OS_{ij,max}]$

Slew Propagation: Example (Maximum Case)



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Input Slew S_y	Delay D_{yx}	Output Slew S_x
10	30	10
30	100	20

- $A_{y,max} = Max[100 + 50, 20 + 80] = 150$
- $S_{y,max} = Max[10,30] = 30$

- $A_{x,max} = 150 + 100 = 250$
- $S_{x,max} = 20$

- Graph-based Analysis (GBA): Safe Bound, Not tight (most popular)

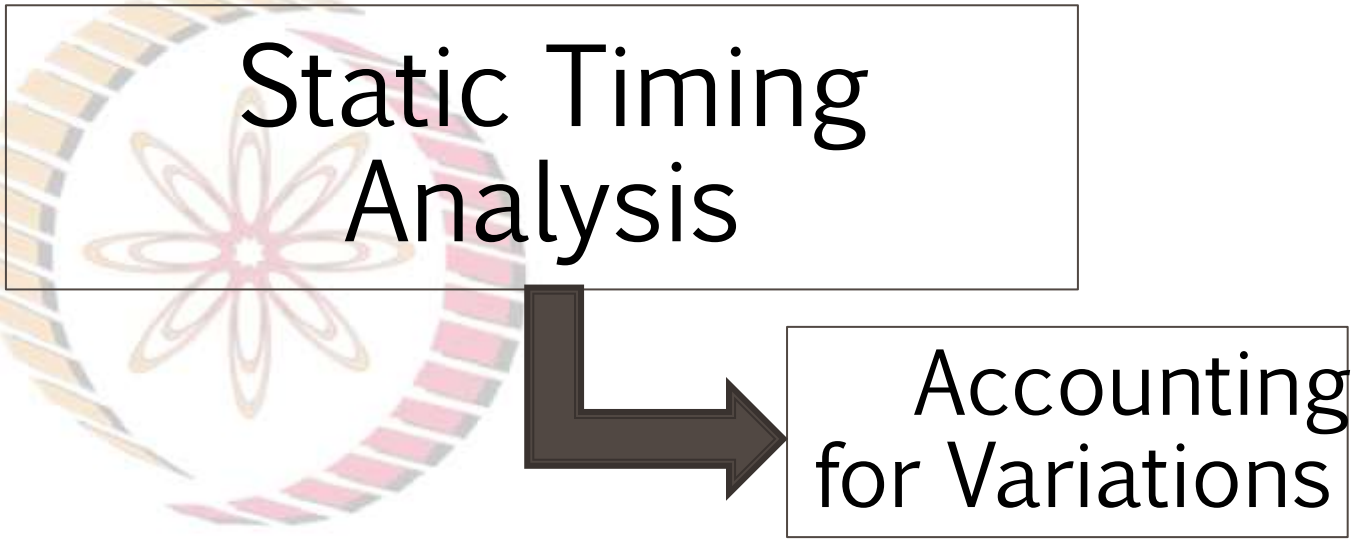
- $A_{y,max} = 150$
- $S_{y,max} = 10$

- $A_{x,max} = 180$
- $S_{x,max} = 10$

- $A_{y,max} = 100$
- $S_{y,max} = 30$

- $A_{x,max} = 200$
- $S_{x,max} = 20$

- Path-based Analysis (PBA): Path-specific, computationally difficult



Need to Account for Variations

- Behavior of transistors/circuit elements can differ from the nominal behavior due to process-induced variations and fluctuations in temperature and voltage (PVT variations)
  - Delay and other timing attributes change
  - Can result in timing failure

- To tackle variations, different techniques are employed.
  - Differ in accuracy, modeling effort, computational resource requirement, and design effort.

Safety Margins

- Easiest technique
- Can convey margins to an STA tool using appropriate constraints
  - ➢ Adjust the required time such that timing requirements become stricter

- Large Margin: overly pessimistic (loss in PPA)
- Small Margin: chance of timing failure, yield loss
- Need to consider these tradeoffs

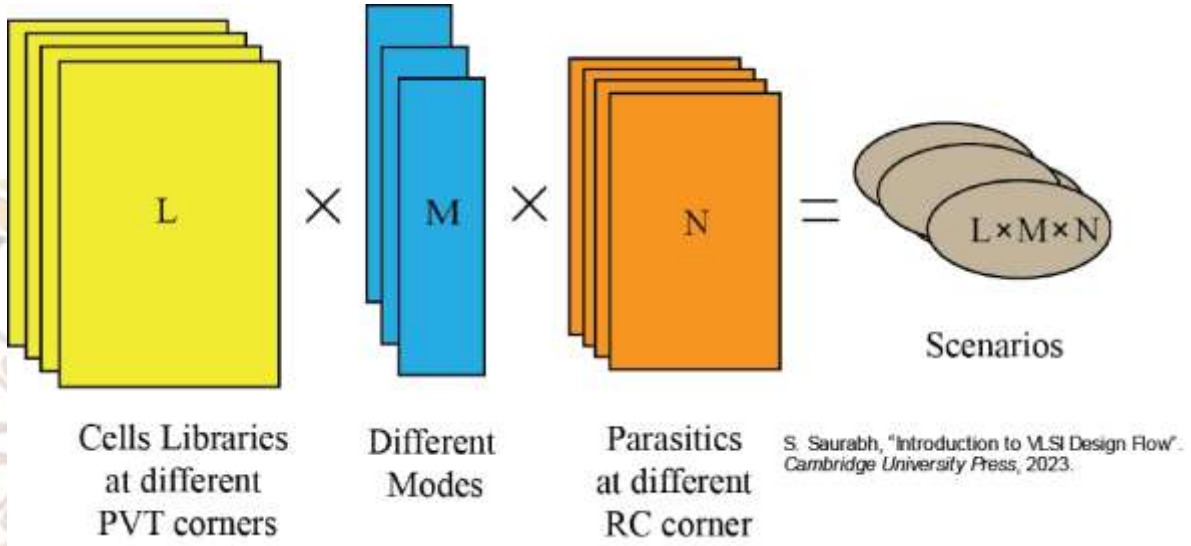
- Typically employed in early stages of VLSI design flow

Multi-mode Multi-Corner (MMMC) Analysis

- Carry out STA at some discrete set of **scenarios** to account for variations

Scenarios are created by a combination of:

- **PVT corners** for technology libraries: accounts for global variations (worst, best, typical, etc.)
- **Multiple modes**: using SDC files for different modes such functional, test, sleep, turbo, etc.
- **RC corners**: extract multiple SPEF files to account for process-induced variations in interconnects.



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- Analyze multiple scenarios simultaneously using MMMC analysis
- Efficiency:
  - Avoiding computation of the dominated scenarios
  - Exploiting parallel processing

On-Chip Variations (OCV) Derate

- Need to account for local variations in the properties of devices and interconnects on the same die
  - ➢ Specify OCV derate factors

- **Effective delay**: obtained by multiplying the nominal delay with the OCV derating factor

Can define different OCV derating factors based on:

- Path bounds (early or late)
- Path type (data or clock)
- Delay type (gate delay or interconnect delay)
- Corners (best, worst, typical, etc.)

Late path derating factor = 1.1
Early path derating factor = 0.9

Setup Analysis:

- Data path and clock launch path: 1.1
- Clock capture path: 0.9

Hold Analysis:

- Data path and clock launch path: 0.9
- Clock capture path: 1.1

Demerit:

- Assumes perfect positive correlation among timing arcs of same group
- Assumes perfect negative correlation among timing arcs of different group
- Overly pessimistic

References

- S. Saurabh, “Introduction to VLSI Design Flow”. Cambridge: *Cambridge University Press*, 2023.
- Bhasker, Jayaram, and Rakesh Chadha. *Static timing analysis for nanometer designs: A practical approach*. Springer Science & Business Media, 2009.