VLSI DESIGN FLOW: RTL TO GDS

Lecture 38
Chip Planning - II

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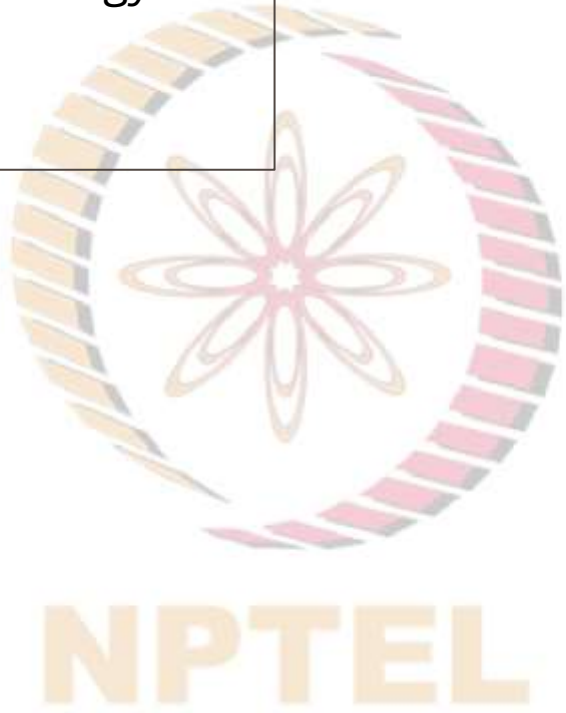
Lecture Plan

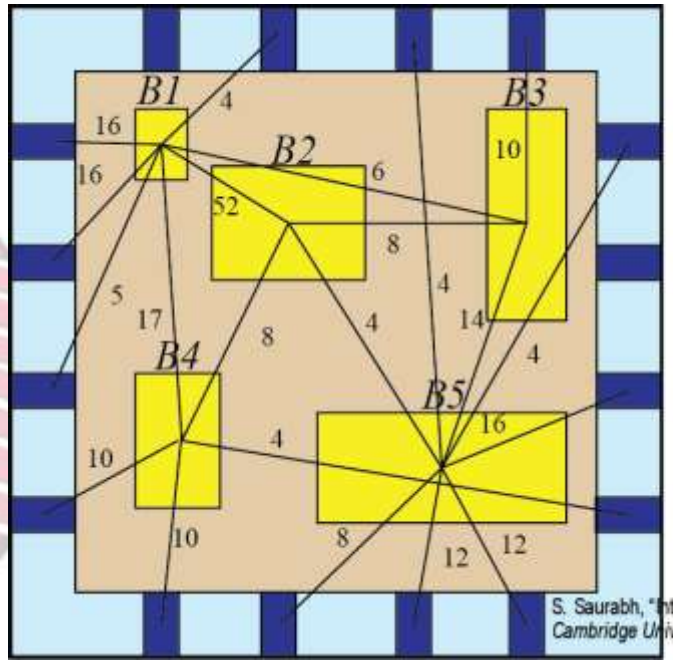
- Chip Planning
  - Hierarchical Design Methodology
  - Floorplanning
  - Power Planning



Large Object (Macro) Placement

- Placement of large objects undertaken during floorplanning
  - Blocks (obtained in partition), RAM, analog blocks (such as PLL), etc.
- Placement of standard will be undertaken during placement stage

- Initial macro placement is guided by connectivity
  - Strongly connected macros placed close together
  - Fly lines can guide the floorplan
  - Macros interacting with external world close to I/O pads
- Predictive routing (rough routing) can be done to get an initial idea of problem in the floorplan



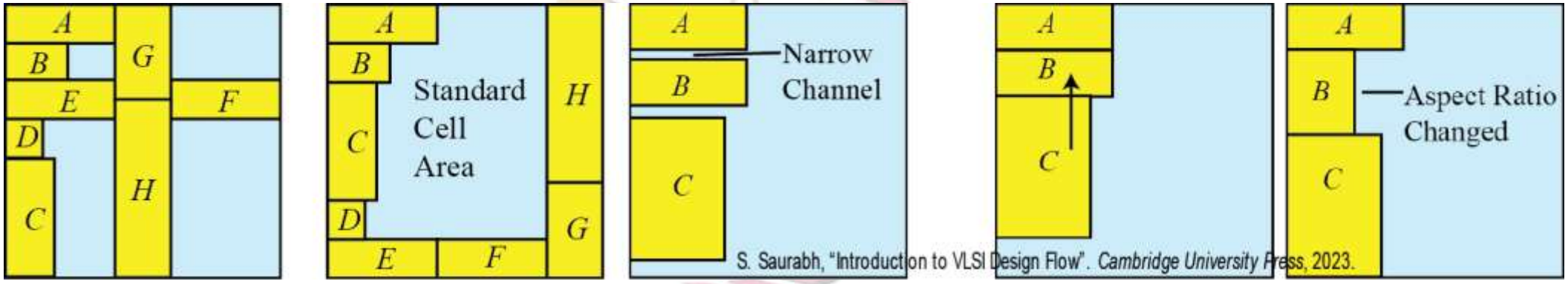
S. Saurabh, "Introduction to VLSI Design Flow". *Cambridge University Press*, 2023.

Macros Placement: Guidelines (1)

- Some guidelines can help in obtaining good floorplan

- Allot contiguous region for standard cells

- Avoid narrow channels between macros



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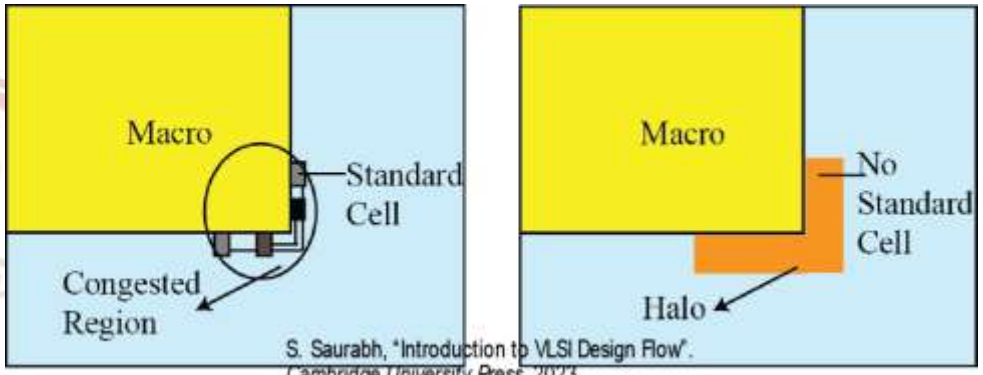
Macros Placement: Guidelines (2)

- Add halos around corners
  - ➢ Halos are placement blockages



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Use flexibility of:

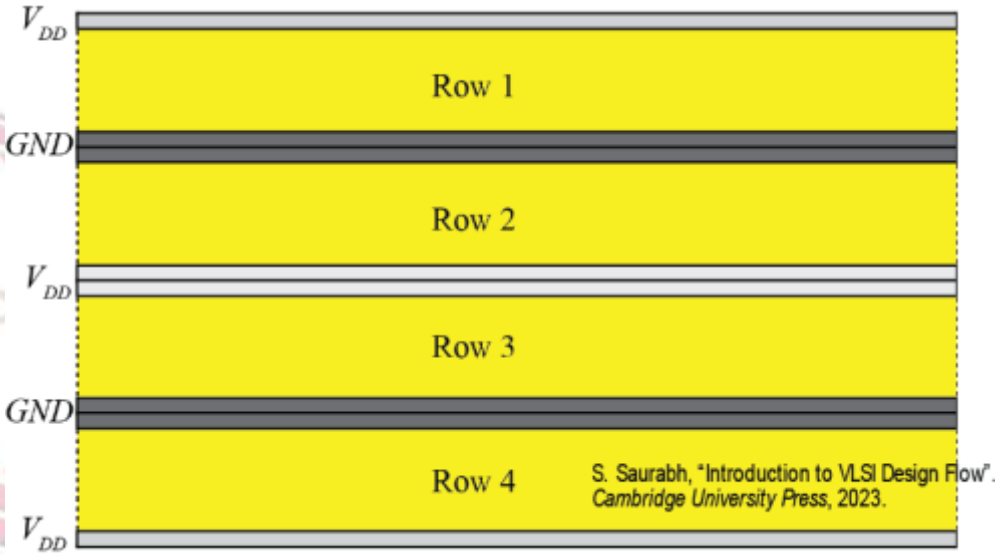
- Orientation: reflection, rotation by 90°
- Shapes: rectilinear
- Pin assignment: locations of movable pins

Floorplanning: Standard Cell Rows

- Height of standard cell rows is equal to the height of the standard cells in the library
  - ➢ Multiple rows of different heights created can also be created

- Standard cell rows generally created by abutment
- Rows are created oriented in alternating 180-degree rotation

- Routing channels can be created between rows to avoid congestion



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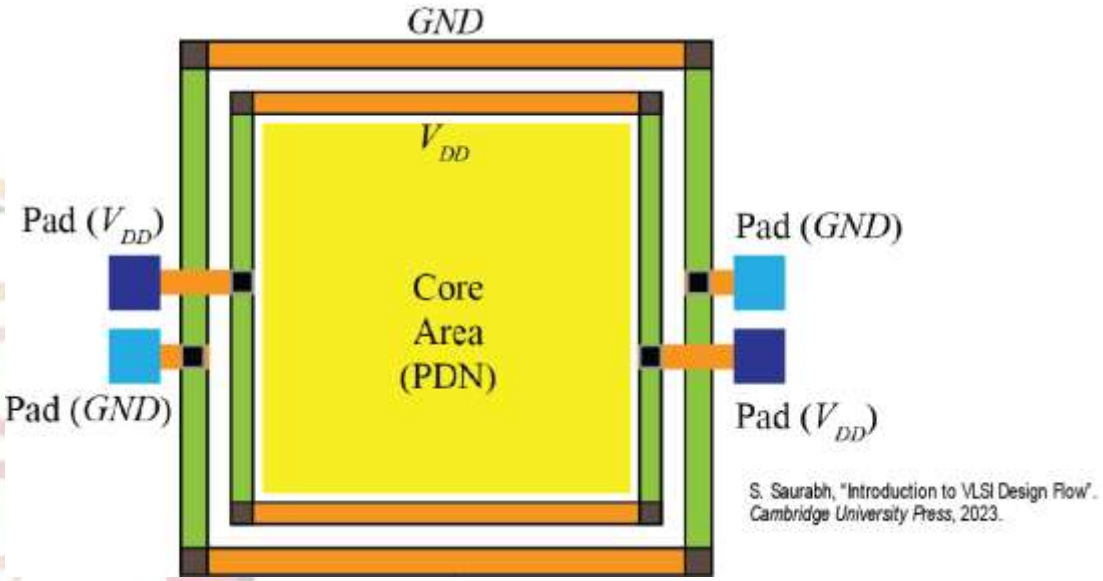
Power Planning

Power Planning: Components

- **Power Pads**: Supply power to the chip from the external world
- **Power Rings**: carry power around the periphery of the die
  - Usually use top metal layers
  - Power Delivery Network (PDN) built in the core area



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Power Delivery Network (PDN)

Mesh Grid Topology:

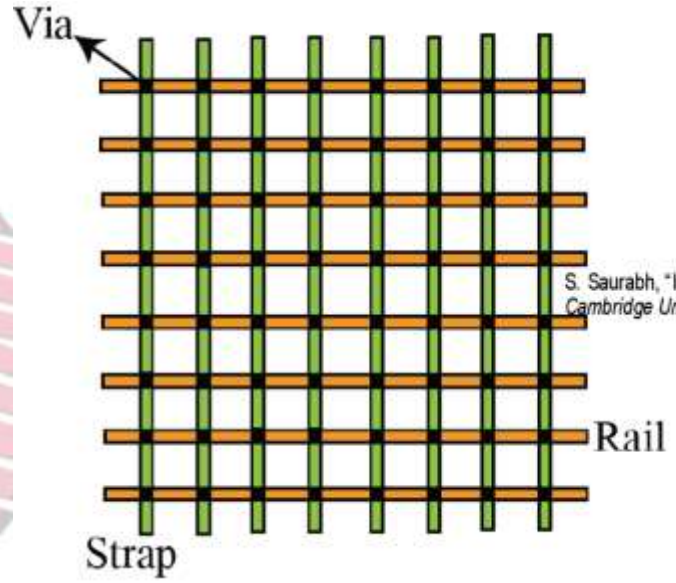
- Popular topology for PDN
- Rails and straps usually organized as a uniformly spaced array

Advantages of mesh grid topology

- Provides low resistance
- Reliability increases
- Uniform current distribution

Design Parameters:

- Layers in which the grid spans
- Width and spacing of wires



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Electromigration

Electromigration

- Flow of unidirectional current in a metal can causes **transport of metal mass** in the direction opposite to current flow
- Ions gain momentum from electrons
- May eventually lead to shorts and open

- PDN prone to electromigration
- Current in PDN needs to be kept within limit defined by process technology
  - Ensure conductor size is adequate
  - Ensure there are no current density "hot spots"

Voltage Drop

Cause of Voltage Drop:

- Resistance (R): between supply voltage origin and load
- Inductance (L): mainly between package-to-die interconnection
- Static and Dynamic Voltage Drop

$$Voltage = iR + L\frac{di}{dt}$$

Decoupling Capacitors (Decap Cells)

- Capacitors inserted between power and ground wires
  - ➢ Acts as local charge storage
  - ➢ Placed on die at strategic locations
- Demerits: increase die area and leakage power dissipation
- Number of decap cells, size and placement should be optimized

Impact on Performance

- Slows down signal propagation along the path
- Maximum frequency at which a circuit will operate is limited
- Need to perform voltage drop analysis in both static and dynamic conditions
  - ➢ Fix IR drop hotspots

References

- S. Saurabh, “Introduction to VLSI Design Flow”. Cambridge: *Cambridge University Press*, 2023.