VLSI DESIGN FLOW: RTL TO GDS

Lecture 30
Power Optimizations

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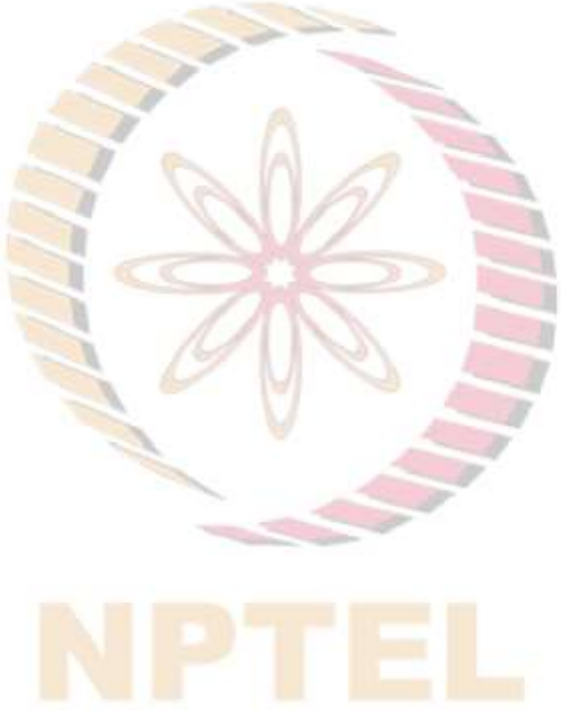
Lecture Plan

Overview of power-driven optimizations



Strategies for Reducing Power Dissipation

$$P_{tot} = C_L V_{DD}^2 \alpha f_{clk} + V_{DD} I_{SC} + V_{DD} I_{leak}$$

where,

- $V_{DD} =$ supply voltage
- $C_L =$ load capacitance
- $f_{clk} =$ frequency of the clock in the circuit
- $\alpha =$ activity of the signal

Power saving strategies:

- Reduce supply voltage
- Reduce clock frequency
- Reduce activity of the signal
- Reduce load capacitance

Dynamic Voltage Frequency Scaling (DVFS)

- Utilizes the strategy of reducing supply voltage and clock frequency

- Popular technique employed in processors:
  - Exploit variations in workload to save energy
  - Full speed of a processor is utilized by only a few tasks or for a small time duration.
  - For the remaining period, the deadlines can be met at low speed and consuming significantly less energy

Illustration:

- Consider a processor that can perform a task in 10 ms at 1.2 GHz and 1.2 V.
- Let us reduce the clock frequency and the supply voltage to half (600 MHz, 0.6 V),
  - Task will now complete in double the original time, i.e., 20 ms.
  - Will reduce the switching power dissipation by $1/8$ ($P_{tot} \propto V_{DD}^2 f_{clk}$)
  - Will reduce the energy consumption by $1/4$

Power Gating

- Utilizes the strategy of eliminating supply voltage

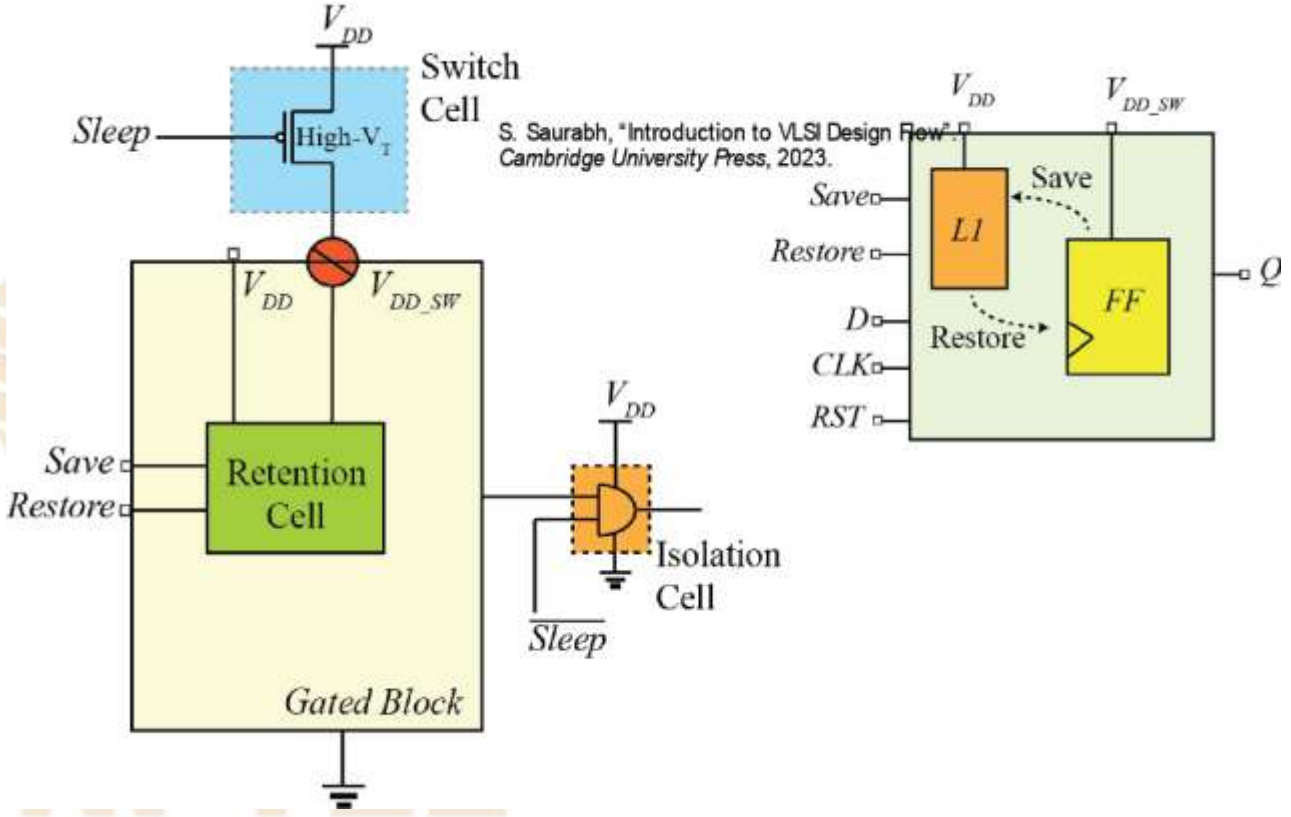
Power Gating:

- Switch off the power supply for a block
- Effective technique to tackle both static and dynamic components of power dissipation.
- Requires a careful circuit design and inserting specially designed circuit elements.

Power Gating: Circuit Elements

Circuit Elements

- Switch Cell
- Retention Cell
- Isolation Cell



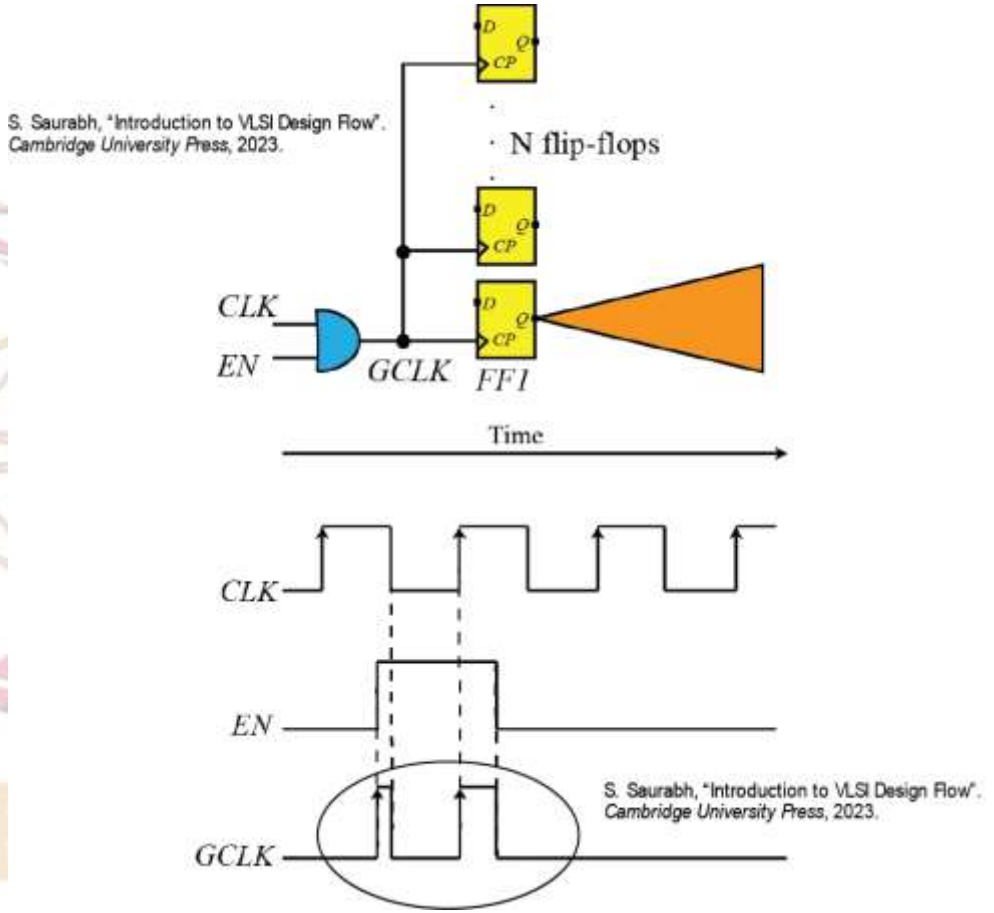
Clock Gating

- Utilizes the strategy of reducing activity

Assume that there is a set of N flip-flops that captures new data conditionally

- Shut off the clock when that condition is false
- Save power in charging/discharging capacitors in the clock network, including flip-flops
- Find enabling condition of clocking

- Simple AND of EN and CLK will lead to glitch

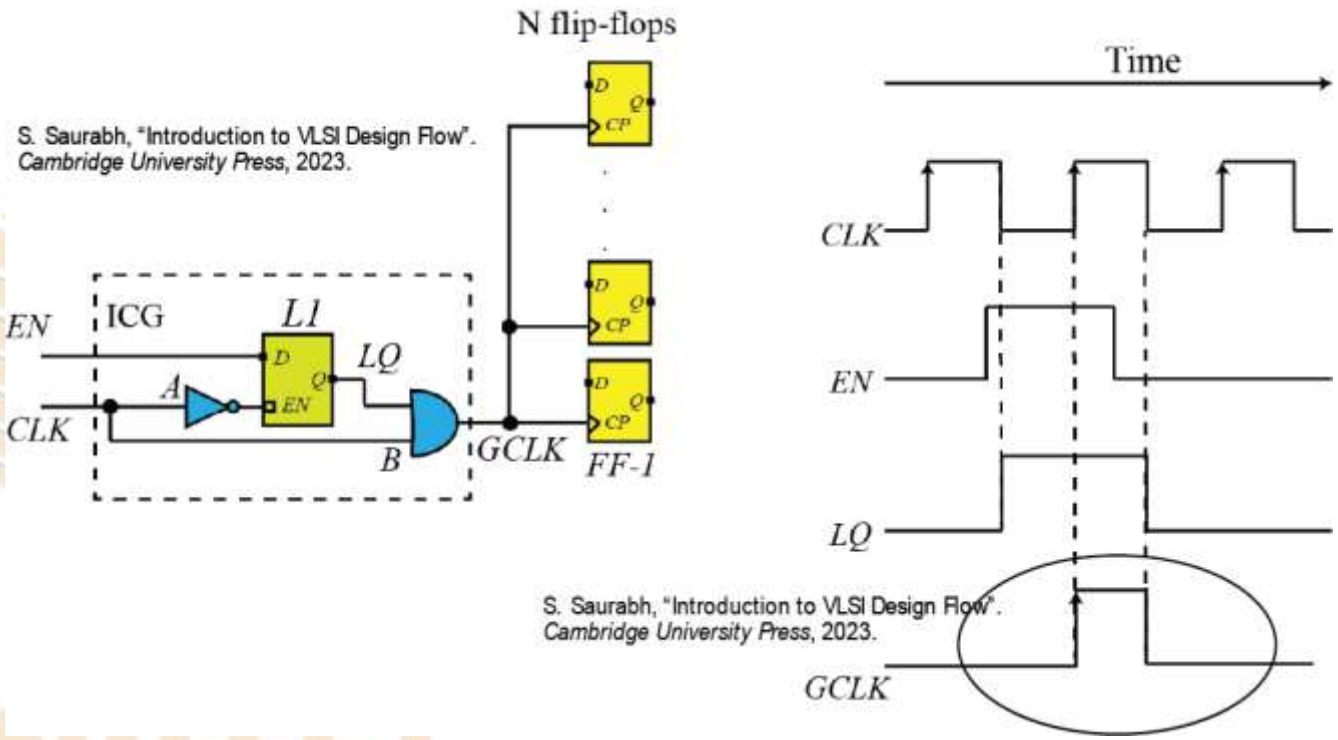


Clock Gating: Integrated Clock Gater

Integrated Clock Gater (ICG)

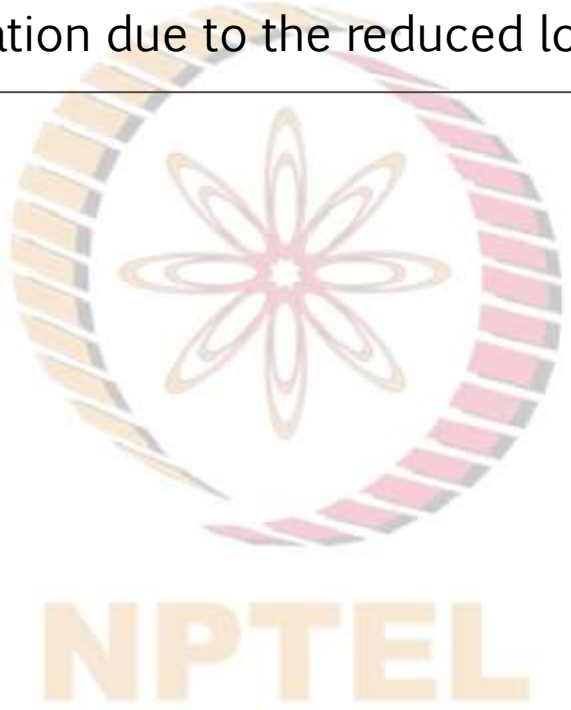
- Logic gate with an enable signal so that clock is propagated when the $EN = 1$

- Latch (negative sensitive) allows EN to propagate only when CLK is low
- When CLK is high, Latch (LT) output is stable and glitch cannot propagate



Resizing

- Resize cells to reduce power dissipation
  - For example, we can use smaller cells in the noncritical path of a circuit
  - Reduce the power dissipation due to the reduced load capacitances



References

- S. Saurabh, “Introduction to VLSI Design Flow”. Cambridge: *Cambridge University Press*, 2023.