VLSI Design Flow: RTL to GDS
(NPTEL Course)
Tutorial 5

1 Objective

To demonstrate the installation of RTL synthesis tool. Also, the working of the tool is explained with an example Verilog code.

2 Choice of Tools

- You can use the opensource tool YOSYS for the RTL systhesis.
- You can use any open-source tool for this lab activity.

3 Steps to install Yosys Open SYnthesis Suite [1]

- Install all prerequisites for building yosys:

```
$ sudo apt-get install build-essential clang bison flex \
      libreadline-dev gawk tcl-dev libffi-dev git \
      graphviz xdot pkg-config python3 libboost-system-dev \
      libboost-python-dev libboost-filesystem-dev zlib1g-dev
```

- Clone the GitHub repository

```
$ git clone https://github.com/YosysHQ/yosys.git
```

  once the cloning is completed, the yosys directory is formed. You can check by doing

```
$ ls
```

- Change directory to yosys

```
$ cd yosys
```

- Compile the source code

```
$ make
```

- Move all the application files to the appropriate system directories

```
$ sudo make install
```

This ends the installation process of the yosys tool. You can check the same by invoking the tool

```
$ ./yosys
```

The tool launches, and the command prompt changes to

```
yosys>
```

4 Steps to get the Technology Library file

- Go to the Silicon Integration Initiative (Si2) Public Download section https://si2.org/open-cell-library/
- Scroll down to find the Open-Cell and FreePDK Download Request Form and provide your details. It is important to input the details correctly, as these are verified.
- Fill out your name, your association, i.e. company/university, address of company/university, email address associated with company/university. Please make a note of their criteria: You must have a valid member company or university (.edu) email address to receive Open-Cell library download links. Download links will not be delivered to free or public email accounts.
- In the Si2 Membership Status select the option that applies to you. And lastly, select the FreePDK45 Library and submit.
- You can expect to receive the download link within a day, and it will remain valid for just three days. Therefore, it is advised to download the files as soon as you receive the email.
- Unzip and locate the library file as shown in Figure 1.

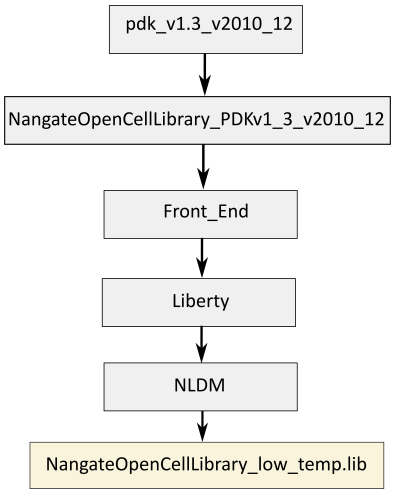

Figure 1: Libaray file location

- If you do not have the above-mentioned Nangate library for any reason, you can use the library file "toy.lib" instead. This library file is available on the NPTEL website as study material for Week 5.

5 Example code [2]

```
/*
* Verilog code to demonstrate the netlist synthesis
*/

module top(a, b, clk, select, out);
    input a, b, clk, select;
    output out;
    reg out;
    wire y;
    assign y=(select) ? b:a;
    always @(posedge clk)
    begin
        out<=y;
    end
endmodule
```

6 TCL script

```
# Read modules from Verilog file
read_verilog top.v

# Elaborate design hierarchy
hierarchy -check -top top

# Translate processes to netlists
proc

# Mapping to the internal cell library
techmap

# Mapping flip-flops to NangateOpenCellLibrary_typical.lib
# for e.g., always block
dfflibmap -liberty NangateOpenCellLibrary_typical.lib

# Mapping logic to NangateOpenCellLibrary_typical.lib
# for e.g., assign block
abc -liberty NangateOpenCellLibrary_typical.lib

# Remove unused cells and wires
clean

# Write the current design to a Verilog file
write_verilog -noattr  synth_example.v
```

7 Steps to perform the logic synthesis

- A comprehensive explanation for the commands used in this demonstration is provided here [3], [4].
- Launch the Linux distribution and `cd` to the directory where you have the required files, here it is `yosys_codes`.
- For netlist synthesis, you require a Verilog code for the implemented functionality, a library file, and a tcl script. The Synopsys Design Constraint (SDC) file is not provided, so the synthesized netlist will be mapped for minimum area constraints. Let's say my verilog code is named `top.v` and the library is `NangateOpenCellLibrary_typical.lib`
- Launch the yosys tool

```
$ yosys
```

- You can individually run the commands listed here [3]. I am using a tcl file.

```
yosys> script yosys_commands.tcl
```

- To view the generated netlist, close the yosys tool with `ctrl+Z`. Once you are back in the `yosys_codes` directory, you can check the contents of the directory using the command `ls`. To view the netlist:

```
$ gedit synth_example.v
```

References

[1] Installation steps for Yosys Open SYnthesis Suite. [Online]. Available: https://github.com/YosysHQ/yosys

[2] S. Saurabh, *Introduction to VLSI Design Flow.* Cambridge: Cambridge University Press, 2023.

[3] Yosys: Example Usage. [Online]. Available: https://yosyshq.net/yosys/

[4] Documentation for Yosys Open SYnthesis Suite commands. [Online]. Available: https://yosyshq.readthedocs.io/projects/yosys/en/manual-rewrite/cmd_ref.html