VLSI DESIGN FLOW: RTL TO GDS

Lecture 41
Routing

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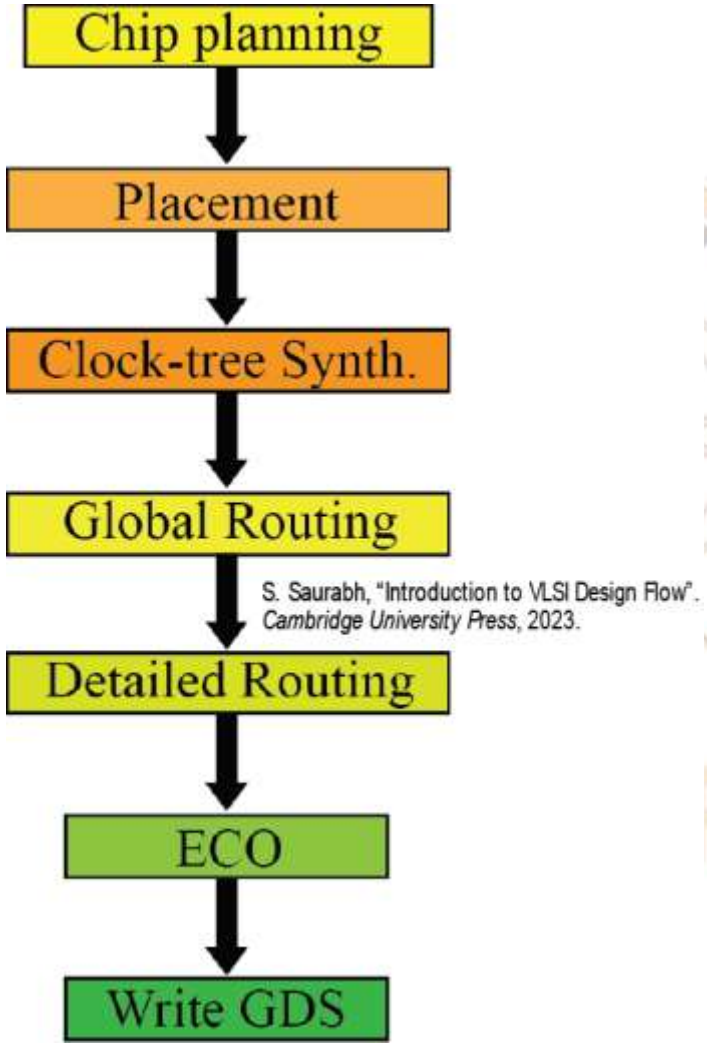
Lecture Plan

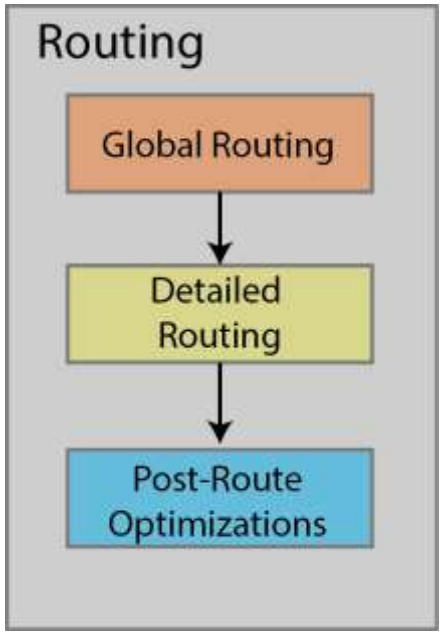


S. Saurabh, "Introduction to VLSI Design Flow". *Cambridge University Press*, 2023.

- Routing
  - Global Routing
  - Detailed Routing
  - Post-routing optimization

Routing: Basics

- Involves making physical interconnections between different components of a design
- Honor connectivity as in the given netlist
- Complicated and time-consuming task.
- Tight constraints (routing resources, design rules, timing, and signal integrity constraints)



Global Routing
- Creates the plan of routing for each net (in terms of *routing regions*)
- Actual layout of nets not created

Detailed Routing
- Decides actual layout of each net in the pre-assigned *routing regions*

Post-Routing Optimizations
- Localized changes to fix issues in the design

Global Routing: Goals and Objectives

Goal:

Provide complete instructions to the detailed router on where to route each net in a design

Objectives

- Maximize the probability that the detailed router can complete the routing
- Minimize Total Interconnect Length
- Minimize critical path delay

Desirable:

- Global Routing used in other design phases for estimates: prototyping, floorplanning, placement etc.
  - ➢ Need to be fast

Global Routing: Routing Model

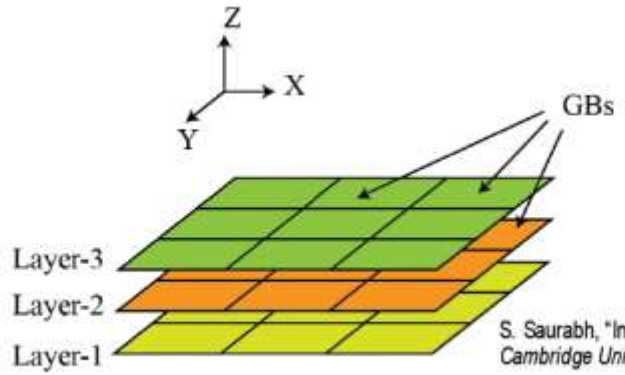
- Routing area is divided into rectangular grids
- Each rectangular region is called **Global Bin** (GB or global tile, routing tile global cell, or bucket)

Grid graph is built using GBs:

- Vertices (v): GBs
- Edges (e) : represent boundary between adjacent GBs
  - ➢ Create edges between two adjacent vertices only if they lie along the preferred direction of routing
  - ➢ Create edges between two vertices that lie vertically adjacent (for vias)

Determining a route for a net:

- Associate a pin with a vertex in the grid graph using the GB in which the pin is placed
- Find an ***optimal*** path in the grid graph that contains all the vertices for that net



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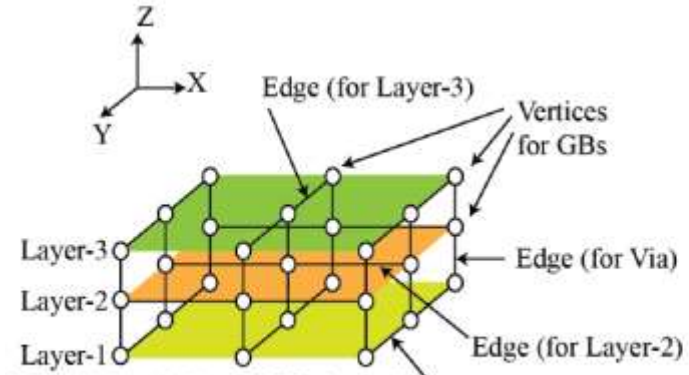

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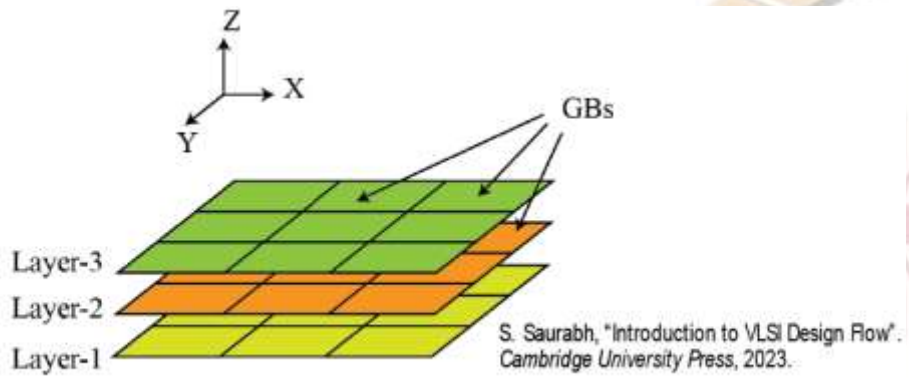
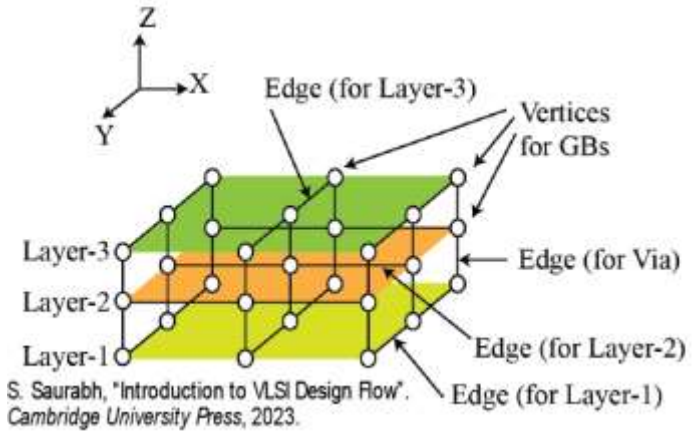
Global Routing: Routing Model

- When a net crosses the boundary of two GBs
  - ➢ Net utilized the corresponding edge





- $\boldsymbol{USE(e)}$: number of nets utilized for an edge
  - ➢ Also called ***demand*** for an edge

- $\boldsymbol{CAP(e)}$: quantifies availability of routing resources for an edge
  - ➢ Also called ***supply*** for an edge
  - ➢ Routing blockages limit the capacity
  - ➢ Depends on layer and design rules

Capacity constraint: $USE(e) \leq CAP(e)$

Overflow $OF(e) = USE(e) - CAP(e)$

Congestion $CG(e) = \frac{USE(e)}{CAP(e)}$

Global routing attempts to route all the nets such that $OF(e) = 0$

Global Routing: Challenges

Runtime versus Accuracy

- Runtime improvement:
  - Increased size of GBs
- Accuracy:
  - Anticipate problems that will be encountered by detailed routing (ease design closure)
  - Better modelling of routing resources and design rules

Detailed Routing

Detailed Routing: Goals and Constraints

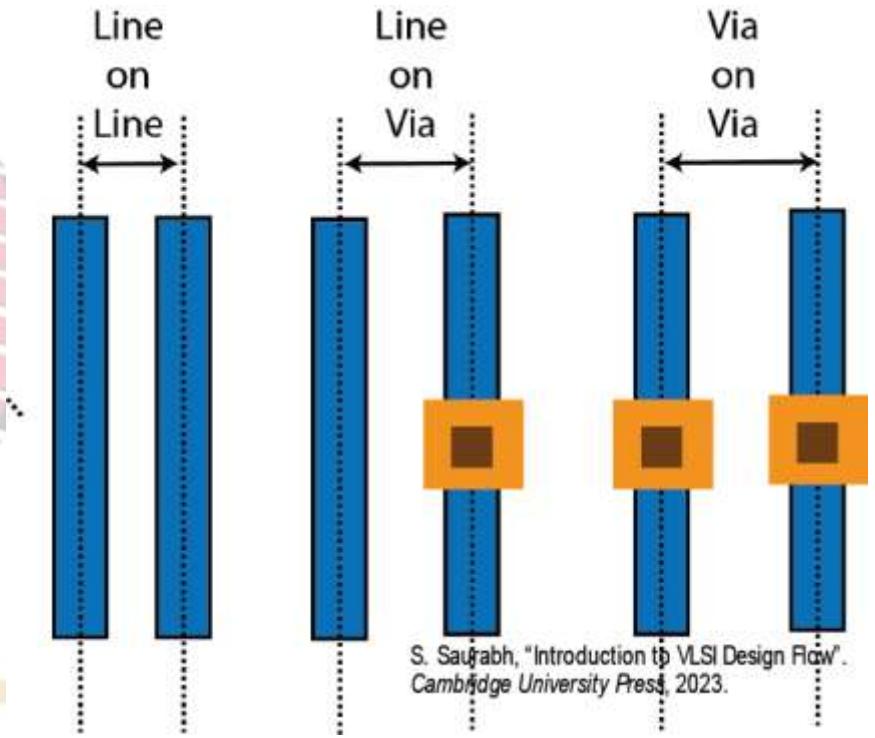
Goal: To determine the exact layout of each net, including all the attributes of wire segments such as width and location

Constraints and Considerations:

- Connectivity, design rules
- Timing, Signal Integrity, Runtime

- More number of metal layers available
  - ➢ Over-the-Cell (OTC) routing done
- Performed using a **detailed routing grid**
  - ➢ Tracks with uniform spacing (routing pitch)
  - ➢ Allows easy automation

- Routing pitch is defined as minimum spacing allowed in a technology (design rules):
  - ➢ Line on Line: can be too aggressive (DRCs)
  - ➢ Via on Via: can be too conservative
  - ➢ Line on Via: trade-off



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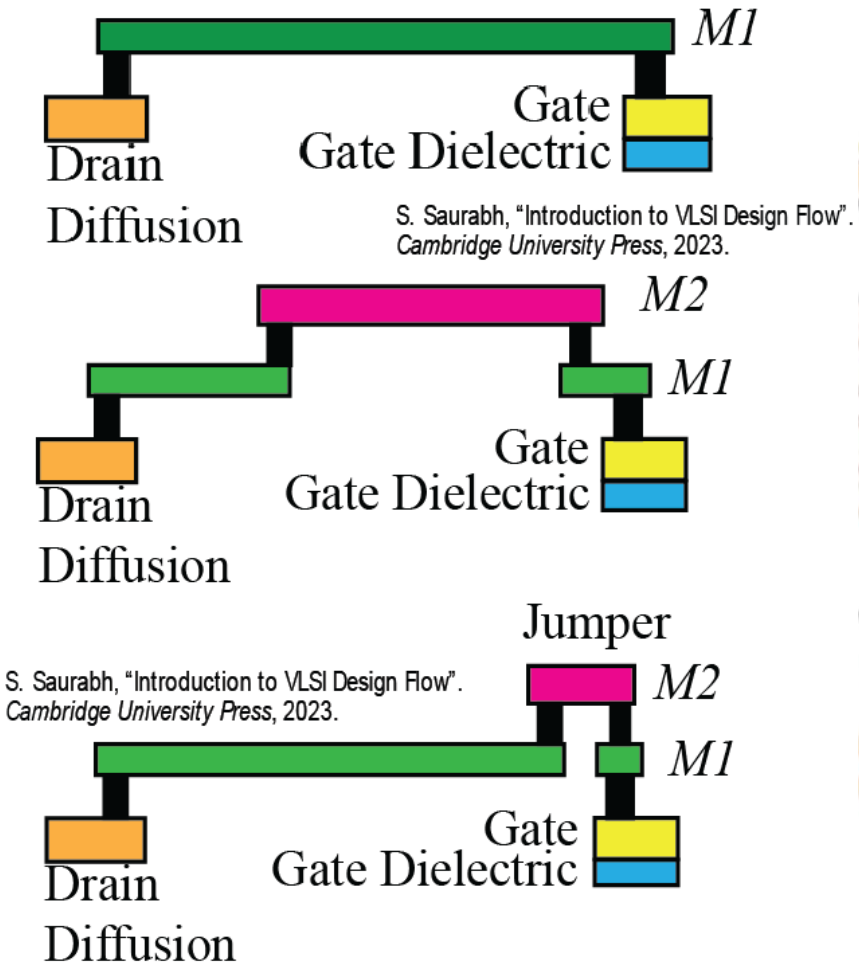
Routing: Final Optimization

- Timing analysis with interconnect layout and parasitics taken into consideration
- Improve timing issues by:
  - Gate upsizing, buffering, automatic/manual re-routing and wire widening

- Reduce power consumption: gate downsizing, removing buffers
  - Cell change with similar *footprint*

- Fix signal integrity issues
  - Increasing distance between wires

Antenna Effect



- Prone to antenna effect-induced gate damage

- Avoid long M1 line directly connected to the gate terminal
  - ➢ Instead use higher layer metal (M2) for routing

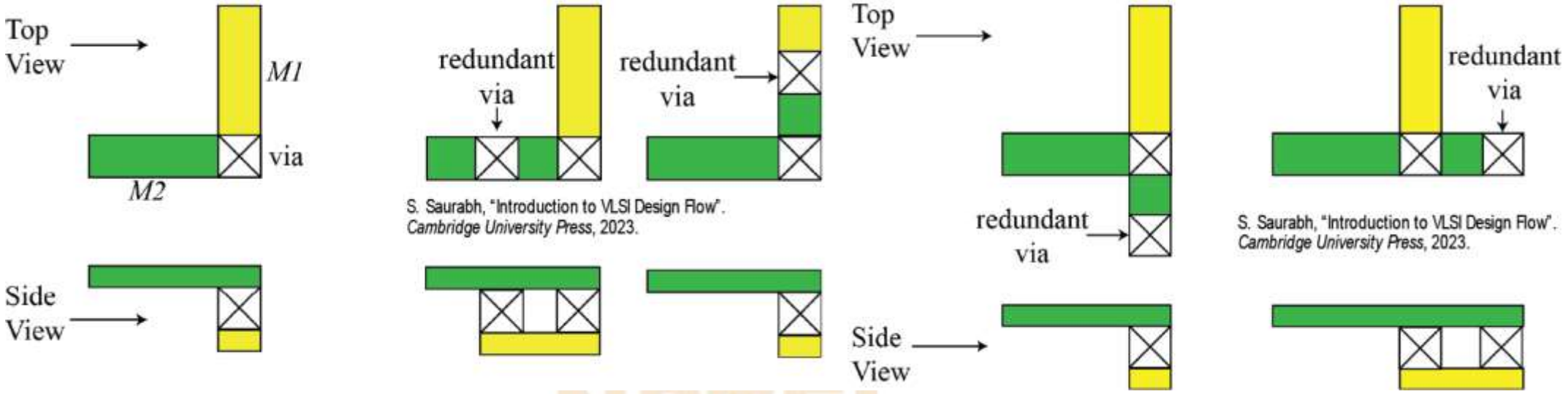
- Add a jumper to fix antenna rule violation after routing

Reliability Issues: Via Defects

Vias are prone to failure

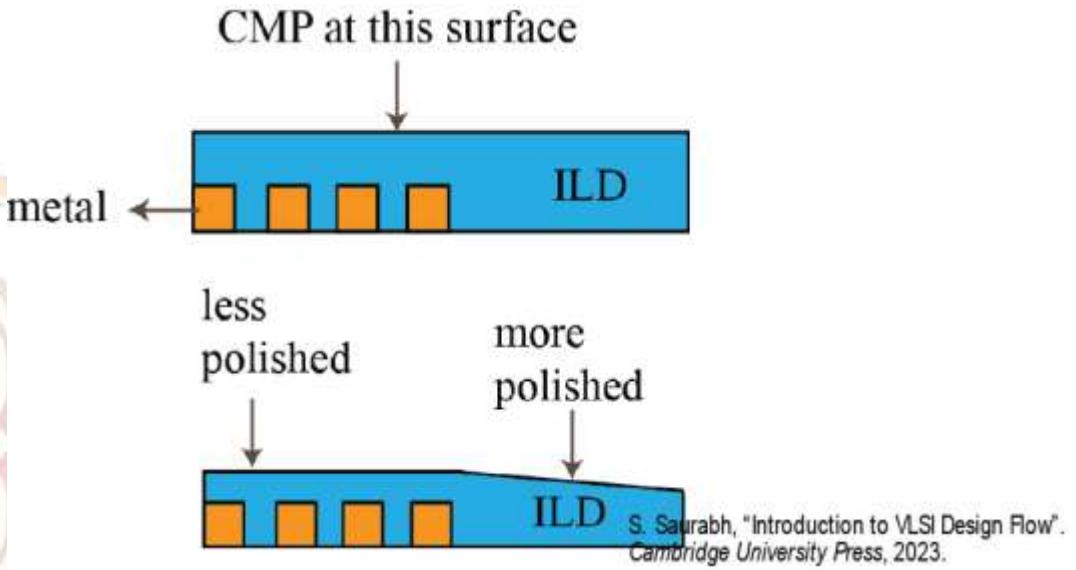
- Can lead to open circuit defects
- Yield loss and reliability problem

Solution: add redundant vias



Manufacturability Issues

- Difference in hardness of metal and dielectric, CMP can produce **irregular topography**



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- Irregular topography can lead to yield loss

- Add dummy ***metal fills*** during routing to ensure more uniform metal density

- The existence of dummy metal fills in the vicinity of current-carrying wires can affect the coupling capacitance.
  - Dummy metal fills can impact the timing of a circuit.

References

- S. Saurabh, “Introduction to VLSI Design Flow”. Cambridge: *Cambridge University Press*, 2023.