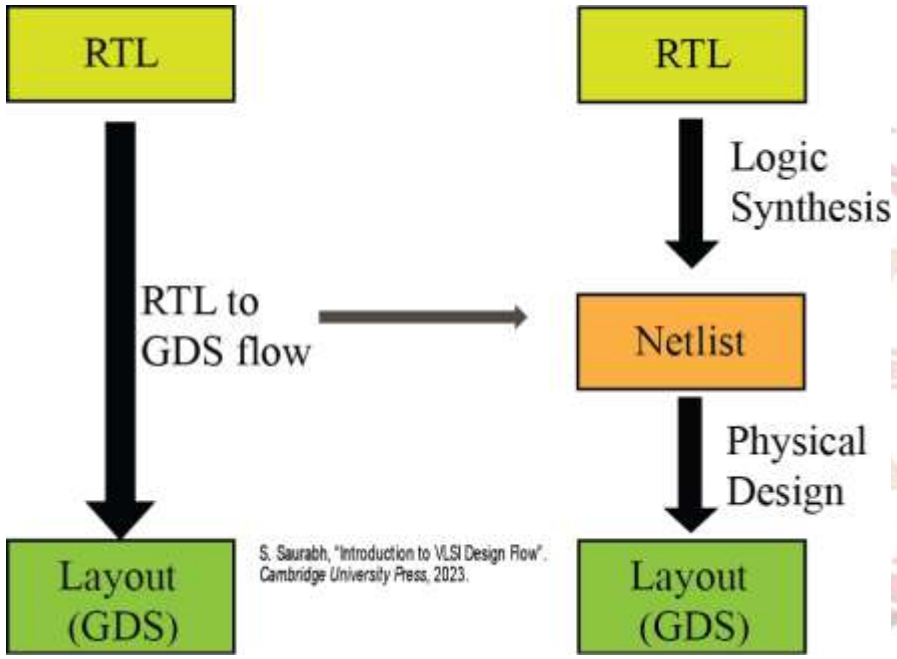
VLSI DESIGN FLOW: RTL TO GDS

Lecture 6
Overview of VLSI Design Flow: IV

Sneh Saurabh
Electronics and Communications Engineering
IIIT Delhi

Lecture Plan



S. Saurabh, "Introduction to VLSI Design Flow", *Cambridge University Press*, 2023.

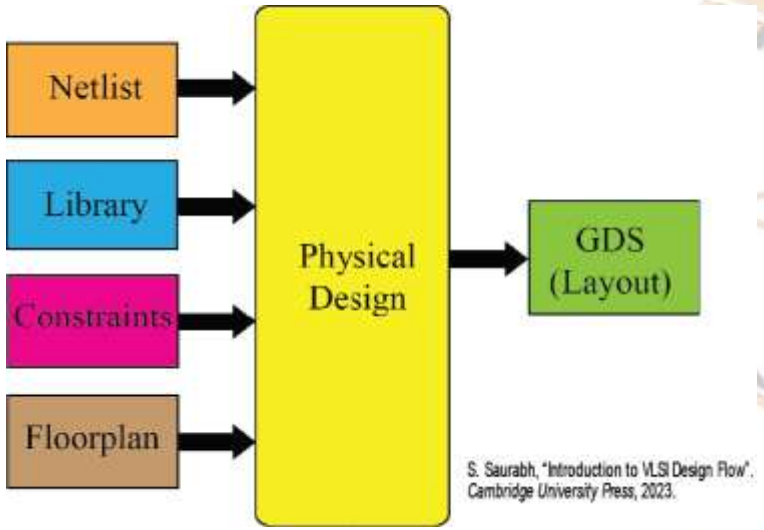
- RTL to GDS Implementation
  - Physical Design

Overview of RTL to GDS Flow

Physical Design

VLSI Design Flow: Physical Design

Physical Design: Process by which a design in the form of a netlist is converted to an equivalent design in the form of layout or GDS (geometrical patterns of masks)



Netlist: input design (output of logic synthesis)

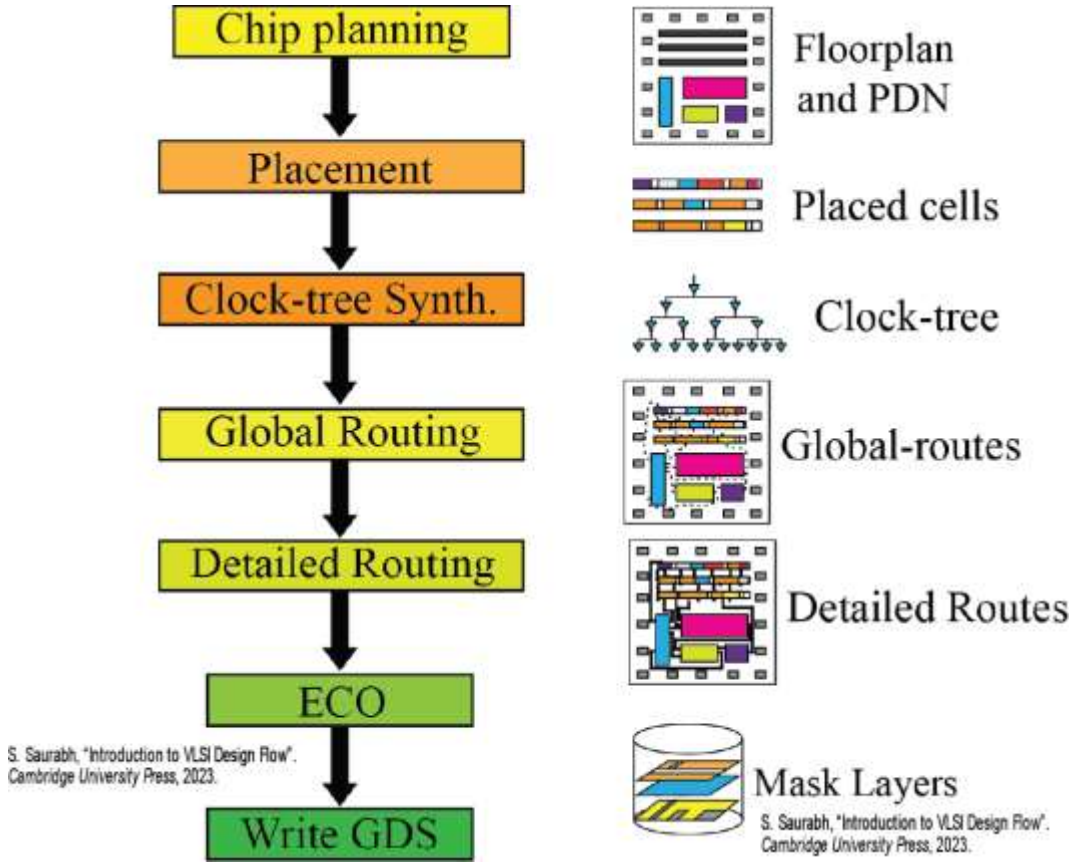
Library:

- Similar as in logic synthesis (Liberty)
- Abstract physical information of cells and technology-specific information (LEF)

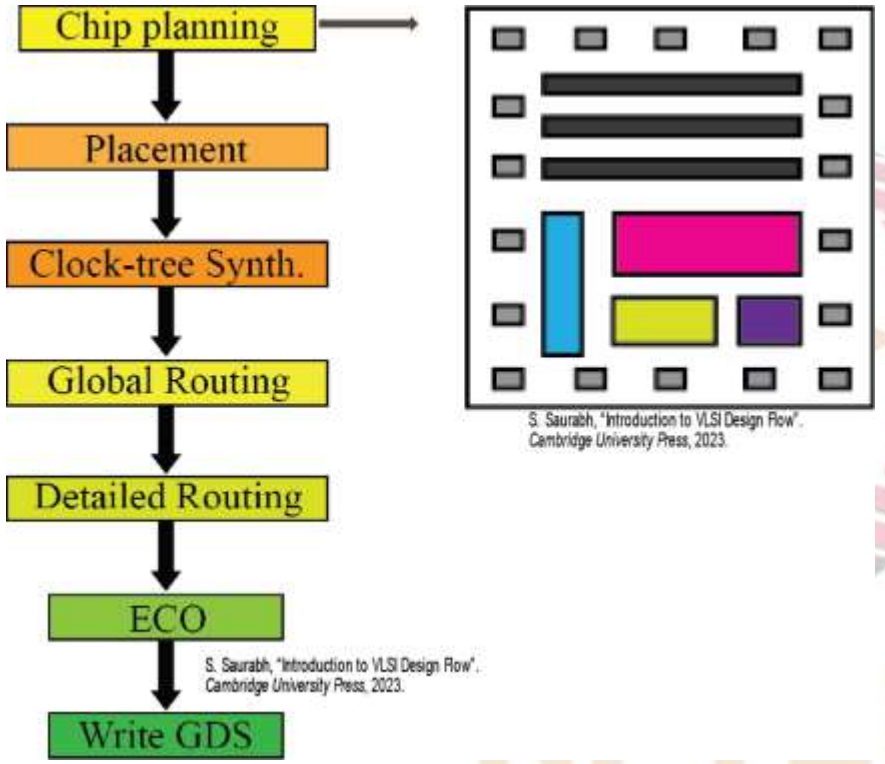
Constraints: design goals, expected timing behavior, environment (similar as in logic synthesis) (SDC)

Floorplan: designer's intent about the physical design (size and shape of die, predefined placement information)

Physical Design: Major Tasks



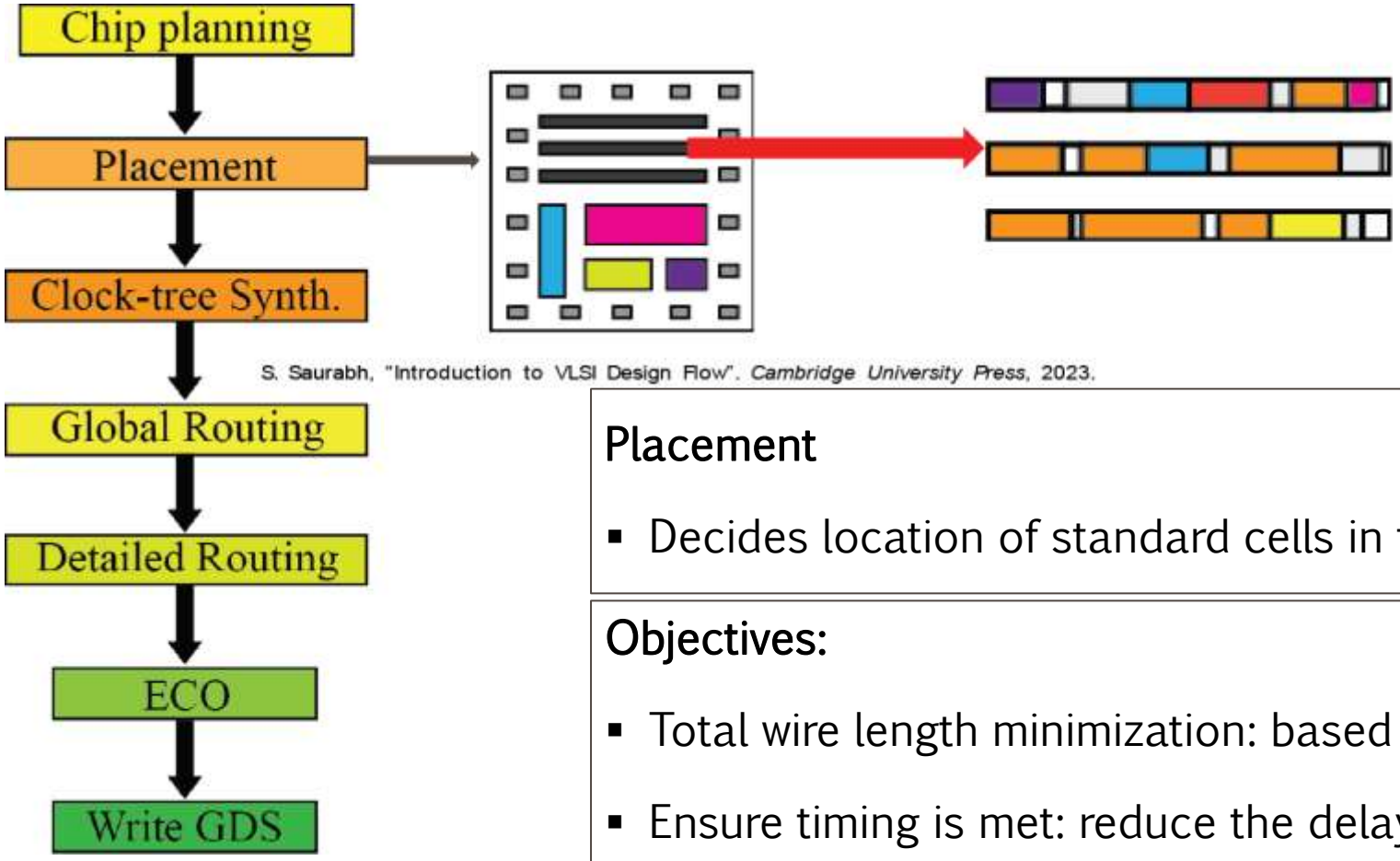
Physical Design: Chip Planning



Chip Planning

- First step in physical design in which we take major decisions
- Partitioning into subsystems or blocks
- Arrange the blocks on the chip/die
- Allocation of area for the standard cells, macros, memory
- Includes IO cell planning and Power Planning

Physical Design: Placement



S. Saurabh, "Introduction to VLSI Design Flow", *Cambridge University Press*, 2023.

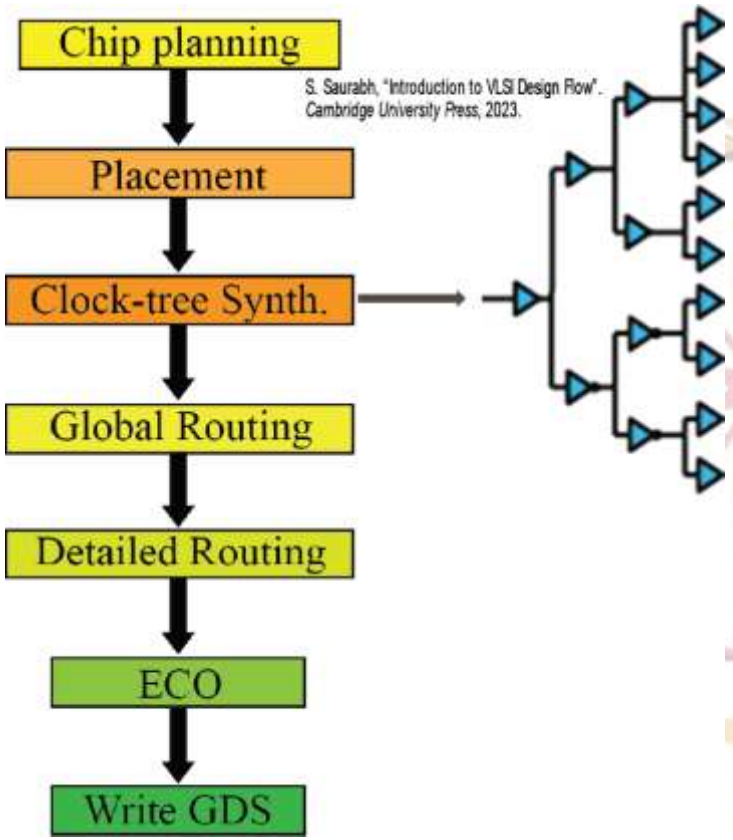
Placement

- Decides location of standard cells in the design

Objectives:

- Total wire length minimization: based on estimates
- Ensure timing is met: reduce the delay of the critical path
- Ensure no congestion

Physical Design: Clock Tree Synthesis



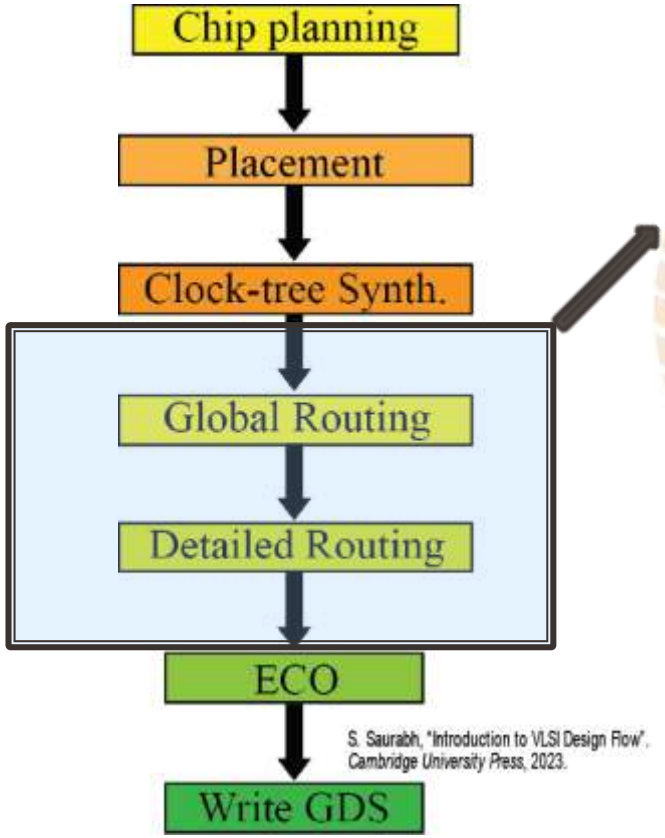
Clock Tree Synthesis (CTS)

- Decides topology of clock network and how clock reaches each clocked element
- CTS also performs wiring of clock network (avoids detour since majority of routing resources still unused)

Objectives:

- Ensure minimum skew: symmetric structure
- Minimize power dissipation: clock network consumes large fraction of total power

Physical Design: Routing

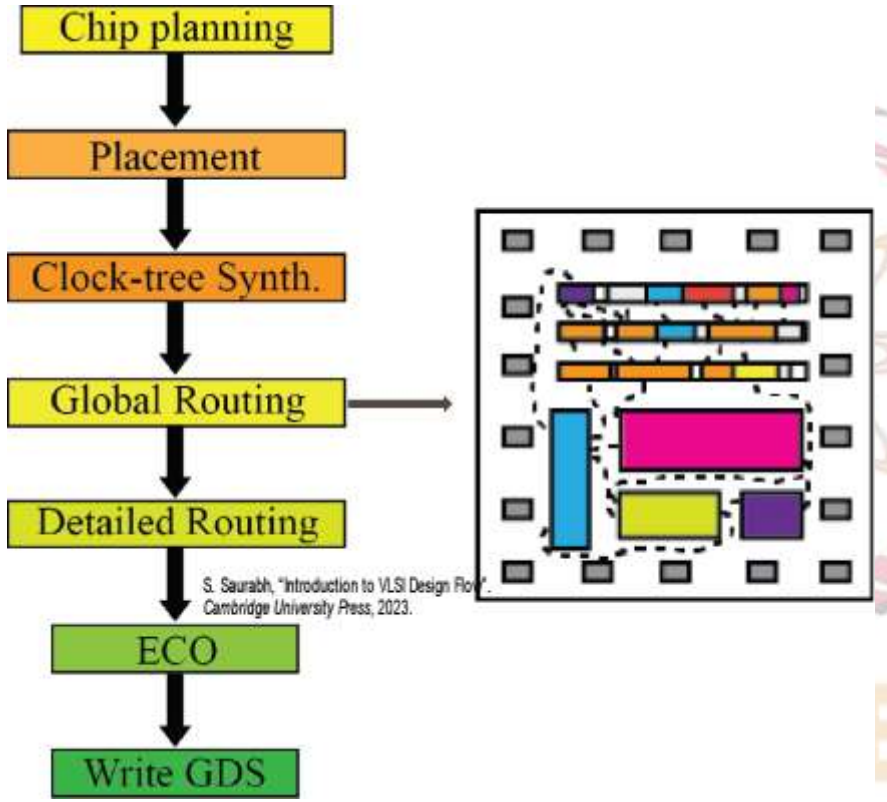


Routing

- Creates wire layout for all the nets (other than clock and power supply) satisfying certain constraints
- **Objective:** Use minimum wire-length, routing area, vias

- Very complicated process (too many nets and routing constraints)
- It is typically done in two steps:
  - Global Routing
  - Detailed Routing

Physical Design: Global Routing

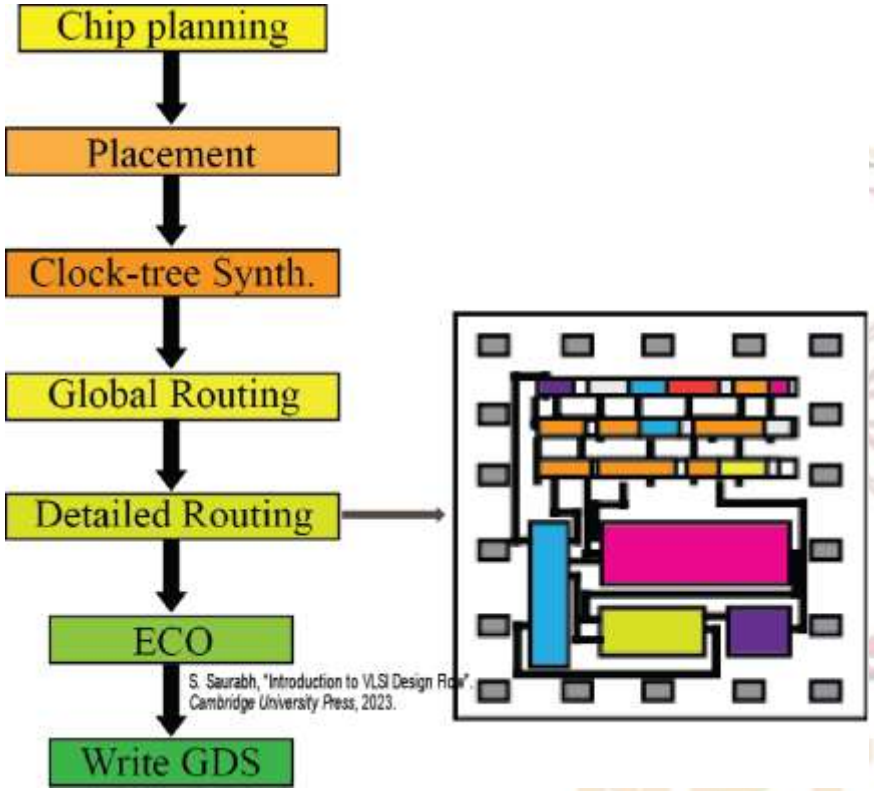


Global Routing

- Planning stage for routing
- Actual layout of wires not created
- A routing plan for a given net is created

- Entire routing region is partitioned into rectangular tiles or **global bins**
- Global routing assigns a set of global bins that will be used for making connections for a given net

Physical Design: Detailed Routing

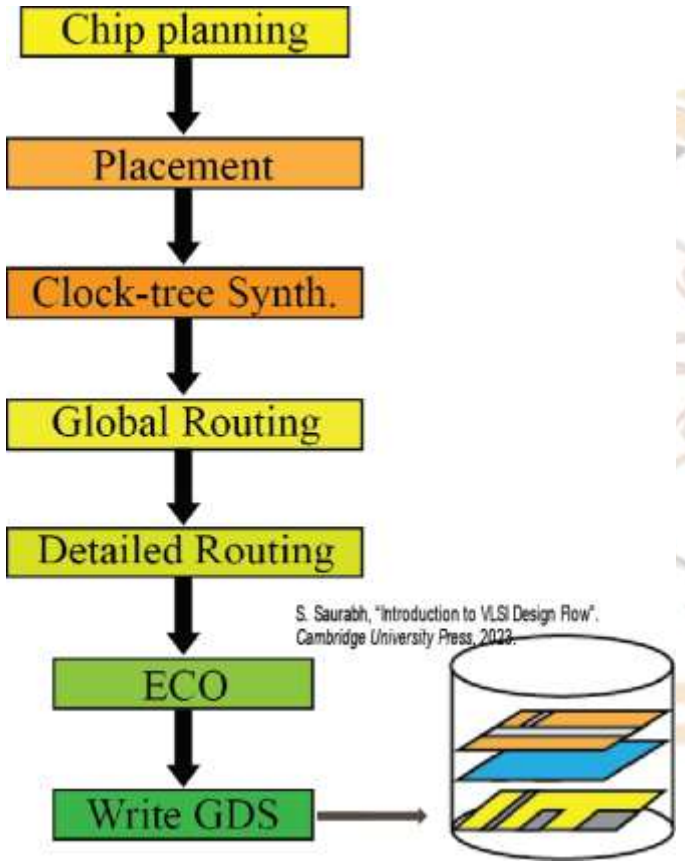


Detailed Routing

- Decides actual layout of each net in the pre-assigned global bins

- The detailed router decides the actual physical interconnections of nets by:
  - Allocating wires on each metal layer
  - Vias for switching between metal layers

Physical Design: ECO and GDS Writing



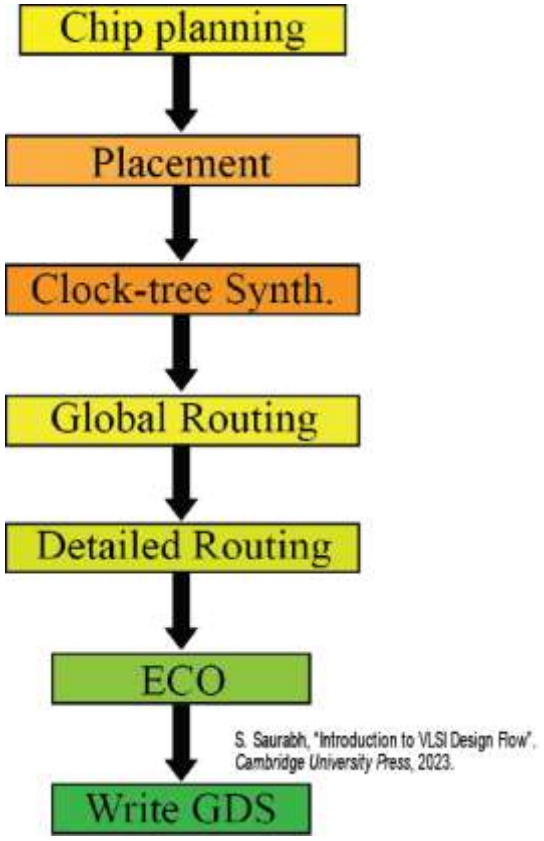
Engineering Change Order (ECO)

- Make small final fixes in the design

Write GDS

- Dump the layouts of each layer in a GDS file

Physical Design: Optimizations

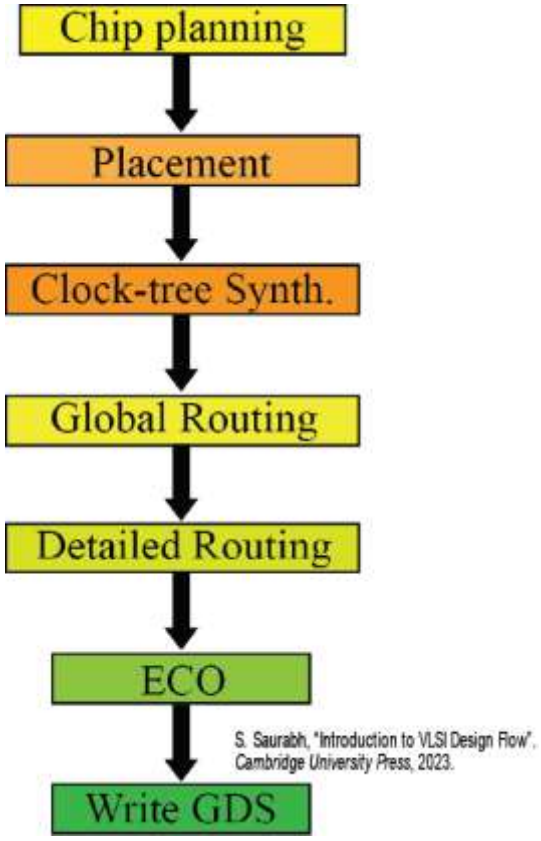


S. Saurabh, "Introduction to VLSI Design Flow", Cambridge University Press, 2023.

- Between each physical design task there are optimization steps:
  - ➢ Small changes in the design to improve PPA
  - ➢ Example of changes in the design:
    - ✓ Buffer insertion on a given net
    - ✓ Changes in the size of a given cell
    - ✓ Changes in the placement of a given cell
    - ✓ Changes in routing for a given net

- Incremental refinements to the design
- Changes are kept to be small and restricted to a small portions of a design
  - ➢ Do not create large disruptions in the design
  - ➢ Design flow should converge

Physical Design: Iterative flow



S. Saurabh, "Introduction to VLSI Design Flow", Cambridge University Press, 2023.

- Physical design implementation tasks performed along with verification tasks (timing, power, signal integrity, etc.)
- Physical design implementation should ensure design closure (including *timing* closure) [all constraints are satisfied]

- Achieving design closure is challenging
  - ➢ Design tasks do not have the full information and works with estimates that can be wrong

- Physical design flow is typically **iterative**
- One task may require that previous tasks retract some design decisions
  - ➢ This creates loops in the physical design flow

- Achieving design closure with minimum number of iterations is the goal of a physical design flow

References

- S. Saurabh, “Introduction to VLSI Design Flow”. Cambridge: *Cambridge University Press*, 2023.
- M. J. S. Smith. “Application-Specific Integrated Circuits,” vol. 7. *Addison-Wesley Reading*, MA, 1997.