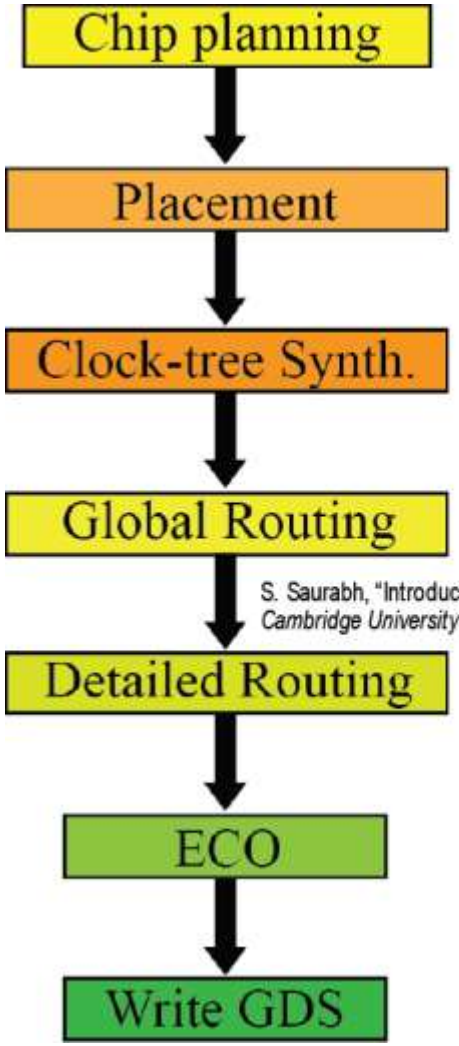
VLSI DESIGN FLOW: RTL TO GDS

Lecture 40
Clock Tree Synthesis (CTS)

Sneh Saurabh
Electronics and Communications Engineering
IIIT Delhi

Lecture Plan



S. Saurabh, "Introduction to VLSI Design Flow". *Cambridge University Press*, 2023.

Clock Tree Synthesis (CTS):

- Terminologies
- Clock Distribution Networks
- Clock Network Architectures
- Useful Skews

Clock Tree Synthesis (CTS): Basics

Ideal clock signal:

- Has the same waveform (voltage vs. time relationship) at all the points in the circuit.
  - ➢ No clock skew or no difference in the arrival time of the clock signal at the flip-flops

- Clock Tree Synthesis implements clock distribution structure on the layout having behavior similar to the ideal clock
  - ➢ Minimizes the clock skew
  - ➢ Inserts clock buffers/inverters and performs routing of clock distribution network

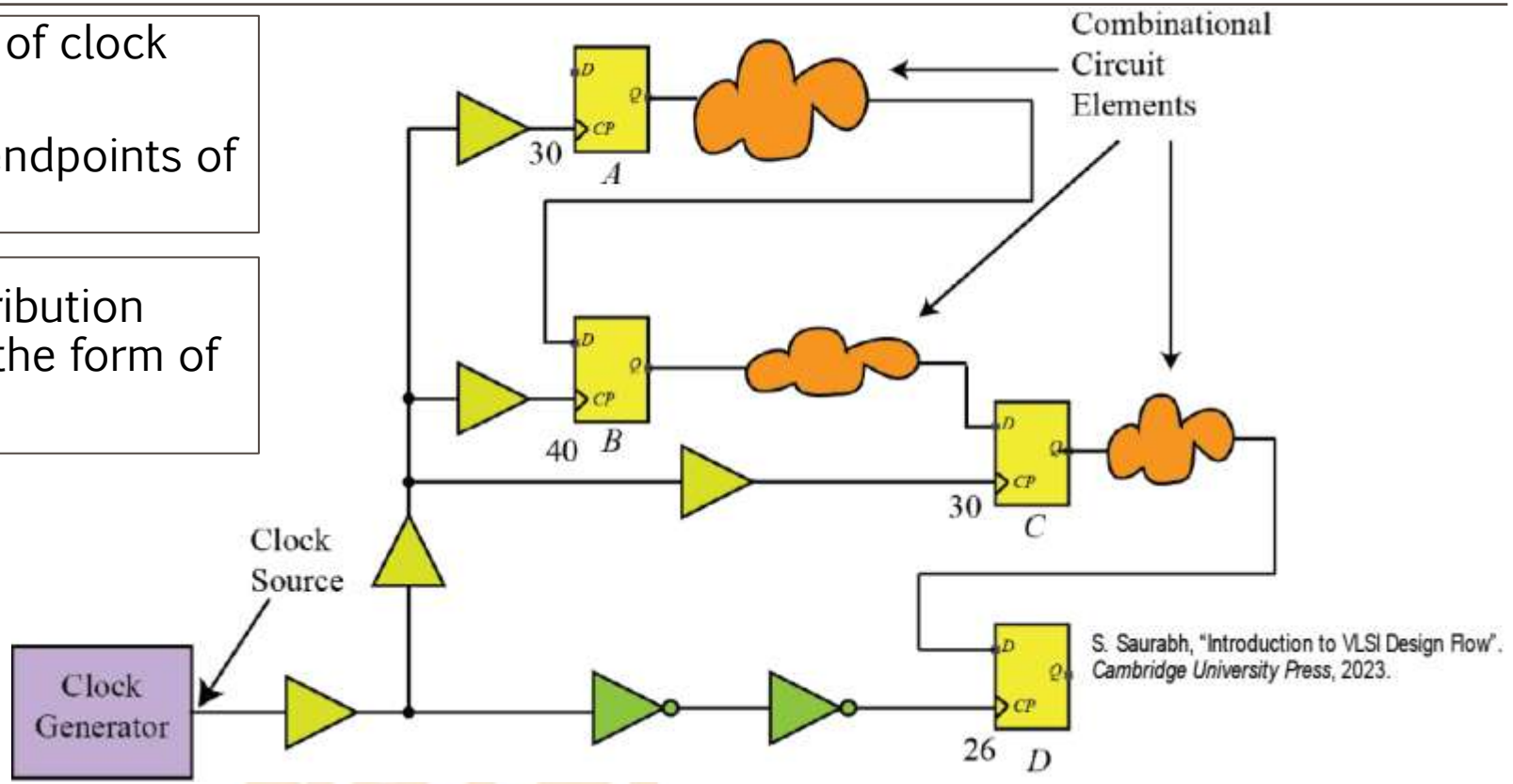
- Targets power reduction
  - ➢ Clock network consumes significant portion of total active power $(25\% - 70\%)$
- Fixes timing violations and signal integrity issues

CTS: Terminologies (1)

Source: starting point of clock signal

Sinks: final receiving endpoints of the clock signal

Clock Tree: clock distribution network organized in the form of a tree



Insertion Delay/delay/latency: time taken by the clock signal to propagate through a clock tree and reach a clock sink

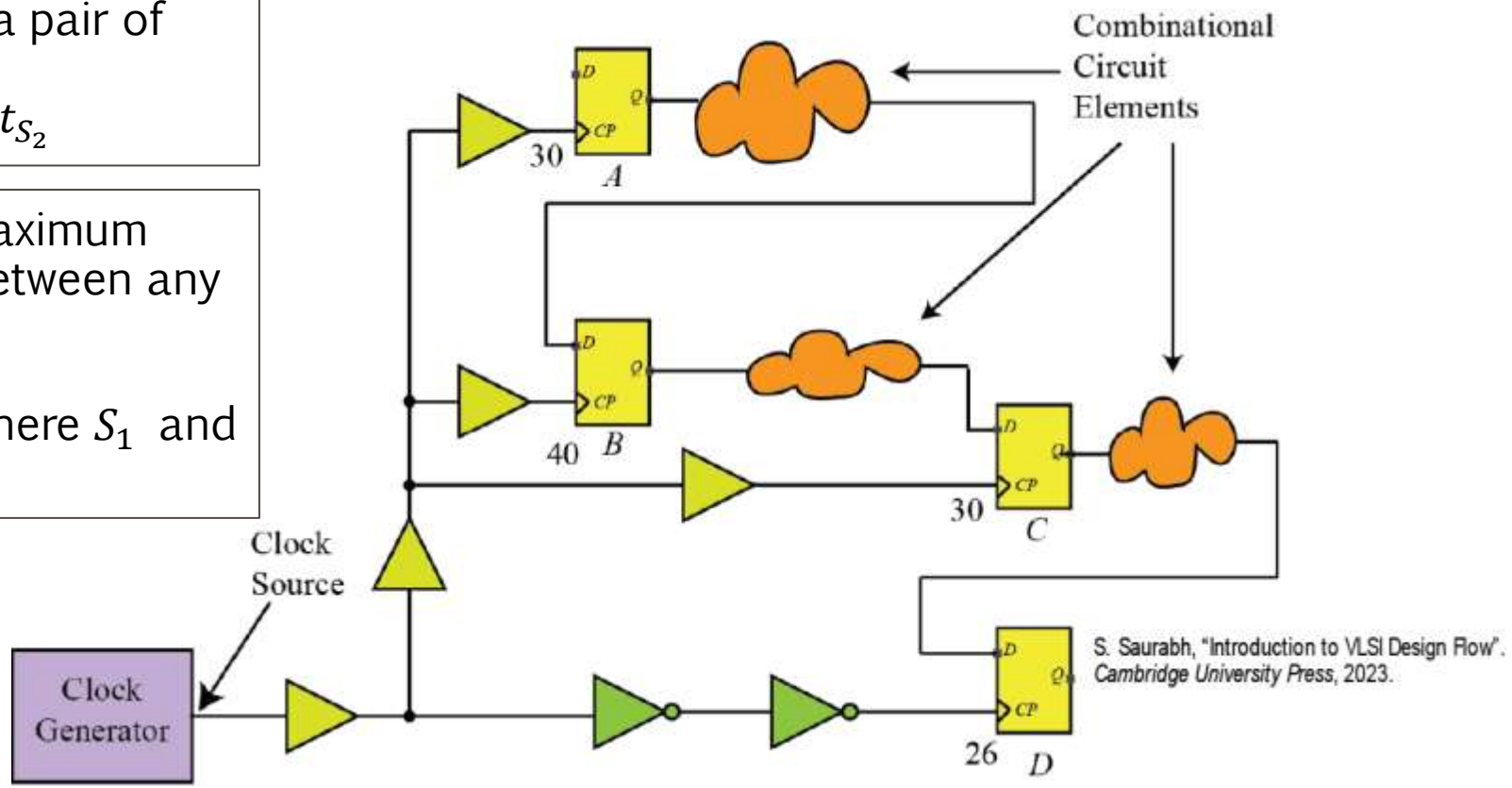
CTS: Terminologies (2)

Clock Skew between two sinks: difference in the arrival time of clock signal between a pair of sinks S_1 and S_2, i.e.,

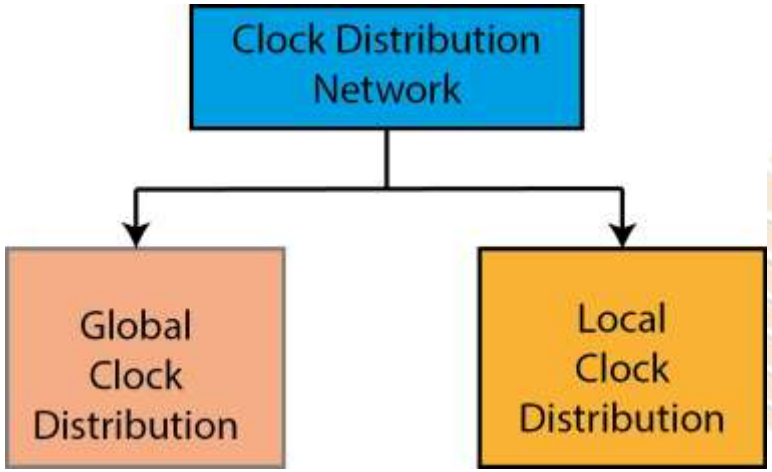
$$\delta_{S_1 S_2} = t_{S_1} - t_{S_2}$$

Global Clock Skew: maximum value of clock skew between any pair of sinks

$\Delta_{global} = Max|\delta_{S_1 S_2}|$ where S_1 and S_2 are sinks



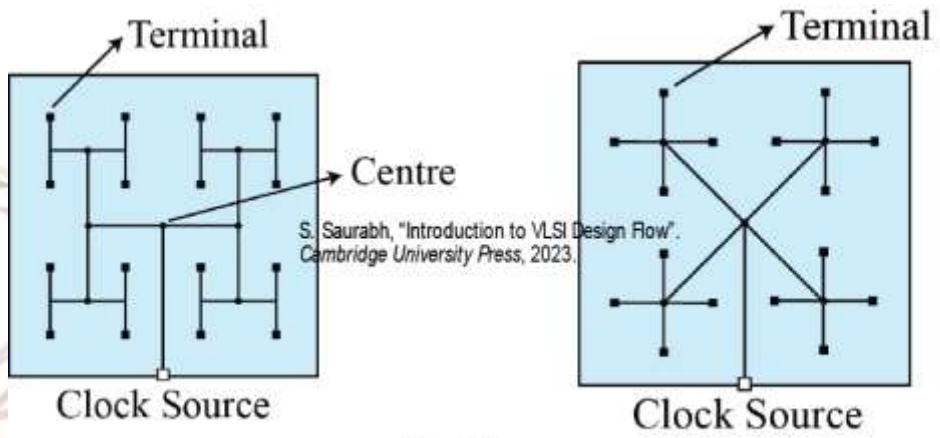
Clock Distribution Network



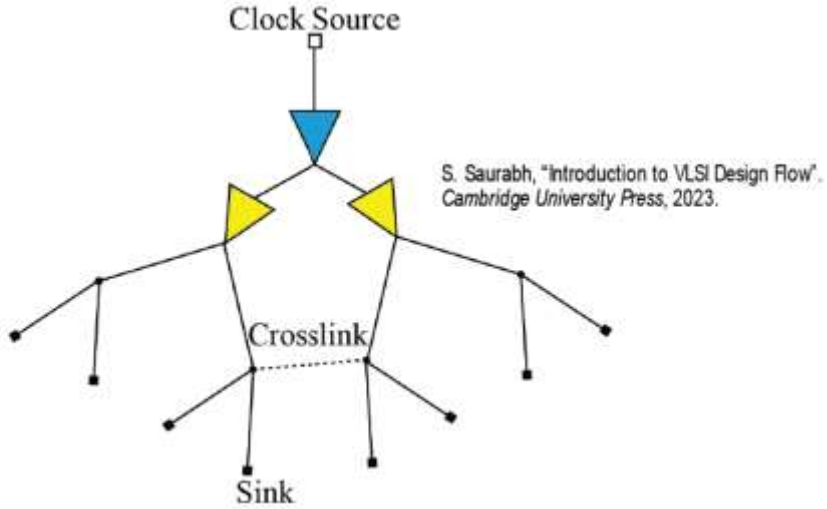
Global Clock Distribution	Local Clock Distribution
Distributes clock to various parts of chips and over large area	Distributes clock to smaller parts of circuits
Clock Buffers are large and more	Clock Buffers are smaller and fewer
Consume large power	Consume less power
Top-level Clock Distribution Network needs to be planned	Automated Clock Tree Synthesis can be used

Symmetric Tree Architecture

- Clock is first routed to a central point in the chip
- From central point another symmetric architecture forks out
- Example: H-Tree, X-Tree



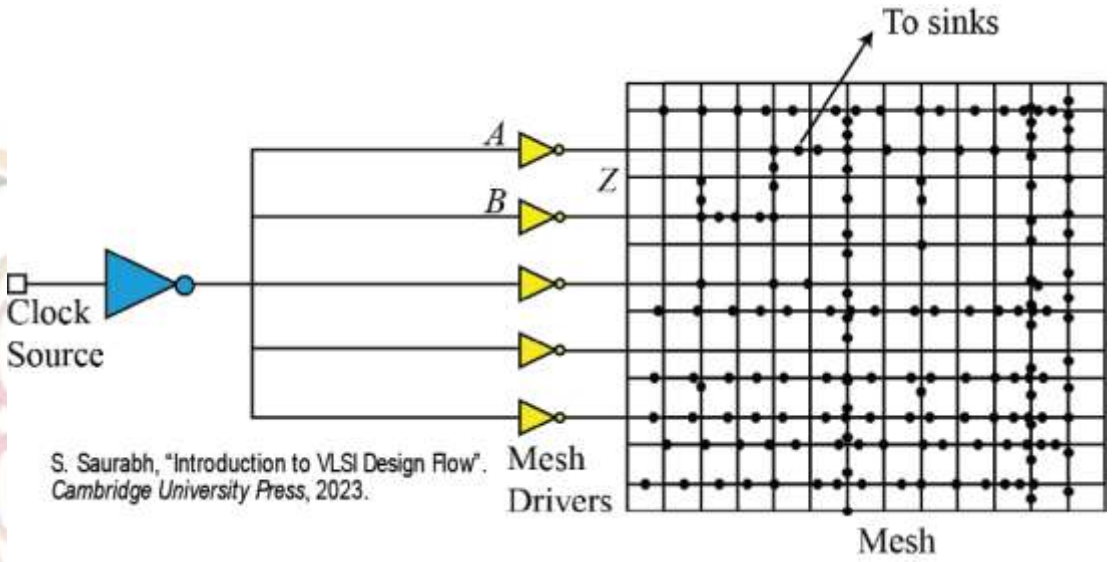
- Ideally if each path is balanced, skew will be zero
- Due to PVT variations, skew is still observed
- Non-tree architecture can reduce impact of PVT variations



Mesh Architecture

- Create 2-D structure with redundant wires and devices

- Ensures more paths between mesh drivers and clock sinks
  - ➢ Very small skew
  - ➢ Decreased impact of process induced variations
  - ➢ Robust



S. Saurabh, "Introduction to VLSI Design Flow". *Cambridge University Press*, 2023.

Disadvantages:

- ➢ Increases total capacitance and the size of clock drivers
- ➢ Increases power consumption (due to increased capacitance and short-circuit power dissipation)

Useful Skews

- Introducing well-controlled skews can improve the system performance (useful skews)

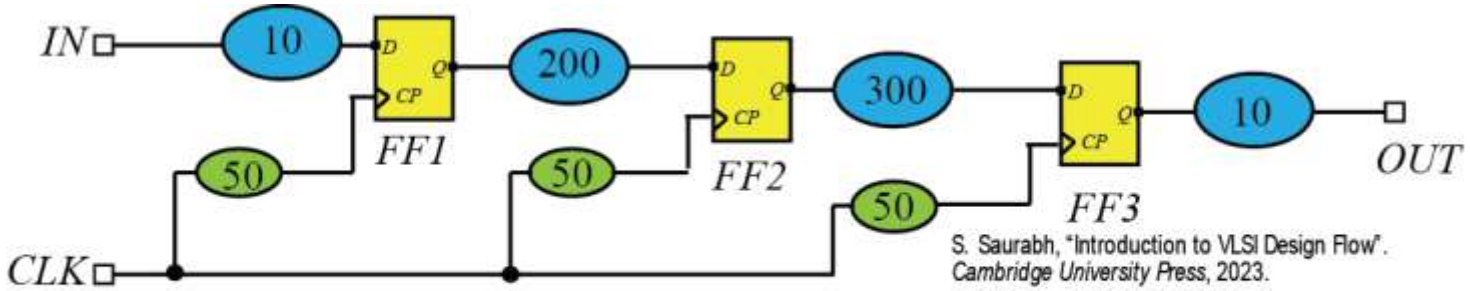
When can clock skews be useful?

- If a significant difference in the slack exists on the two sides of a flip-flop

Technique:

- Allocate the excess margin on one side of the flip-flop to the more critical path side
  - Provide more time for data to propagate on the critical path

Useful Skews: Illustration

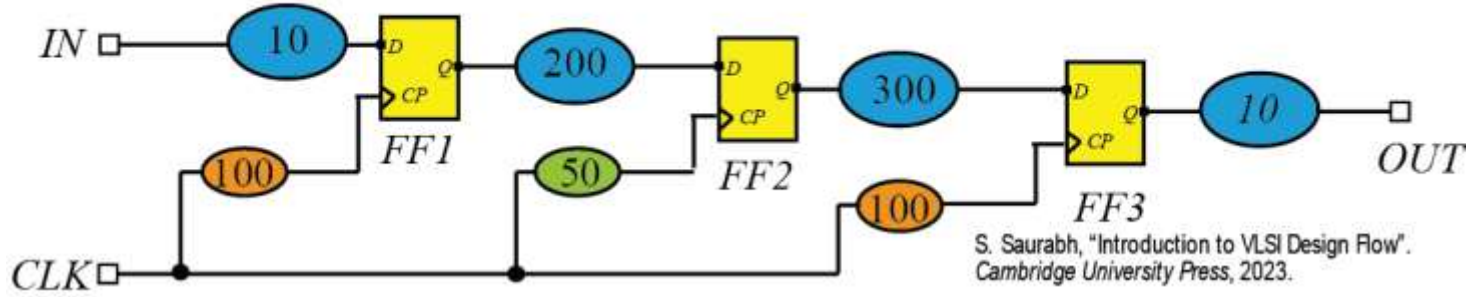


S. Saurabh, "Introduction to VLSI Design Flow". *Cambridge University Press*, 2023.

$$50 + 200 < T_{period} + 50$$
$$\Rightarrow 200 < T_{period}$$

$$50 + 300 < T_{period} + 50$$
$$\Rightarrow 300 < T_{period}$$

$$f_{max} = \frac{1}{300ps} = 3.33\ GHz$$



S. Saurabh, "Introduction to VLSI Design Flow". *Cambridge University Press*, 2023.

$$100 + 200 < T_{period} + 50$$
$$\Rightarrow 250 < T_{period}$$

$$50 + 300 < T_{period} + 100$$
$$\Rightarrow 250 < T_{period}$$

$$f_{max} = \frac{1}{250ps} = 4\ GHz$$

Obtaining Useful Skews

- CTS tools calculates useful skew targets for all critical registers
- Increase arrival time of the clock for target registers by addition of delay buffers or extra wires

- Useful skew also helps in reducing voltage drop problems
  - Registers do not switch at the same time
  - Simultaneous current drawn is less

CTS: Post Optimization

- Before CTS clocks were ideal
- After CTS clock network is fully built
- Need to inform STA tool to use actual delays on the clock path

```
set_propagated_clock [all_clocks]
```

- New timing violations may show up after CTS
  - Due to additional skew
  - Due to some logic in data path moved out (placement changed) due to addition of buffers in clock network

- Clock Network is frozen after post-CTS optimization and very small ECO fixes are allowed

References

- S. Saurabh, “Introduction to VLSI Design Flow”. Cambridge: *Cambridge University Press*, 2023.