VLSI Design Flow: RTL To GDS (NPTEL Course)

Tutorial 6

Objective: To gain a hands-on experience on Logic Optimization using Yosys

Requirement:

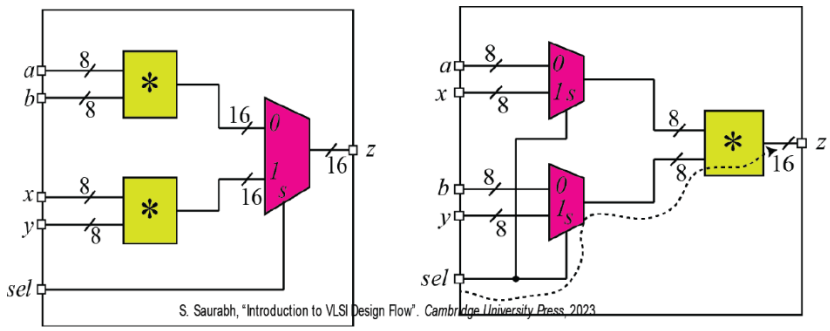
- **Yosys**: The installation and how to run Yosys is described in Tutorial 5. Please refer to it if you do not have Yosys installed on your machine.
- **Files:**
  - Design file: top.v
  - Yosys script files: opt.tcl, not_opt.tcl
  - Technology library: toy.lib

  All the above files are available on the NPTEL website as study material for Week 6

Optimization:

From Lecture 13 (Resource Sharing):

```
if (sel == 1'b0) z = a*b;
else z = x*y;
```



Experiment: Run Yosys and observe resource sharing and how it leads to decrease in area.