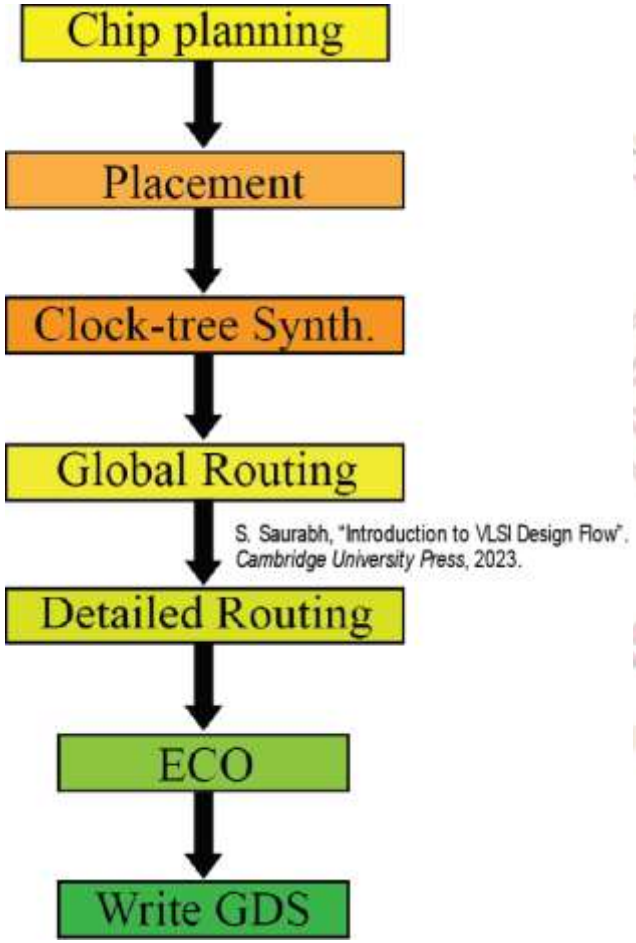
VLSI DESIGN FLOW: RTL TO GDS

Lecture 39
Placement

Sneh Saurabh
Electronics and Communications Engineering
IIIT Delhi

NPTEL

Lecture Plan

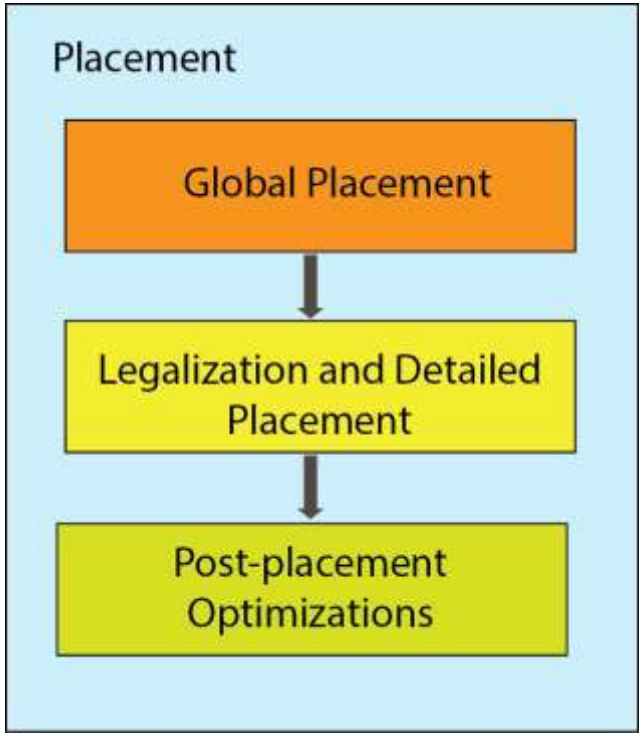


S. Saurabh, "Introduction to VLSI Design Flow", *Cambridge University Press*, 2023.

- Placement
  - Global Placement
  - Legalization and Detailed Placement
  - Scan Cell Reordering
  - Spare Cell Placement

Placement: Basics

- Decide locations of standard cells
- Goal: to ensure routability of a design
- Metrics: total wirelength
  - Other metrics: timing, congestion



- Global Placement
  - Cells are spread over the core area
  - Overlap may exist

- Legalization and Detailed Placement
  - Overlap between cells removed
  - Cells moved to “legal” positions (legalization)

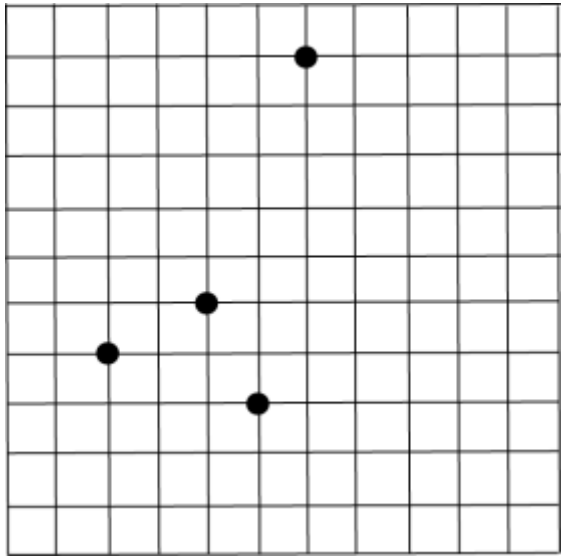
- Post-Placement Optimizations
  - Buffering, resizing, etc.

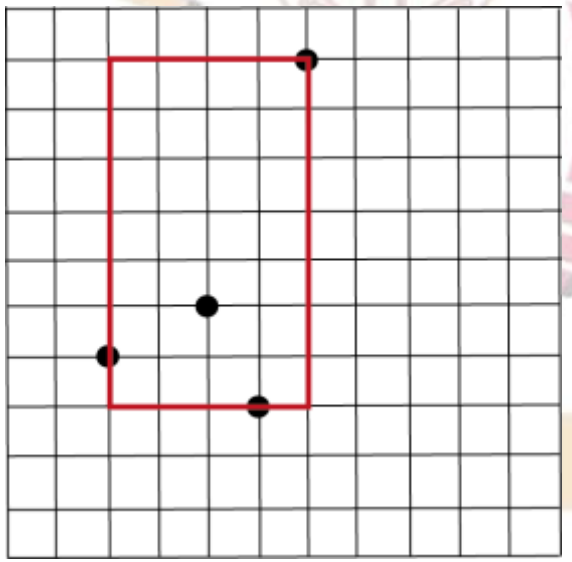
Placement: Wirelength Estimates

- Placer needs to compute the wirelength of each net multiple times
- Ideally, estimated wirelength should match post-routing wirelength

Half-perimeter Wirelength (HPWL)

- Easy to compute
- Half of the perimeter of the bounding rectangle that encloses all the pins of a net
- Widely used





Half-perimeter wirelength=11

Global Placement Techniques

- Well-studied problem: since 1970s
- Various heuristics have been proposed

Analytical Placement Algorithm:

- Considers each cell as point object with co-ordinates (x_i, y_i)
- Cost function (such as wirelength) and constraints are defined mathematically
  - Wirelength a function of $(x_i - x_j)^2 + (y_i - y_j)^2$

- Use efficient solvers to obtain minimum cost for the mathematical formulations
  - Suitable constraints of fixed entities
  - Cost related to cell density added
- Cells allowed to overlap in global placement
  - Legalization becomes necessary

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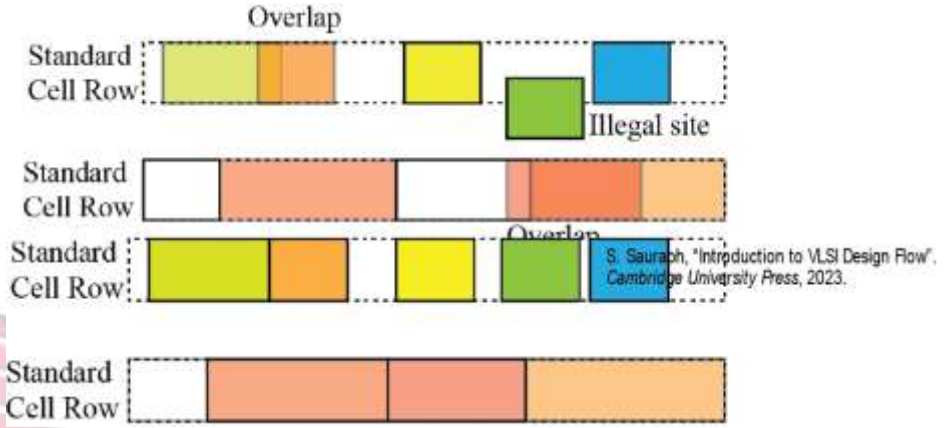
Placement: Legalization and Detailed Placement

A placement is illegal if:

- Cells overlap
- Cells occupy illegal sites (for example between placement rows)



Legalization:

- Removes all overlaps and snap cells to legal sites
  - With the minimum impact on the wirelength, timing and congestion

Detailed placement:

- Improves the QoR by incremental changes to the cell location(s)
- Improves wirelength and routability by:
  - Swapping location of neighboring cells
  - Re-distributing free sites
  - Moving cells to unused location

Timing-driven Placement

- Perform timing analysis internally and incrementally during placement
  - Target Worst Negative Slack (WNS) and Total Negative Slack (TNS)
- Control the proximity of cells that are on critical paths
- Depending on placement algorithm, different approaches to obtain timing driven placement is taken
- Additional weight is added to nets to indicate timing criticality
  - Give more weights to nets that are timing critical
  - Additional weights bias the placement engine to place timing critical objects together

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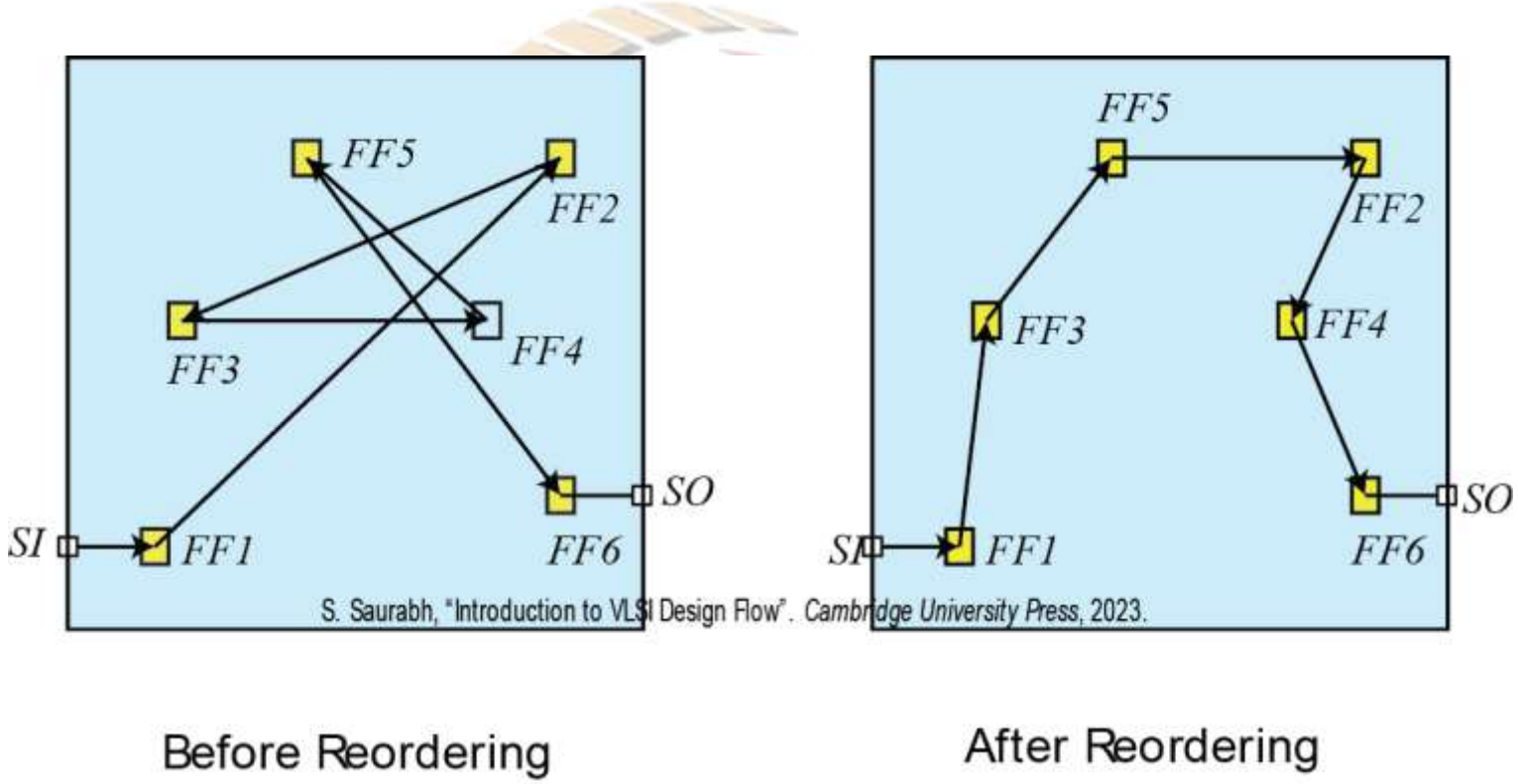
Scan Chain Reordering

- Scan cells that are nearby form consecutive flip-flops in the scan chain



Spare Cell Placement

Spare cells:

- Extra cells put in the circuit in anticipation of later use
- After fabrication, if it is required that some cells need to be connected, then spare cells can be used
  - ➢ Only the top metal layers might need to be changed

- Cannot be anticipated where will be the spare cells be actually be required to be connected
  - ➢ Place randomly over the unused placement area
- Tools must be informed that which are spare cells and should not be optimized out

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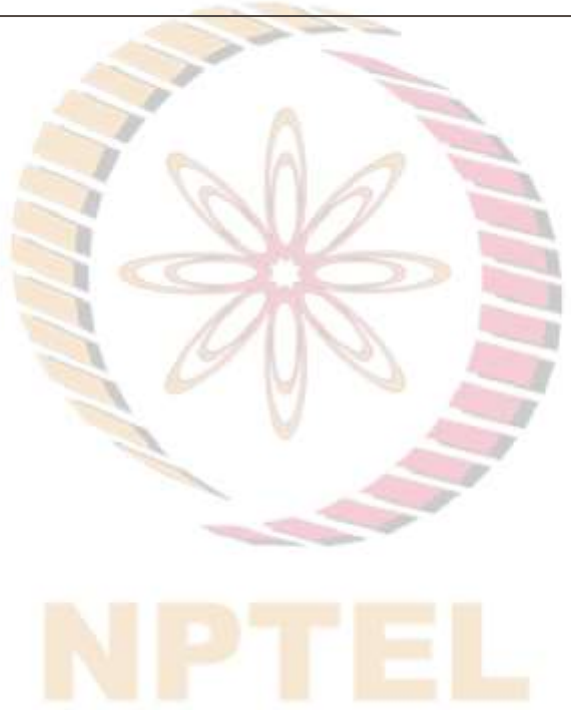
References

- S. Saurabh, “Introduction to VLSI Design Flow”. Cambridge: *Cambridge University Press*, 2023.



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