VLSI DESIGN FLOW: RTL TO GDS

Lecture 21
Technology Library

Sneh Saurabh
Electronics and Communications Engineering
IIIT Delhi

Lecture Plan

Till now....

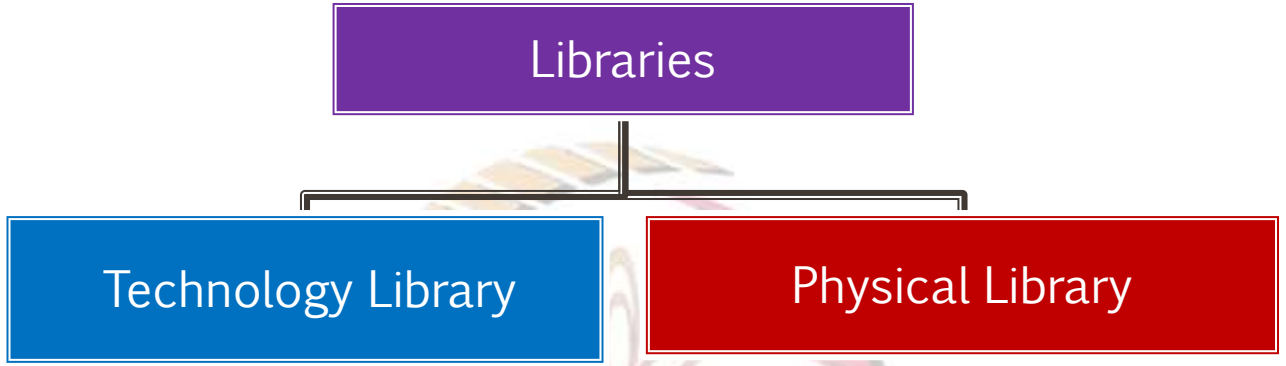
- Logic Synthesis:
  - Transformation of RTL to netlist of generic logic gate
  - Logic optimization

Subsequently ....

- Map generic logic gates to the cells of a given technology library
- Perform timing analysis and other types of verification

- Need information of the cells contained in a given technology library

Libraries in VLSI Design Flow



Technology Library:

- Introduced for logic synthesis
- Evolved to support various design tasks
  - Timing verification, physical implementation, and test activities
  - Also referred to as timing library.
- Liberty format
  - ASCII files (.lib extension)

Physical Library:

- Contains abstract information about the layout of the cells and technology.
- Library Exchange Format (LEF)
  - ASCII files (.lef extension)

Motivation for using Libraries

- Simplifies design task by decomposing the overall design process into two steps:
  - Creating Library
  - Using Library

Creating Library:

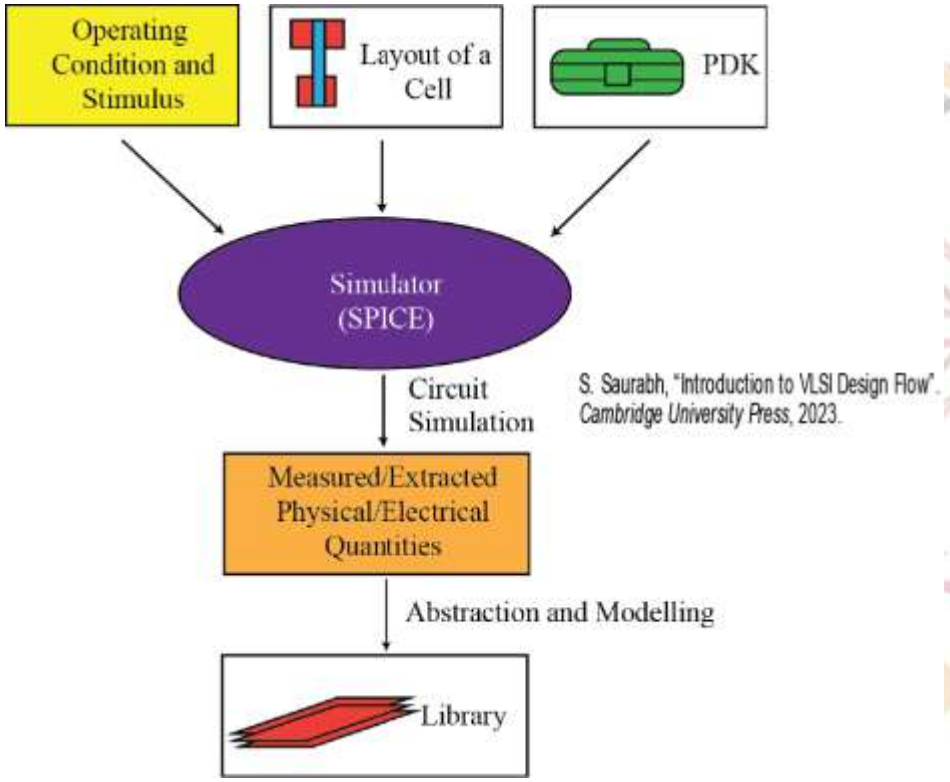
- Design each cell at the transistor level
  - Determine its optimal layout.
- Extract essential information about the cells and write them in the library.
- Many designs can employ the same library
  - Cost of developing a high-quality library gets distributed over multiple designs

Using Library:

- Instantiate cells from a library to achieve desired functionality
- Allows focusing on their instantiations
  - Design time and effort decrease.
  - Reduce the chances of errors within the cells.
- Raises the abstraction from the transistor level to the cell level
  - Makes complex synthesis, static timing analysis (STA), and physical design tasks feasible

Library : How are libraries created? (1)

Library Characterization: process of creating the library (at foundry or design house)



S. Saurabh, "Introduction to VLSI Design Flow", *Cambridge University Press*, 2023.

- Design each cell optimally and verify
- SPICE simulations of each cells for:
  - Given operating condition and stimulus
  - Transistor model, process (retrieved from PDKs)
- Measure/extract the parameters of interest such as delay, slew, voltage, capacitance, power, etc.
- Build an abstract model and write in the given format

Library Models

Why are SPICE simulations using PDKs not directly used for delay/power computation?

- SPICE simulations are time taking
  - Differential equations are formulated and typically solved using iterative techniques

Library models:

- Relevant information from SPICE simulation are extracted and modelled in the library
- EDA tools use library models instead of SPICE simulations for computing delay, slew, power, voltage variations, etc.
  - Order of magnitude faster than SPICE simulation and of reasonable accuracy

Requirement of library models:

- Speed and Accuracy
- Robustness
- Portability
- Variety and Uniformity:
  - Multiple cells for same function
  - Low Power, High Performance, High Density, Low-VT, High-VT
  - Height uniform, width variable

Library: Content

- Process parameters, Voltage, Temperature (collectively called PVT conditions)
- Cell data:
  - Pins, functionality
  - Timing, area and power information

- Libraries typically contains cells with hundreds of different logic functions:
  - Combinational/sequential standard cells
  - I/O Pads
  - Memories, macros

When do we use libraries?

- Libraries are used throughout RTL to GDS flow
  - Synthesis, timing and power analysis, verification, Design For Test (DFT), physical design

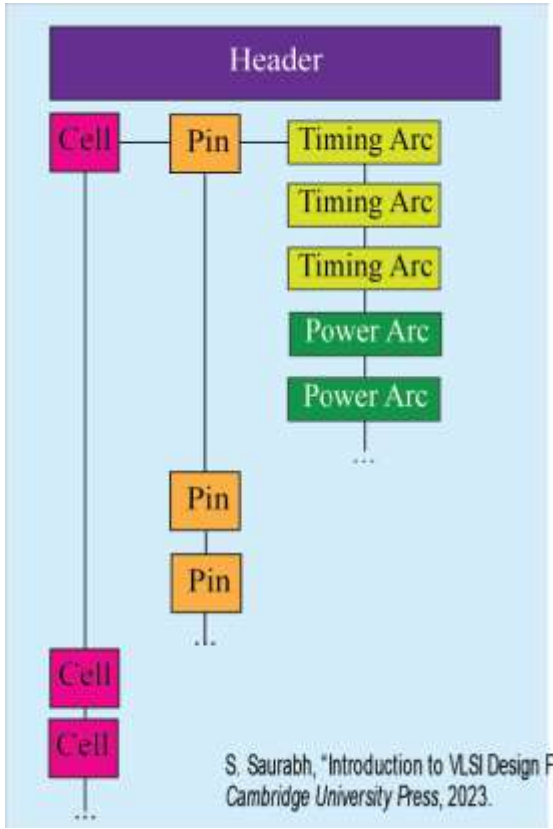
Library: Liberty format (1)

- Liberty format is simple ASCII/text format

- Data is primarily stored as attributes
  - Mapping between an attribute name and its value
  - Example: time_unit : “10ps”;

- Information is organized as a hierarchy of groups

- At the top level it has a Header
- Header contains:
  - PVT conditions, scaling factors, units
  - Information that are valid for all the cells/pins/arcs
  - List of cells

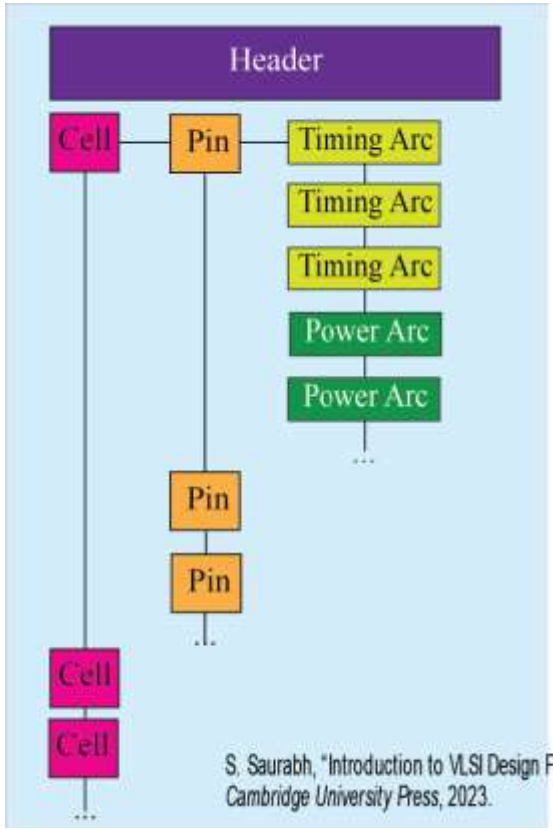


Library: Liberty format (2)

- Cell contains:
  - Area
  - Cell Leakage Power
  - List of pins

- Pin contains:
  - Direction
  - Capacitance
  - Functionality (for output pins)
  - List of timing arcs
  - List of power arcs

- Timing arcs are used to perform timing analysis or computing delays of the arcs
- Power arcs are used to perform power analysis



Technology Library

Modelling Delay

Library : Timing Arcs

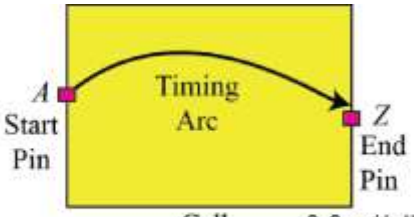
- Timing Arcs are used to model timing attributes for combinational or sequential cells in a library

Each Timing Arc has:

- Start Pin and End Pin
- Timing arc is specified on the End Pin
- Start Pin is specified using the attribute **related_pin**

Timing Arcs can be of type:

- Delay Arc
- Constraints Arc (setup check, hold check etc.)



S. Saurabh, "Introduction to VLSI Design Flow", *Cambridge University Press*, 2023.

```
pin(Z) {
    direction           : output ;
    ...
    timing() {
        related_pin     : "A" ;
    }
    ...
}
```

Slew Definition

- Slew of a signal quantifies how steeply or sharply transition occurs from “0” → “1” or “1” → “0”

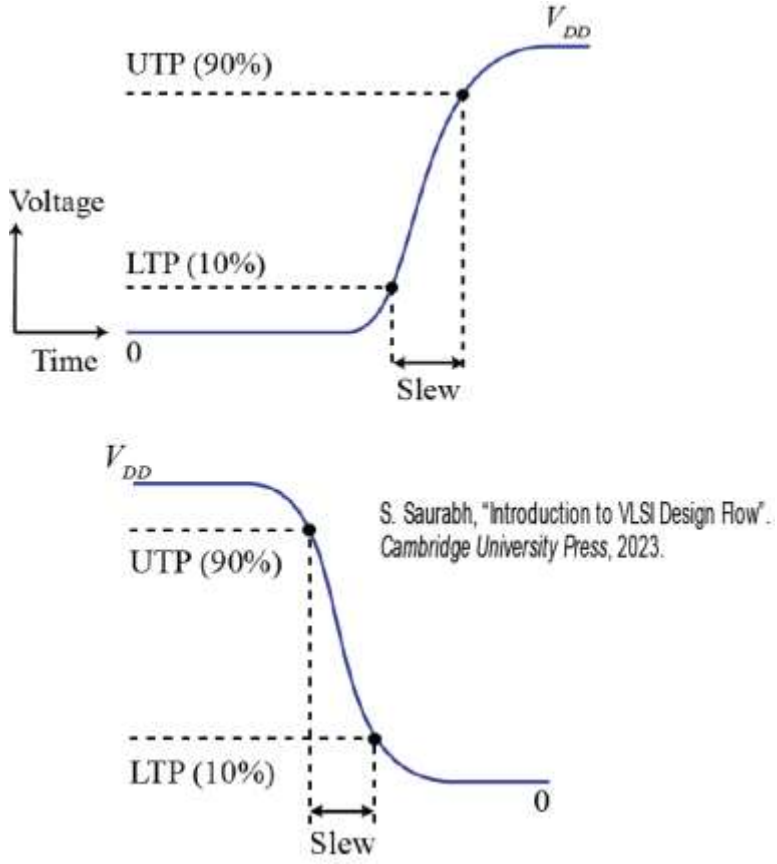
Slew measured by defining two transition points:

- Lower threshold percentage (LTP)
- Upper threshold percentage (UTP)

10-90 Threshold:

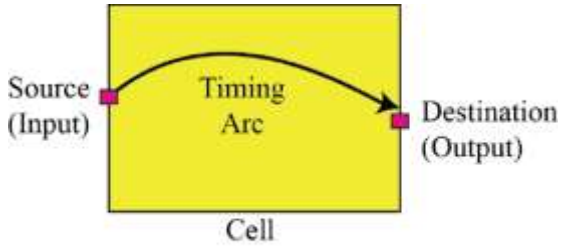
- **Rise slew:** time taken for a signal to reach from 10% to 90% of supply voltage
- **Fall slew:** time taken for a signal to reach from 90% to 10% of supply voltage

- Slew threshold of 20-80, 30-70 can also be used
- Also called: **rise transition time, fall transition time, rise time, fall time**



Delay Definition

- Quantifies how much time it takes for the change in input to propagate to the output



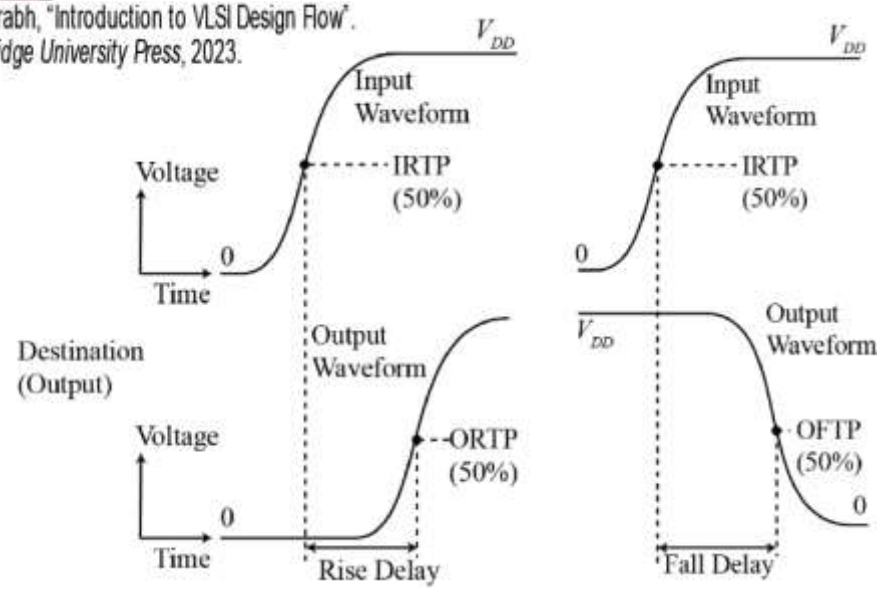
S. Saurabh, "Introduction to VLSI Design Flow".
Cambridge University Press, 2023.

Delay can depend on the direction of transition (rising/falling)

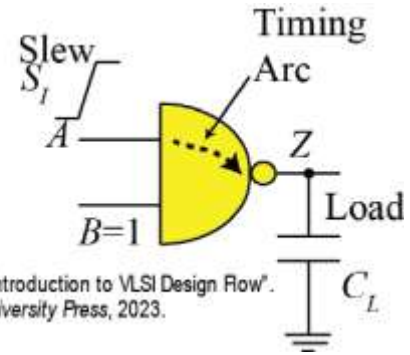
- Rise delay: output rising
- Fall delay: output falling

- Predefined threshold points on the input waveform and the output waveform.
- For the input signal:
  - input rise threshold percentage (IRTP)
  - input fall threshold percentage (IFTP).
- For the output signal:
  - output rise threshold percentage (ORTP)
  - output fall threshold percentage (OFTP)

S. Saurabh, "Introduction to VLSI Design Flow".
Cambridge University Press, 2023.



CMOS : Characteristics of Slew and Delay



S. Saurabh, "Introduction to VLSI Design Flow". *Cambridge University Press*, 2023.

- In general, the **delay** (D) and **output slew** (S_{OUT}) of a given **timing arc** depend on:
  - Input Slew (S_{IN})
  - Output Load (C_L)

- The relationship may be non-linear:
  - $D = f(S_{IN}, C_L)$
  - $S_{OUT} = g(S_{IN}, C_L)$
  - f, g are non-linear function (typically monotonically increasing with S_{IN} and C_L)

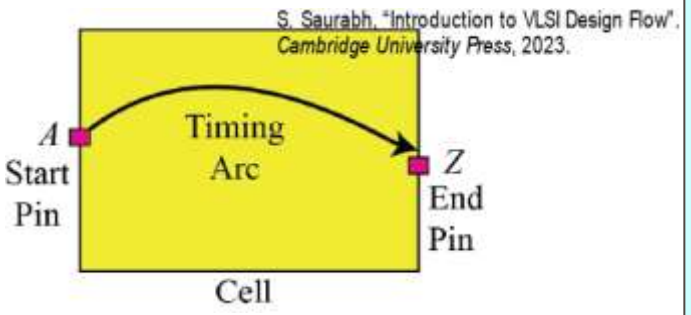
- Modelled approximately as two dimensional discrete point tables

$T(i,j)$	$C_{L,1}$	$C_{L,2}$			$C_{L,N}$
$S_{I,1}$					
$S_{I,2}$					
$S_{I,M}$					

S. Saurabh, "Introduction to VLSI Design Flow". *Cambridge University Press*, 2023.

- Intermediate values are *interpolated* from closest match
- Different tables for delay and output-slew

Non-linear Delay Model (NLDM)




```
u_table_template(index_1) {
        variable_1 : input_net_transition ;
        variable_2 : total_output_net_capacitance ;
        index_1( "10, 20, 30" ) ;
        index_2( "1.2, 5.0,15.0, 37.5) ;
}
....
pin(Z) {

        timing()   {
                related_pin          : “A" ;
                timing_sense       : positive_unate ;
                cell_rise(index_1) {
                        values( "   4, 5, 7, 12,   ...3x4 table);
                }
                ...
        }
}
```

S. Saurabh, “Introduction to VLSI Design Flow”.*Cambridge University Press*, 2023.

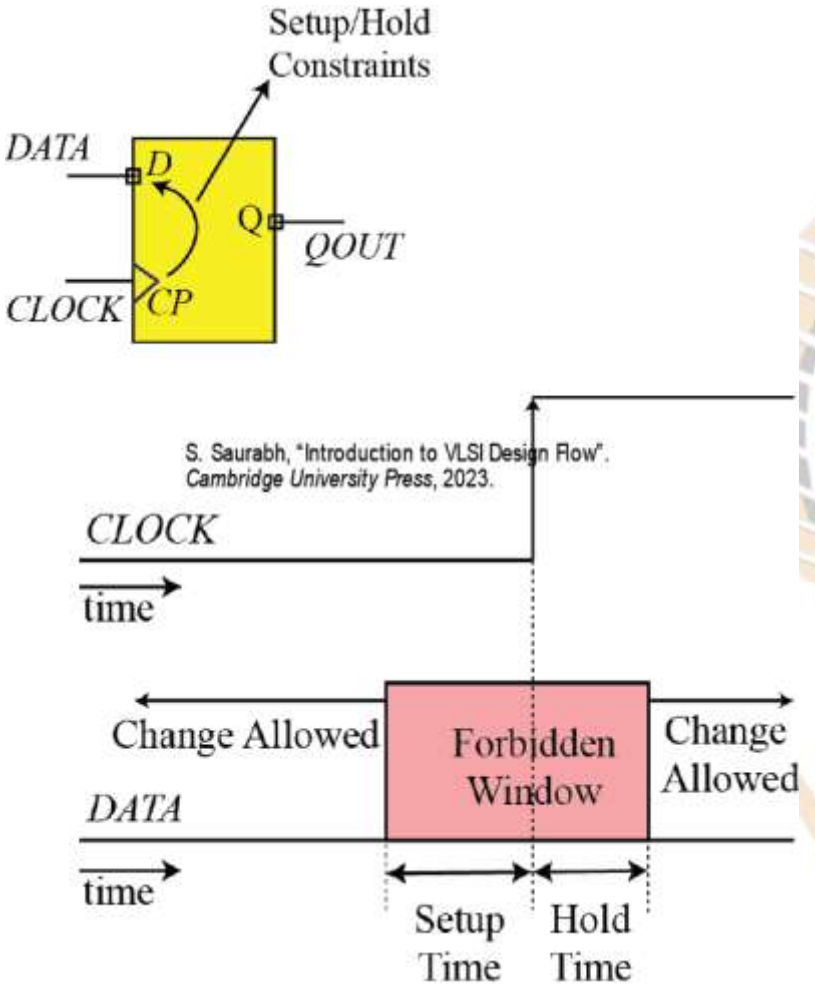
Library : Advanced Delay Model

- At advanced process nodes simple NLDM model is not accurate
- Other delay models based on current source model are employed
  - Composite Current Source (CCS)
  - Effective Current Source Model (ECSM)

Technology Library

Modelling Setup/Hold

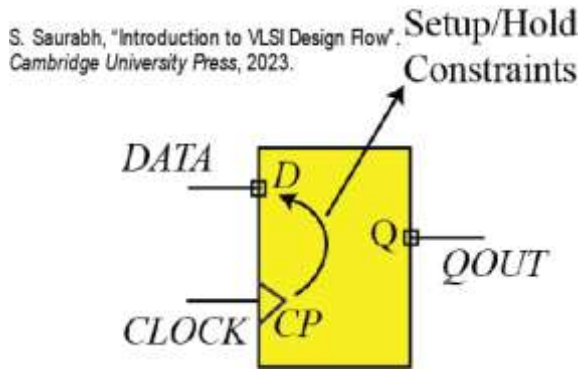
Setup/Hold Time : Definition



- **Setup time**: minimum amount of time the DATA signal should be held steady **before the CLOCK edge** so that the DATA is sampled correctly and deterministically

- **Hold time**: the minimum amount of time the DATA signal should be held steady **after the CLOCK edge** so that the DATA is sampled correctly and deterministically

CMOS : Setup/Hold Characteristics

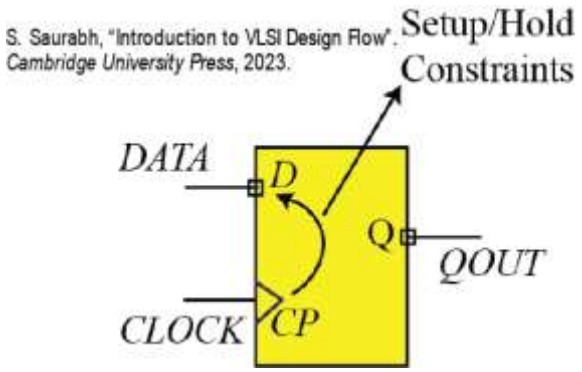


- In general, the **setup** (SU) and **hold** (H) constraints depend on:
  - Data Slew (S_D)
  - Clock Slew (S_{CLK})

- The relationship may be non-linear:
  - $SU = f(S_D, S_{CLK})$
  - $H = g(S_D, S_{CLK})$
  - f, g are non-linear functions

- Modelled as two dimensional discrete point tables
- There are different tables for setup and hold

Library : Modelling Setup/Hold Constraints



- Intermediate values are interpolated from closest match

```
u_table_template(index_1) {
        variable_1 : constrained_pin_transition;;
        variable_2 : related_pin_transition;
        index_1( "10, 20, 30" ) ;
        index_2( "10, 20, 30, 40) ;
}
....
pin(D) {

        timing()   {
                   related_pin          : “CP" ;
                   timing_type : "setup_rising";
                   rise_constraint(index_1) {
                            values( "   4, 5, 7, 12,
...3x4 table);
                   }
                   ...
        }
}
```

S. Saurabh, “Introduction to VLSI Design Flow”.*Cambridge University Press*, 2023.

Library : Other information contained in library

- Power Models
- Models for crosstalk noise analysis
- Power/Ground Pin Information
- State dependent arcs: *sdf_cond*, *when*
- Other attributes that may be vendor specific

References

- Synopsys Inc. “Liberty.” https://www.synopsys.com/community/interoperability-programs/tap-in.html.
- S. Saurabh, “Introduction to VLSI Design Flow”. Cambridge: *Cambridge University Press*, 2023.
- Bhasker, Jayaram, and Rakesh Chadha. *Static timing analysis for nanometer designs: A practical approach*. Springer Science & Business Media, 2009.