VLSI DESIGN FLOW: RTL TO GDS

Lecture 37
Chip Planning - I

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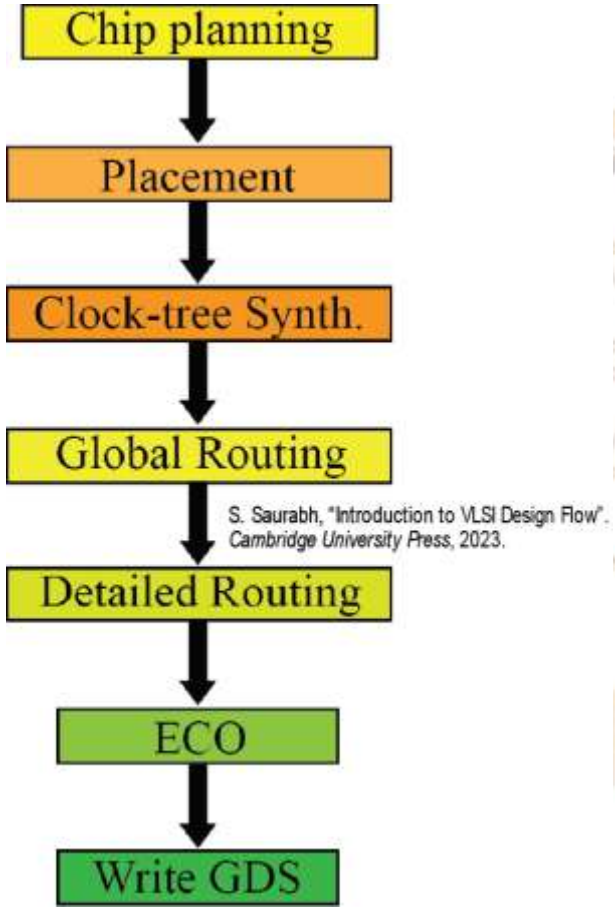
Lecture Plan



S. Saurabh, "Introduction to VLSI Design Flow", *Cambridge University Press*, 2023.

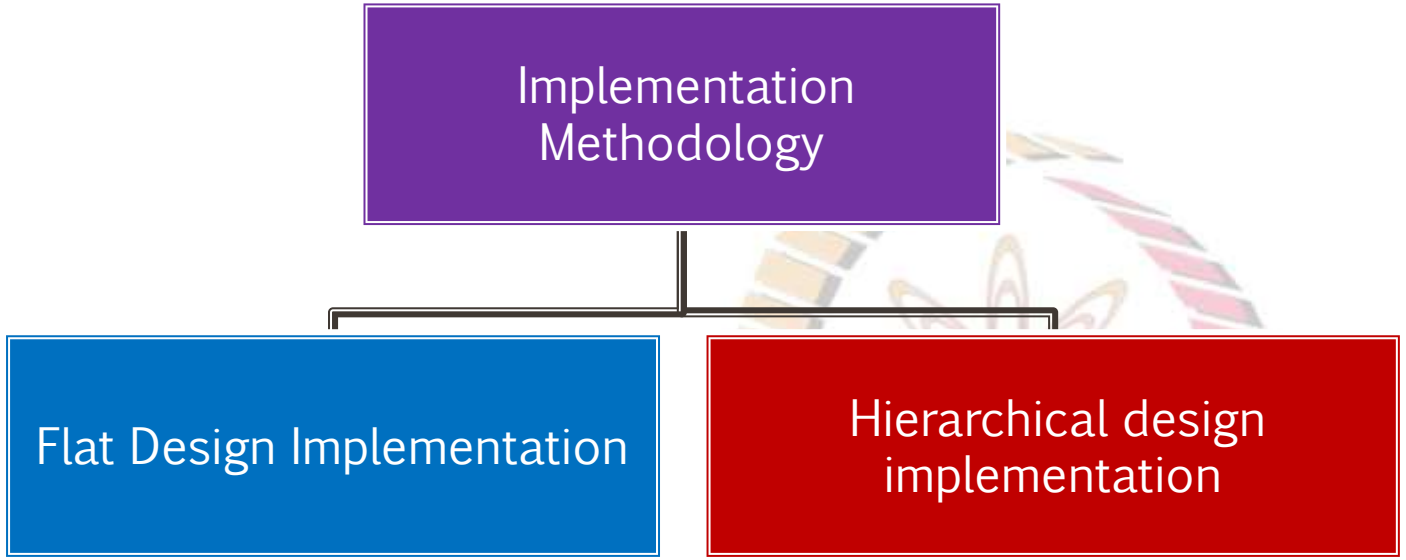
- Chip Planning
  - Hierarchical Design Implementation
  - Floorplanning
  - Power Planning

Laying plans …

"…While times are quiet, it is easy to take action; ere (before) coming troubles have cast their shadows, it is easy to lay plans…. A journey of a thousand miles began with a single step."

—Lao Tzu (ancient Taoist philosopher)

Implementation Methodology



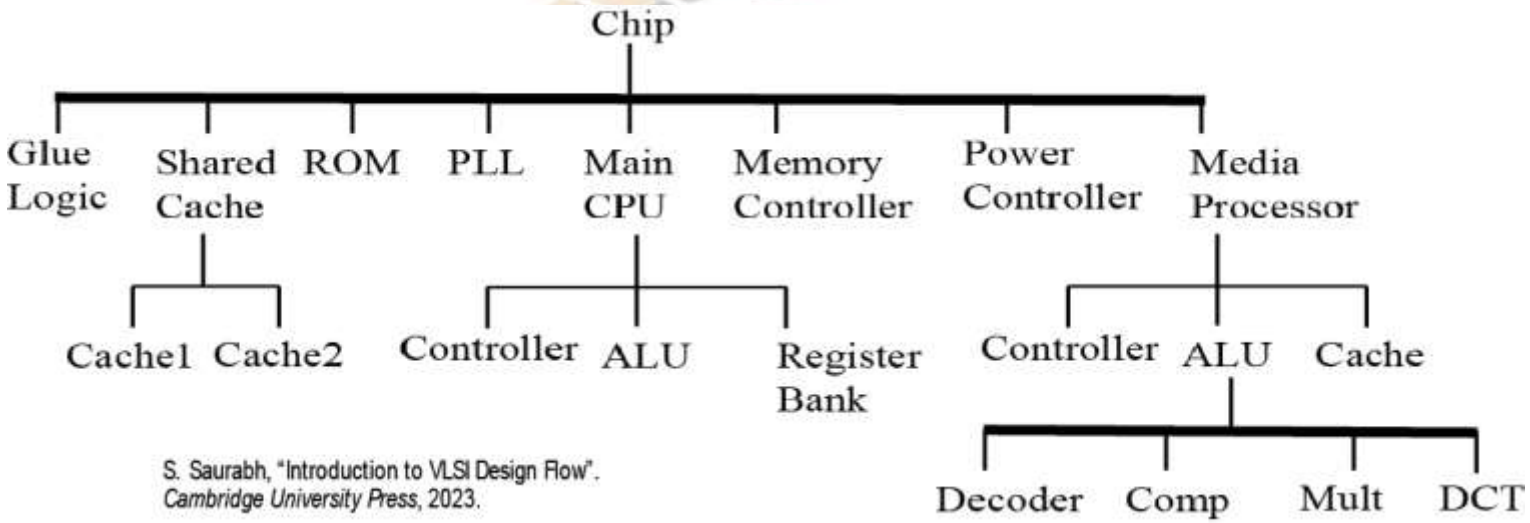
Tasks in hierarchical design implementation

1. Partitioning
2. Budgeting
3. Block Implementation
4. Top-level Assembly

Partitioning

How to partition?
- Partition using logical functionality

- Partitions are called *blocks*



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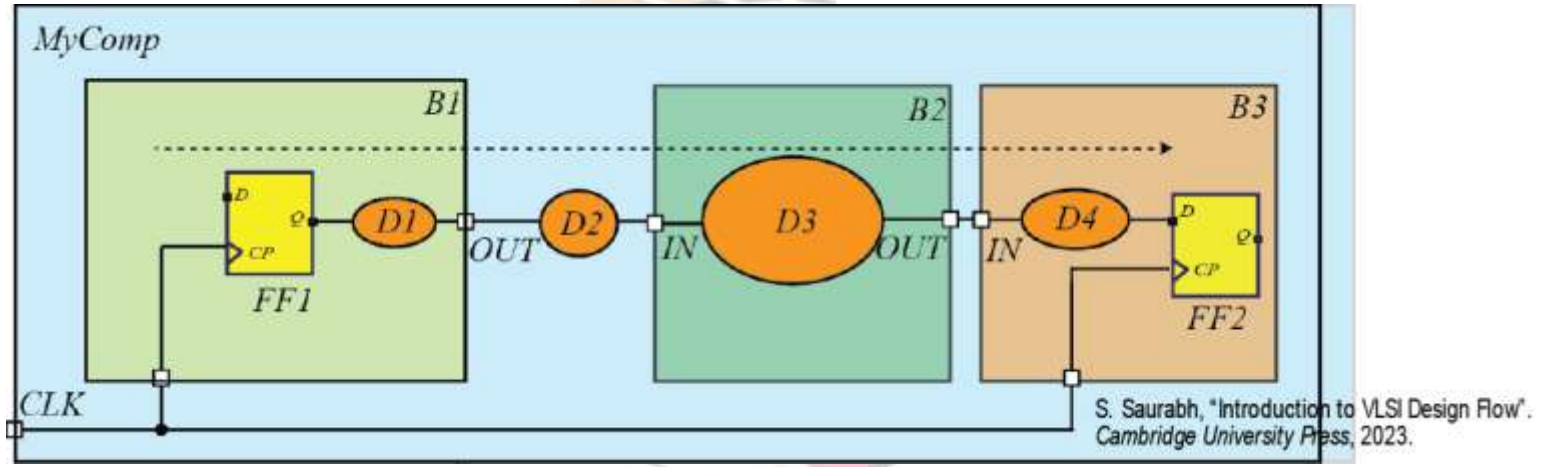
Other approaches:
- Group modules into clusters
- Partition a netlist using partitioning algorithm
  - ➢ Reduce the number of cuts or nets crossing blocks

Budgeting

- Process of allocating some fraction of a clock cycle to different blocks and the top-level design for signals crossing block boundaries



- Create block level SDC

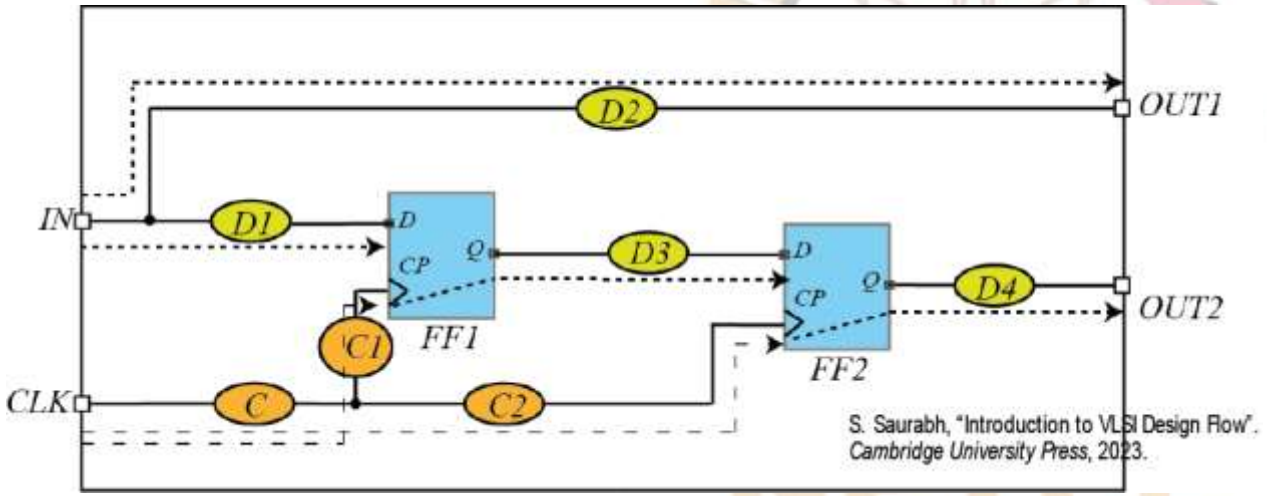
Block Implementation and Top-level Assembly

Block Implementation

- Implement each block separately
- Use allocated timing budgets and block constraints (verify at block level)

Top-level Assembly

- Integrate all the blocks at the top-level
- Carry out verification at the top-level
- Omit details of the timing paths contained entirely within a block



Abstract Timing Model of Blocks:

- Retain information of interface timing paths of the blocks
- Extracted Timing Model (ETM)
- Interface Library Model (ILM)

Hierarchical Design Methodology: Merits and Challenges

Advantages:

- Physical implementation and other EDA tools need to handle smaller problems
- Multiple blocks can be concurrently implemented by different teams
  - ➢ Overall design time decreases

Disadvantages:

- Challenging to partition a design optimally
- Loose some opportunities of inter-block optimizations

Floorplanning

Floorplanning: Basics

- Planning phase of the layout
  - ➢ Designer's intent about physical design
- Prepares a design for other physical design tasks
  - ➢ Huge impact on the final FoM
- Must consider routability, performance, power, etc.

Major Tasks:

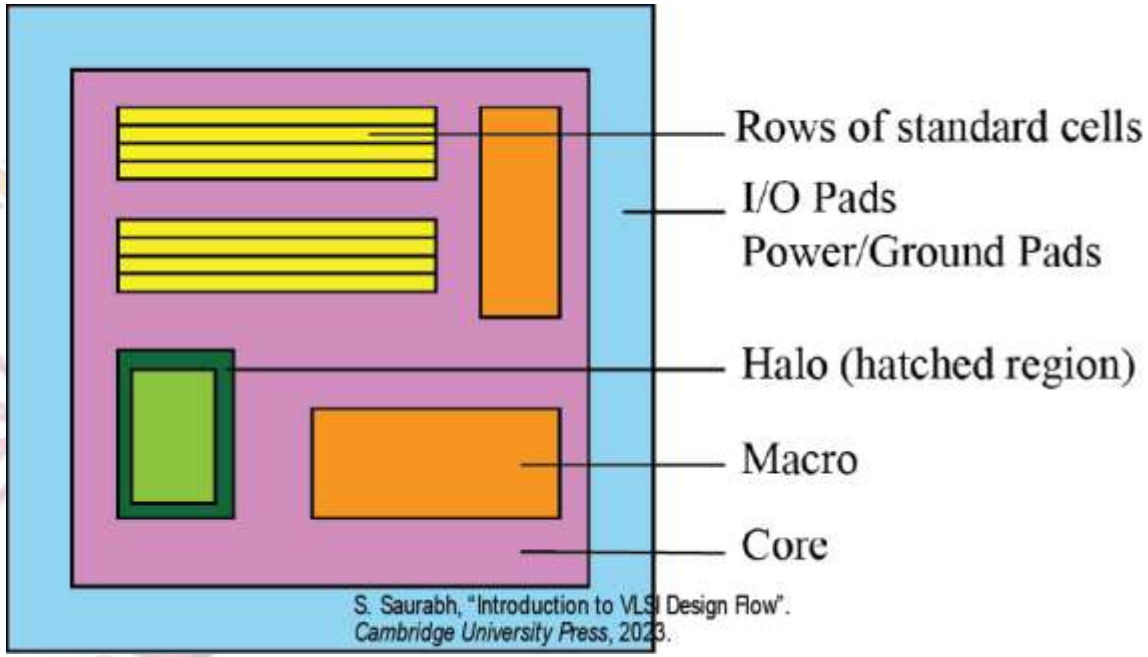
1. Define die/chip size and aspect ratio
2. I/O cell placement
3. Hard macros/block placement
4. Pin assignment
5. Create rows for standard cells

Die Size

Goal: choose smallest size of die that can fit the design

Die area should include area for:

- IO Cells/IO Pads
- Standard Cells
- Macros + Halo
- Interconnects (utilization)



$$Utilization = \frac{Cell\ area + Macro\ area + Halo\ area}{Core\ area}$$

Rough Estimate based on:

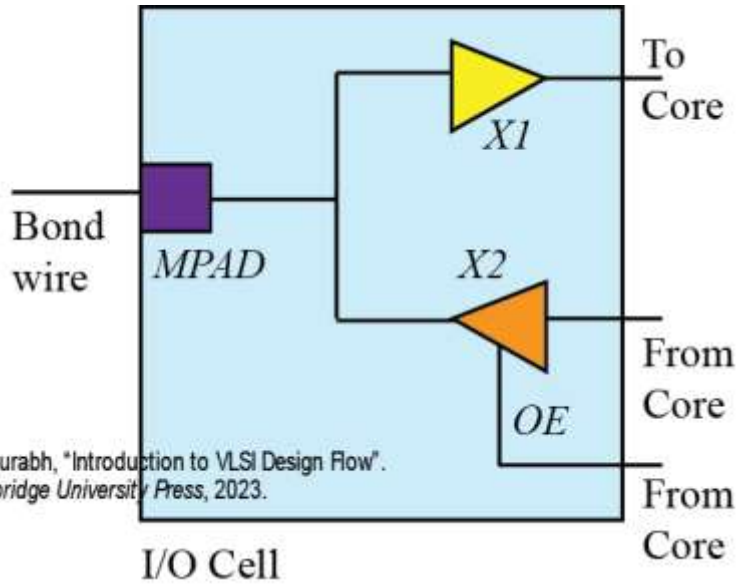
- Previous designs
- Available package size

IO Cells: Basics

- IO cells are special circuit elements through which a chip communicates with the external world
- Can be of type input, output, or bidirectional

Other functions of IO cells

- Drive capability
- Voltage transformation
- Protection against ESD (Electro-Static Discharge) [short high-voltage (several kilovolt) pulses]



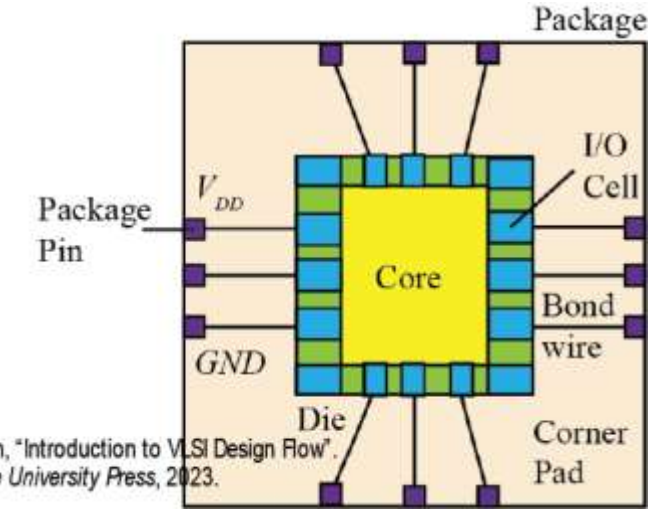
I/O Cell

IO Cells: Connection with Package

- Metallic pad (MPAD) is connected to the package pins using bonding wires

- Power pads: special cells that supply power to a chip
- IO Cells too need power and ground connections

Number of power pads:
- Target level of internal voltages
- Current capacity of the power pads



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Placement of IO Cells are guided by heuristics
- Assign nearby positions to two primary inputs that jointly drive a multi-input logic gate
- Spread power-hungry I/O cells all over the die area to avoid creating voltage drop hotspots
- Avoid placing sensitive (such as clock signals) near IO cells

- Flip-chip technology offers more flexibility in placing macro cells.

References

- S. Saurabh, “Introduction to VLSI Design Flow”. Cambridge: *Cambridge University Press*, 2023.