VLSI DESIGN FLOW: RTL TO GDS

Lecture 42
Post-Layout Verification and Signoff

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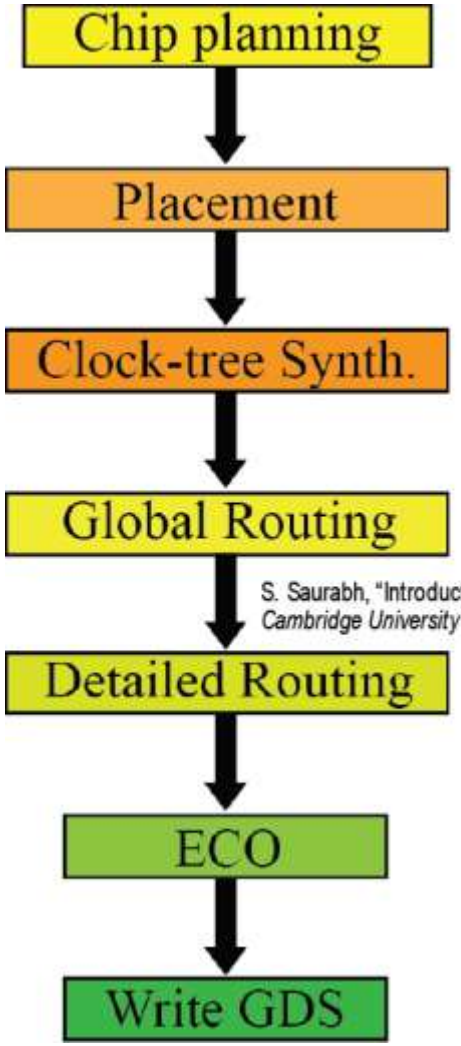
Lecture Plan



S. Saurabh, "Introduction to VLSI Design Flow". *Cambridge University Press*, 2023.

Post-layout Verification

- Layout Extraction
- Physical Verification
- ECO and Signoff

Layout Extraction

Layout Extraction: Basics

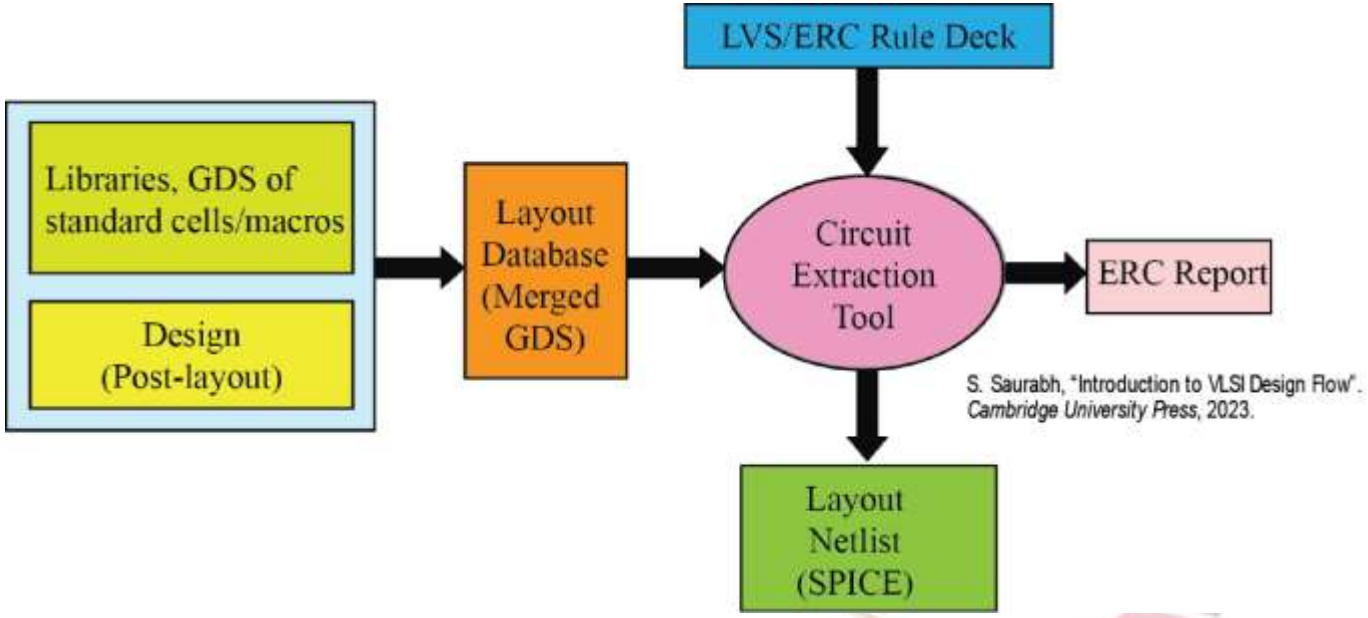
- Layout describes the shapes required on each fabricated layer
  - ➢ Difficult for other post-layout verification tools to work with this information

- Extract various information from the layout
  - ➢ Problem for a verification tool is greatly simplified

Layout extraction consists of two major tasks:

1. **Circuit Extraction:** devices and interconnections
2. **Parasitic Extraction:** parasitic resistance, capacitance and inductance

Circuit Extraction



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Inputs:

- Merged GDS: layout of the design and standard cells/macros
- Extraction rules: for devices and connections (comes from foundry)

Outputs:

- Layout Netlist: typically in SPICE
- ERC Report

Parasitic Extraction

- **Resistance**: each net may be divided into multiple net segments
- **Capacitance:** need to account for various components

Technology pre-characterization

- Performed once for a given technology
- Enumerate millions of sample geometries/structures
- Use accurate Field Solvers for computation
  - ➢ Values stored in lookup tables or empirical formulae created using curve-fitting
- Highly time consuming

Chip-level parasitic extraction:

1. Technology pre-characterization
2. Pattern Matching

Pattern Matching

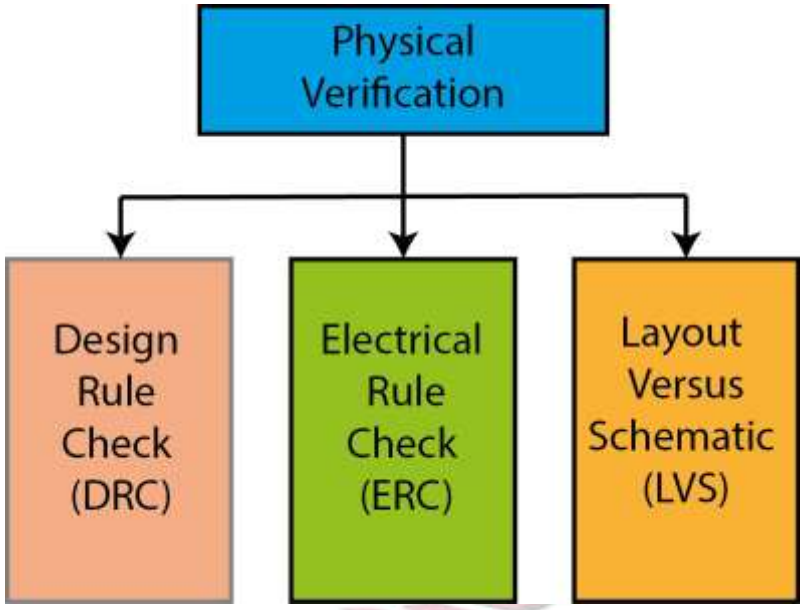
- Partition a layout into smaller windows
- Match windows with pre-characterized patterns
- Compute the capacitance with the help of lookup tables or empirical formulae
  - ➢ Actual geometries of the layout used

Inductance:

- More challenging to extract
- Fortunately, can ignore for most nets
- Numerical techniques used

Physical Verification

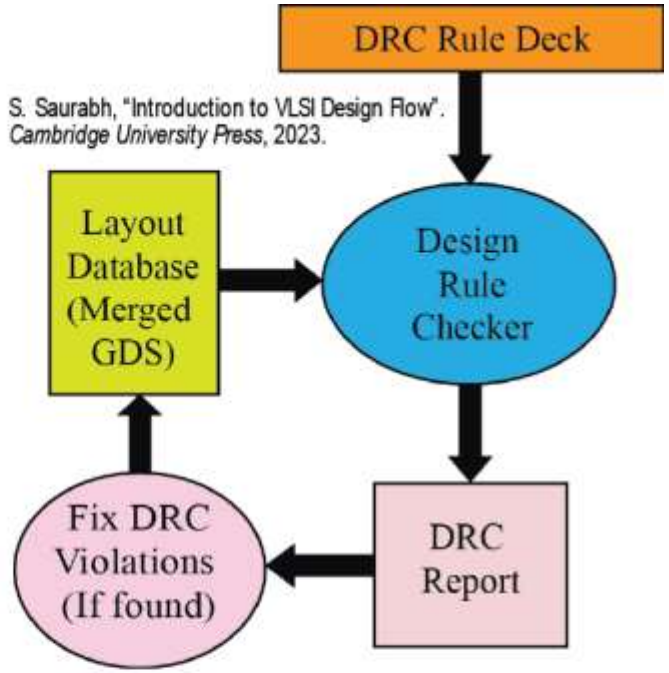
Physical Verification

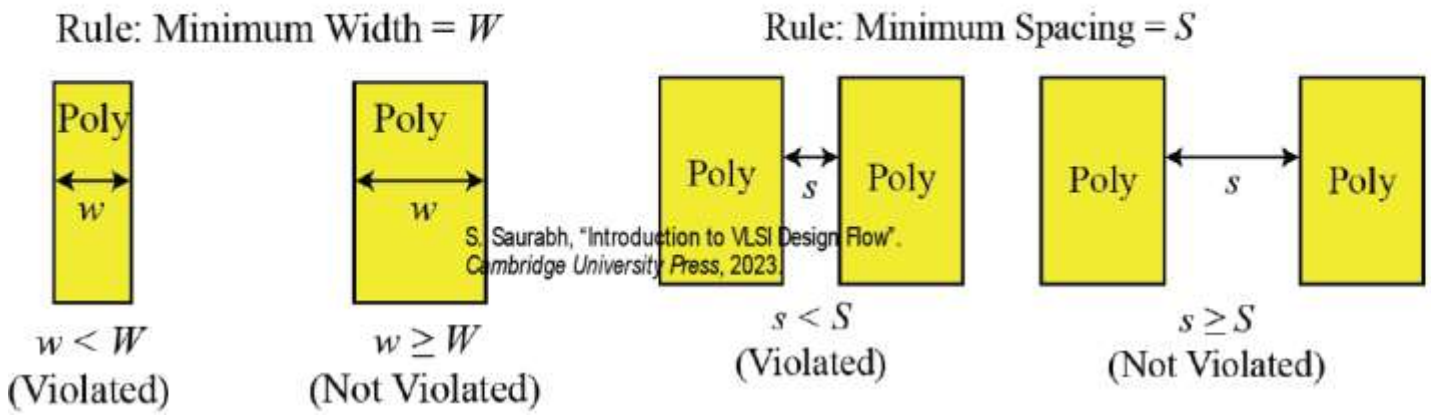


Physical Verification : DRC

Design Rule Check (DRC):

- Ensure that the layout meets the constraints required for manufacturing
- Rules are defined by the respective foundry
  - ➢ Achieve a good yield and improve reliability
  - ➢ Vary with the technology
  - ➢ Become more complicated with advancement in technologies

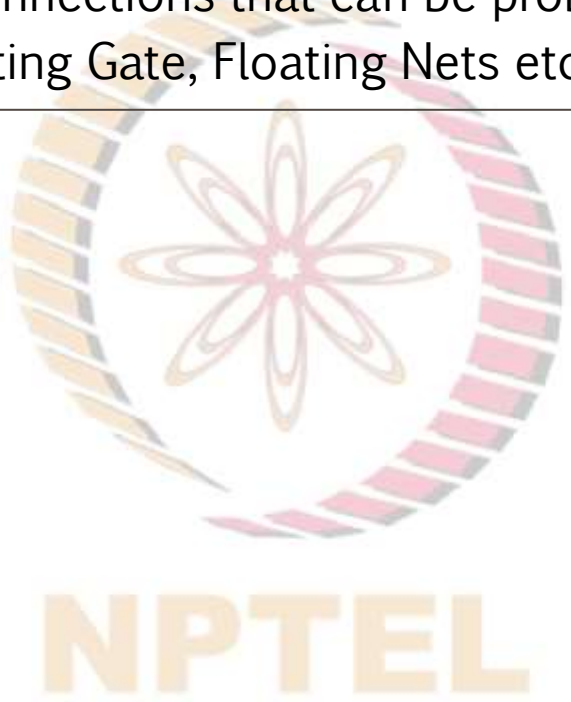




Physical Verification : ERC

Electrical Rule Check (ERC):

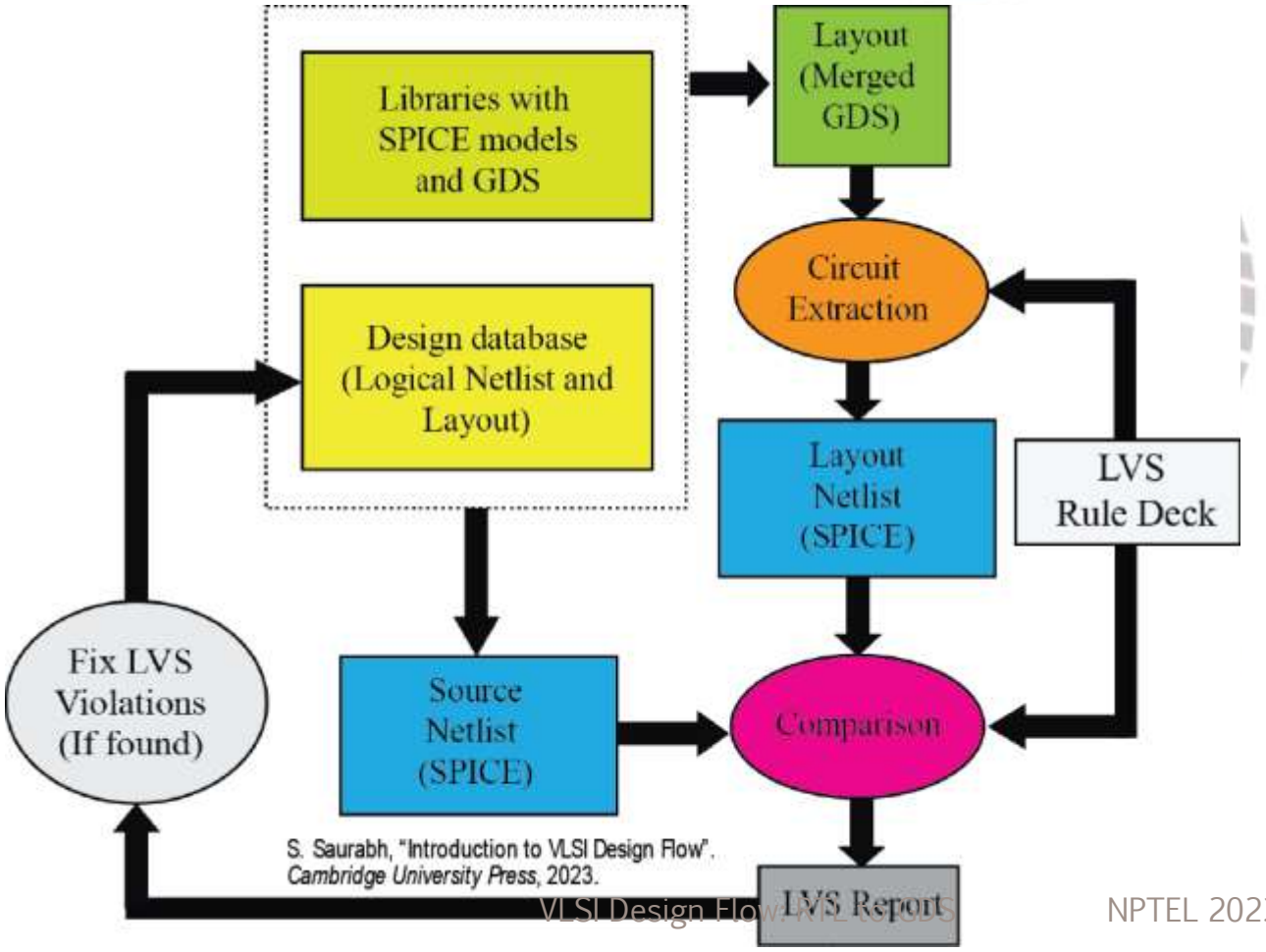
- Check design for electrical connections that can be problematic
- Examples: Shorts/Open, Floating Gate, Floating Nets etc.



Physical Verification : LVS

Layout versus Schematic (LVS):

- Verifies whether the layout corresponds to the original schematic (netlist) of the design



Compares:

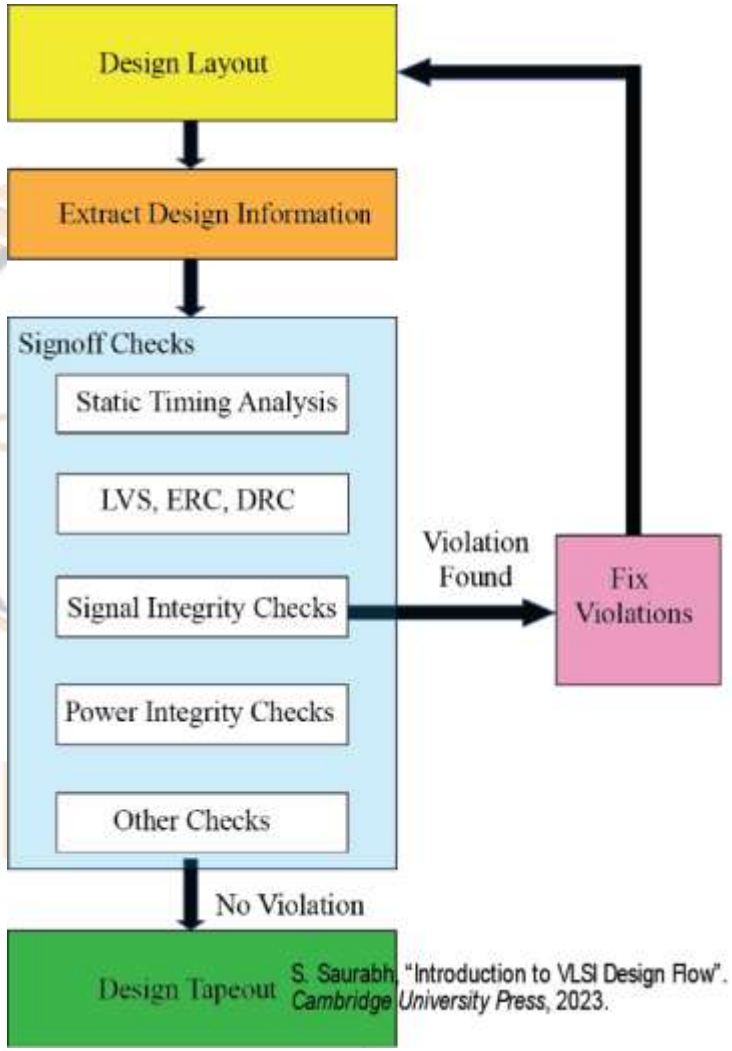
1. Layout netlist (extracted)
2. Source netlist (schematic): logical netlist combined with device information

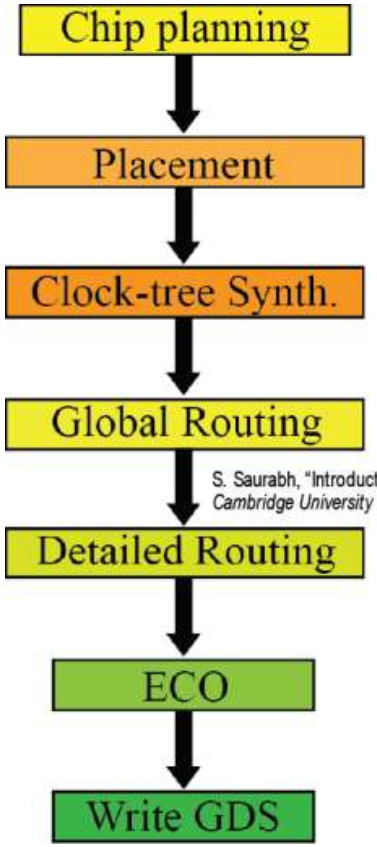
Signoff

Signoff

Signoff:

- Series of verification steps that must be carried out before sending the layout (GDS) to a foundry
- Ensures that the layout delivers the intended functionality and meets various figures of merit





Engineering Change Order (ECO)

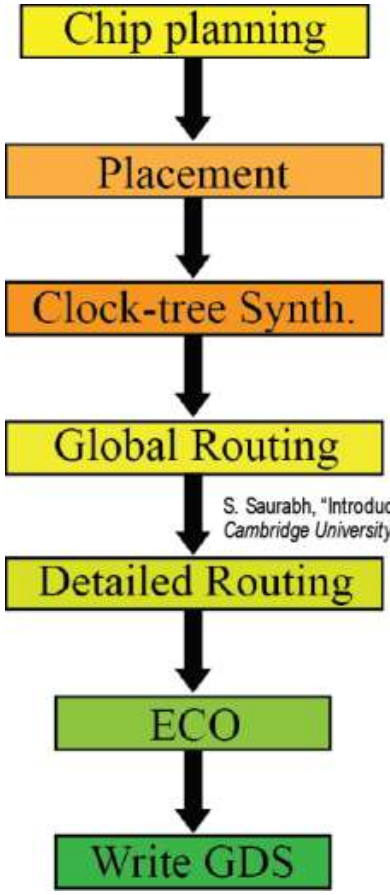
- Sometimes last moment incremental changes in a design needed
  - ➢ Fix issues discovered late or new incremental functionality
- Risky changes
  - ➢ Incorporate them using Engineering Change Order (ECO)

ECO tools:

- Enable making targeted incremental changes, rather than re-implementing the entire design
- Verify the correctness of the ECO changes.
  - ➢ Saves designer time, effort, cost, and risk

Types of ECO changes

- Functional ECO: changes logic
  - ➢ Logic re-synthesis or use spare cells
- Direct changes in layout to fix setup/hold time violations, SI-related issues, and design rule violations.



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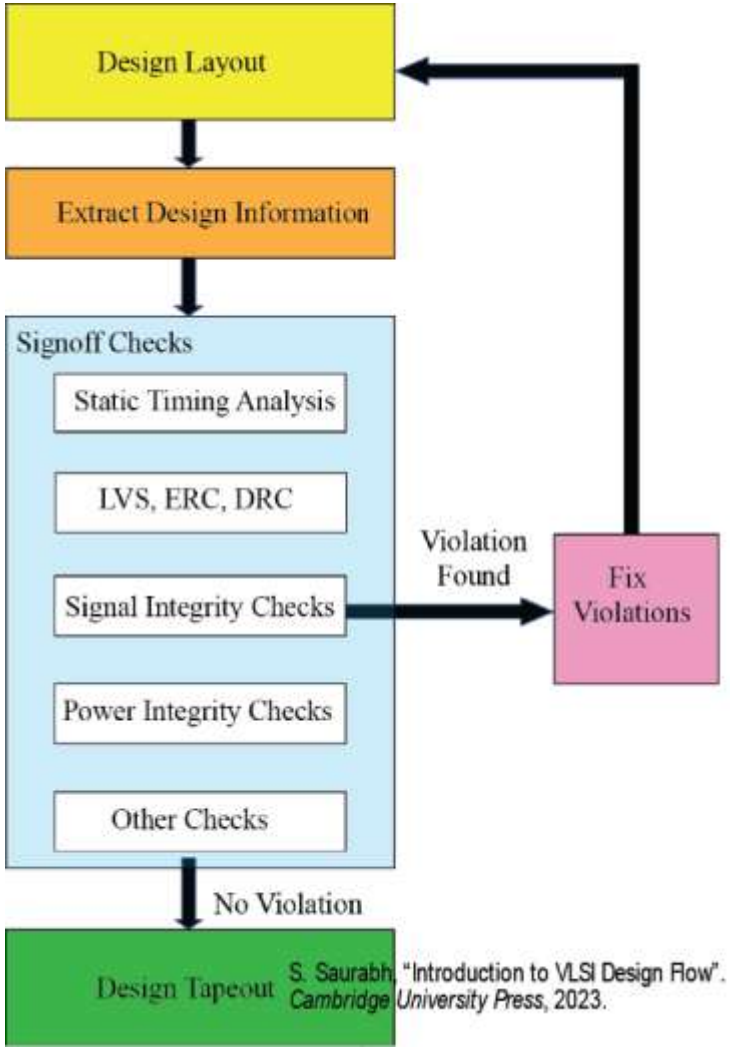
Signoff and Tapeout



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- Design Tapeout: send the GDS for fabrication
- Occasion to celebrate !

References

- S. Saurabh, “Introduction to VLSI Design Flow”. Cambridge: *Cambridge University Press*, 2023.