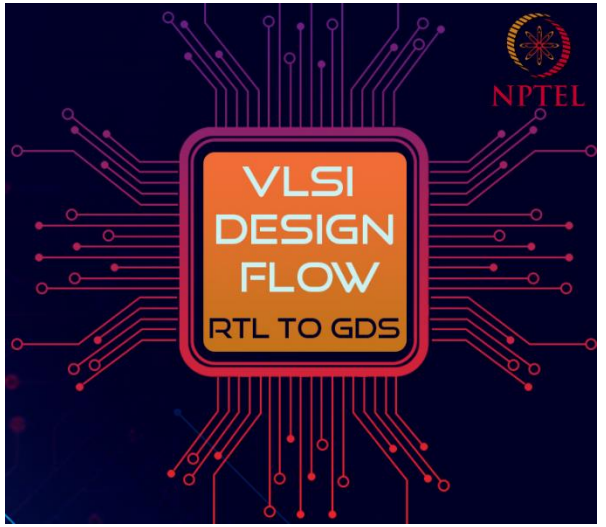
VLSI DESIGN FLOW: RTL TO GDS

Lecture 27
Technology Mapping



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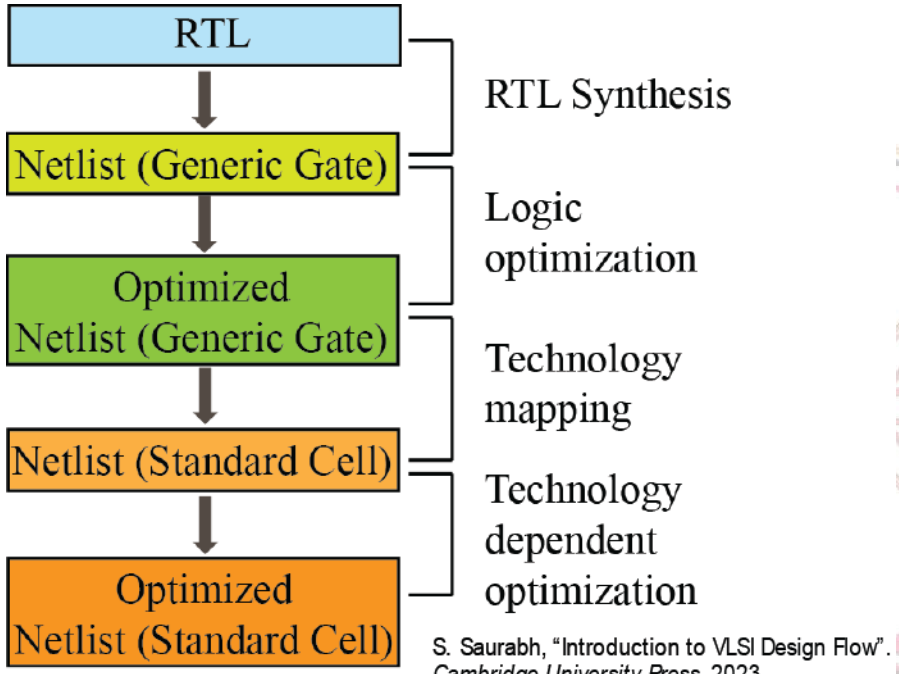
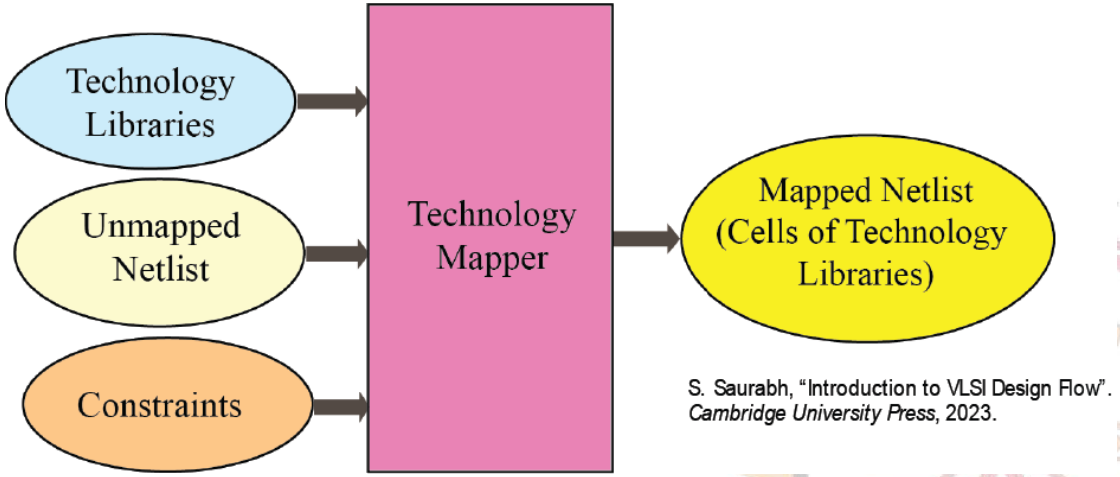
Lecture Plan



S. Saurabh, "Introduction to VLSI Design Flow". *Cambridge University Press*, 2023.

- Technology Mapping

Technology Mapping: Framework



S. Saurabh, "Introduction to VLSI Design Flow". *Cambridge University Press*, 2023.

Technology Libraries

- Cells with different logic functions
- Cells with same function, but of different sizes

Unmapped Netlist:

- Netlist of generic logic gates

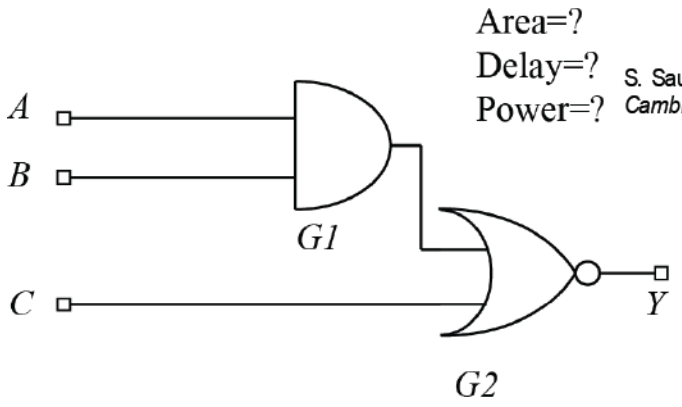
Constraints:

- Synopsys Design Constraint (SDC) file
- Objectives:
  - Minimize area under a given delay constraint
  - Minimize delay under a given area constraint

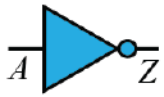
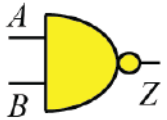
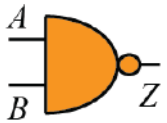
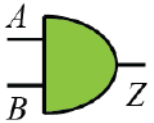
Mapped Netlist:

- Netlist consisting of library cells
- Functionally equivalent to unmapped netlist

Illustration of Mapping: Given Problem



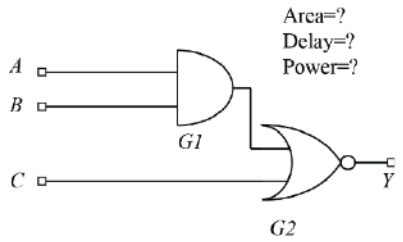
S. Saurabh, "Introduction to VLSI Design Flow". *Cambridge University Press*, 2023.

Cell Name	Symbol	Function	Area	Delay	Power
INV1		*Z=A'*	1	4	5
NAND1		*Z=(A.B)'*	4	8	20
NAND1_LP		*Z=(A.B)'*	5	12	6
AND1		*Z=A.B*	8	9	30

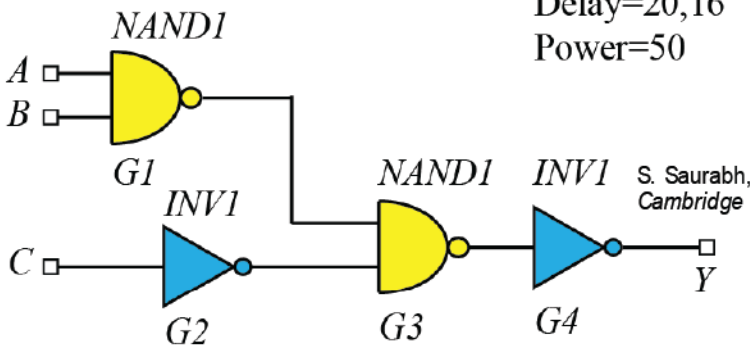
Logic Function:

- $Y = (A.B + C)'$

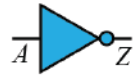
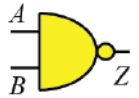
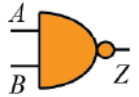
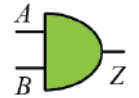
Illustration of Mapping: Solution 1



Given: $Y = (A.B + C)'$



Area=10
Delay=20,16
Power=50

Cell Name	Symbol	Function	Area	Delay	Power
INV1		*Z=A'*	1	4	5
NAND1		*Z=(A.B)'*	4	8	20
NAND1_LP		*Z=(A.B)'*	5	12	6
AND1		*Z=A.B*	8	9	30

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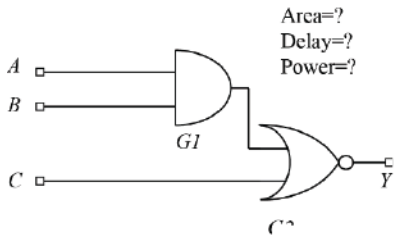
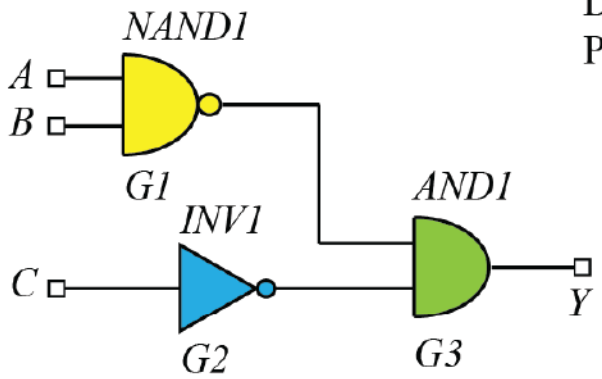
Logic Function:

$$Y = \left(((A.B)'.C')'\right)'$$
$$= (A.B)'.C'$$
$$= (A.B + C)'$$

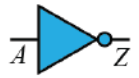
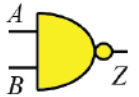
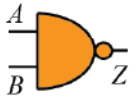
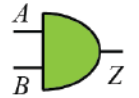
Illustration of Mapping: Solution 2



Given: $Y = (A.B + C)'$



Area=13
Delay=17,13
Power=55

Cell Name	Symbol	Function	Area	Delay	Power
INV1		*Z=A'*	1	4	5
NAND1		*Z=(A.B)'*	4	8	20
NAND1_LP		*Z=(A.B)'*	5	12	6
AND1		*Z=A.B*	8	9	30

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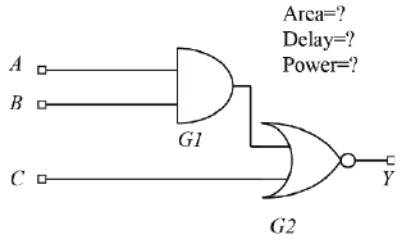
Logic Function:

$Y = (A.B)'.C'$

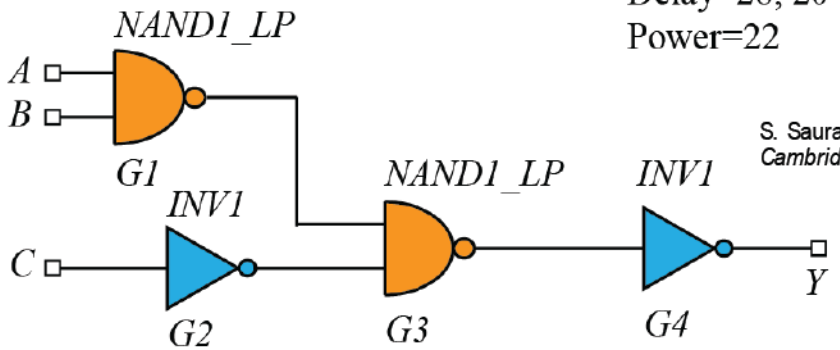
$= (A.B + C)'$

Illustration of Mapping: Solution 3



Given: $Y = (A.B + C)'$

Area=12
Delay=28, 20
Power=22



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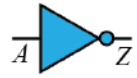
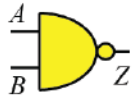
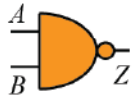
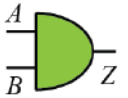
Cell Name	Symbol	Function	Area	Delay	Power
INV1		*Z=A'*	1	4	5
NAND1		*Z=(A.B)'*	4	8	20
NAND1_LP		*Z=(A.B)'*	5	12	6
AND1		*Z=A.B*	8	9	30

Logic Function:

$Y = \left(((A.B)'.C')'\right)'$

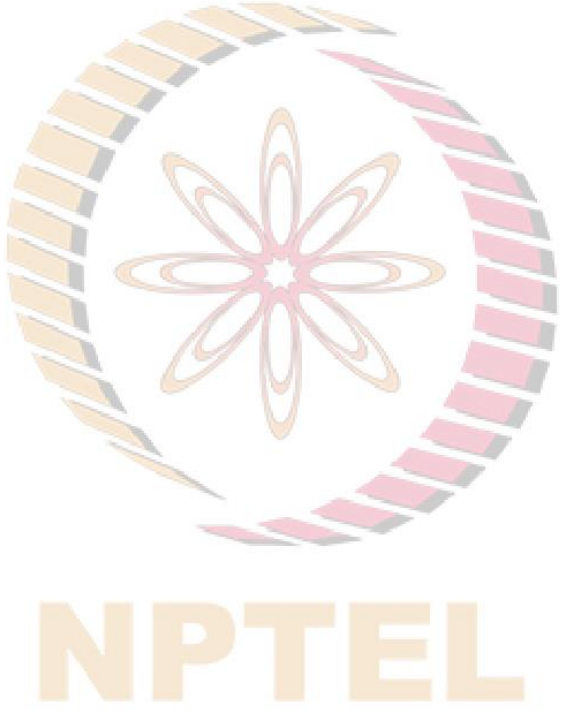
Summary of Solutions

	Area	Delay	Power	Comments
Solution 1	10	20	50	Minimum Area
Solution 2	13	17	55	Minimum Delay
Solution 3	12	28	22	Minimum Power

Technology Mapping: Approaches

Two approaches:

- Structural Mapping
- Boolean Mapping



References

- G. D. Micheli. “Synthesis and Optimization of Digital Circuits”. *McGraw-Hill Higher Education*, 1994.
- S. Saurabh, “Introduction to VLSI Design Flow”. Cambridge: *Cambridge University Press*, 2023.