VLSI DESIGN FLOW: RTL TO GDS

Lecture 25
Constraints I

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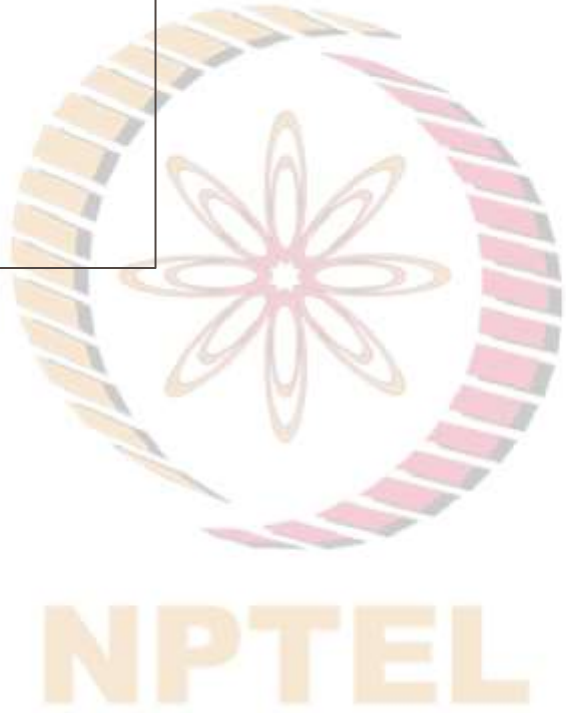
Lecture Plan

- Basics of constraints
- Clock constraints
- Input/Output constraints
- Timing exceptions



Constraints: Basics

Constraints are:

- **Requirements** of a design that needs to be honoured or attempted to be honoured by the CAD tools
- **Information** about a design that could potentially be exploited by the CAD tools to improve the PPA of the design

- Constraints are normally specified in **Synopsys Design Constraints (SDC)**
- ASCII format written in **Tool Command Language (TCL)**

create_clock -period 10 -waveform {5 10} [get_ports CLK]

set_clock_transition -rise 0.1 [get_clocks CLK]

set_clock_uncertainty 0.2 [get_clocks CLK]

set_input_delay -clock CLK 3.0 [get_ports INPA]

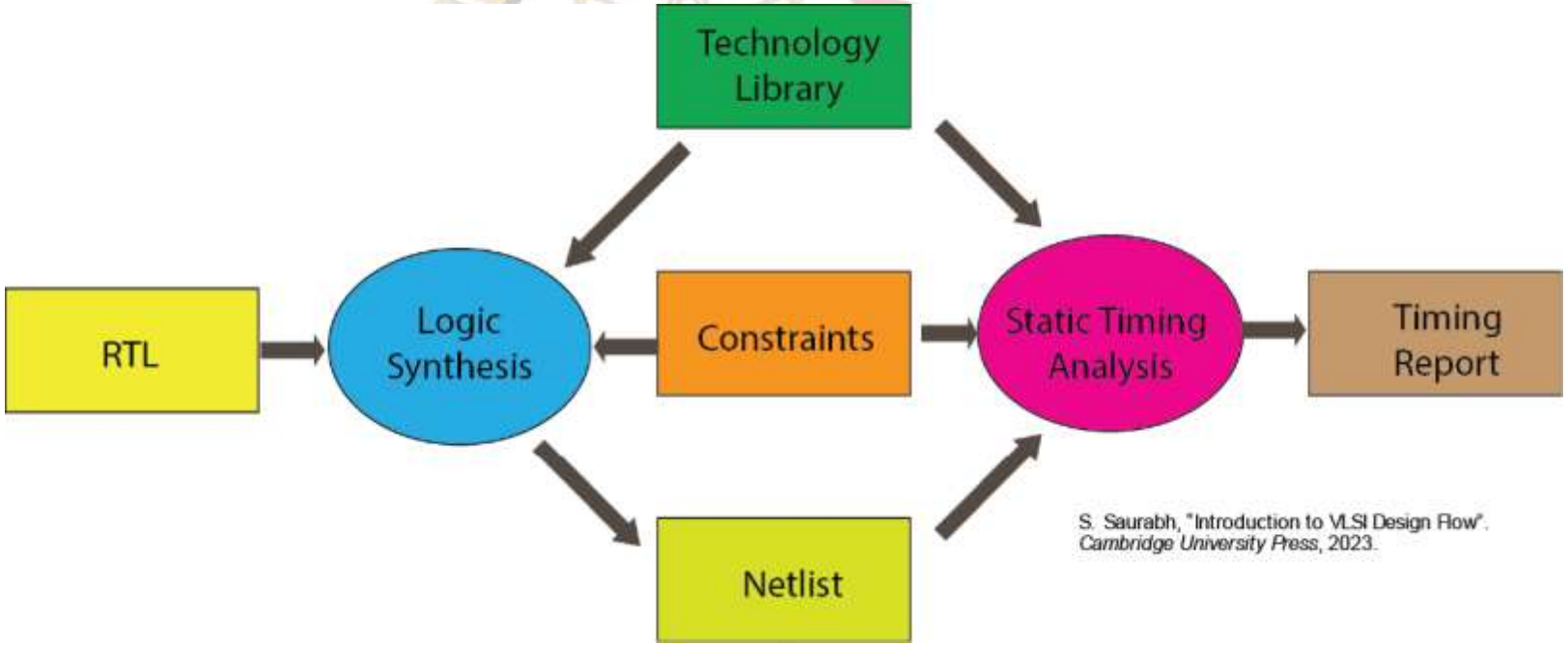
set_output_delay -clock CLK 3.0 [get_ports INPA]

set_false_path –from [get_ports TE]

set_multicycle_path –from [get_ports mult_out]

Constraints: Application

- Most of the constraints are related to *timing* of a design (also called timing constraints)
  - Employed by implementation tool to gather information about the expected timing behavior
  - Employed by STA tool to verify timing



S. Saurabh, "Introduction to VLSI Design Flow", *Cambridge University Press*, 2023.

Constraints: What is the origin?

Constraints are normally manually written

- Designer have the knowledge of design goals and environmental constraints
- There are certain tools for automatic constraints generation
  - Some user intervention is always required

It is important to write correct constraints

- Otherwise design implementation tools can produce unexpected results
- There should be consistency between different constraints
- Constraints should be consistent with design attributes

Constraints: Types

Clock signal

- Attributes of a clock signal such as frequency, duty cycle, skew, uncertainty and delay

Environment under which the design operates

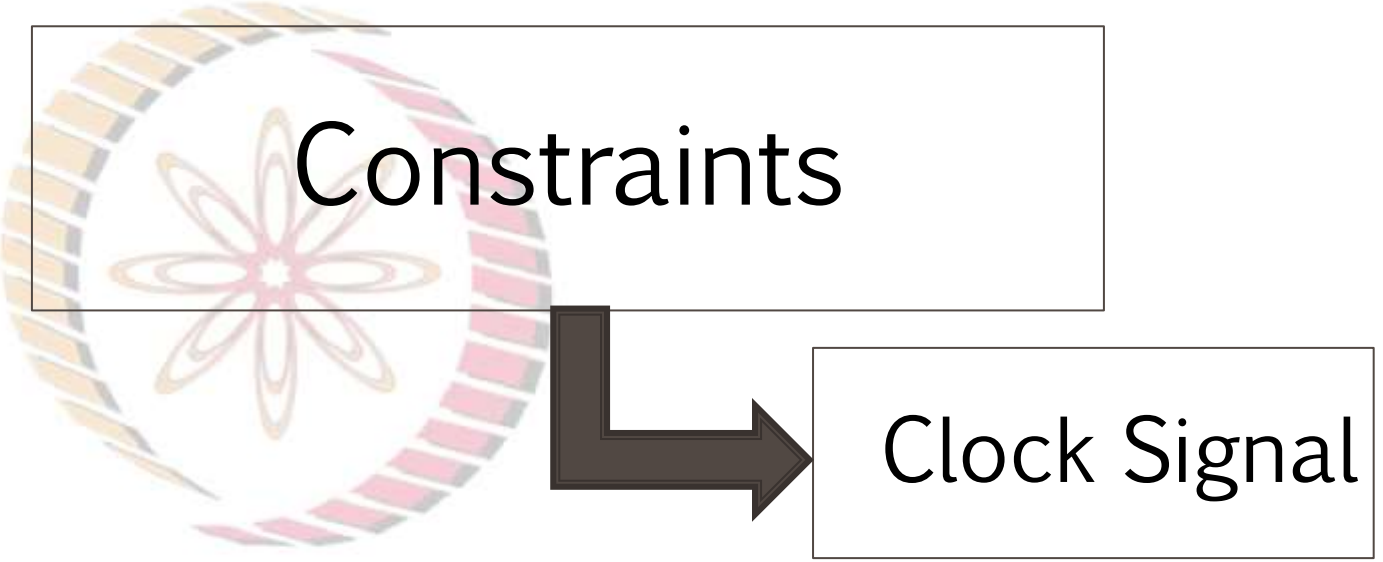
- Attributes of external incoming signal and expected behavior of the signals produced by a design

Functionality of the design (informative)

- Timing exceptions (paths that are *false* and paths that are allowed to behave differently than traditional synchronous behavior), modes of design

Design rules and optimization constraints

- Maximum slew at the port, maximum capacitance at a pin, and soft constraints

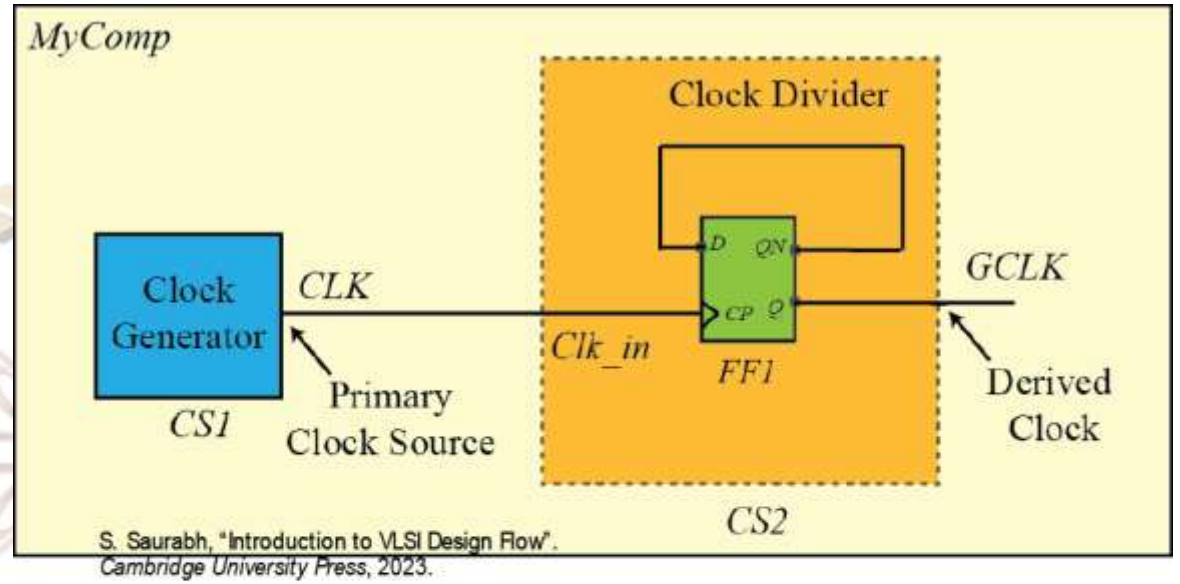


Clock Constraints: Sources

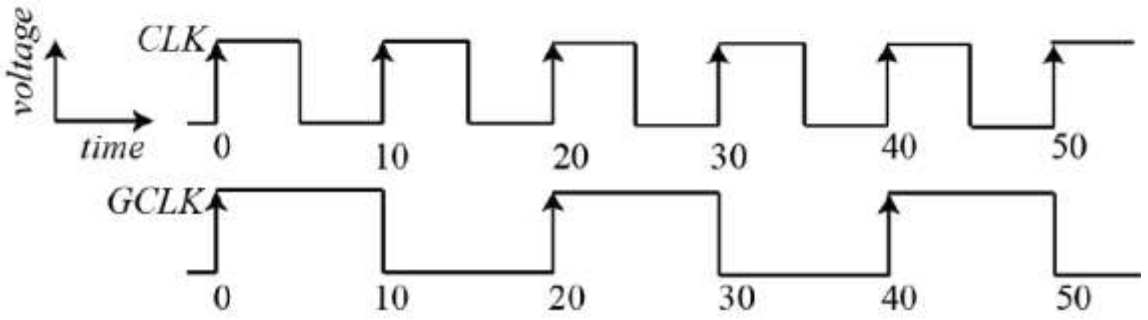
Two types of clock sources

- **Primary clock sources**: waveform independent of other clock sources in that design
- **Derived clock sources**: waveform depends on other clock sources

- **Master clock**: clock from which we derive another clock is known as the master clock of the derived clock
  - *CS1* is the master clock source of *CS2*

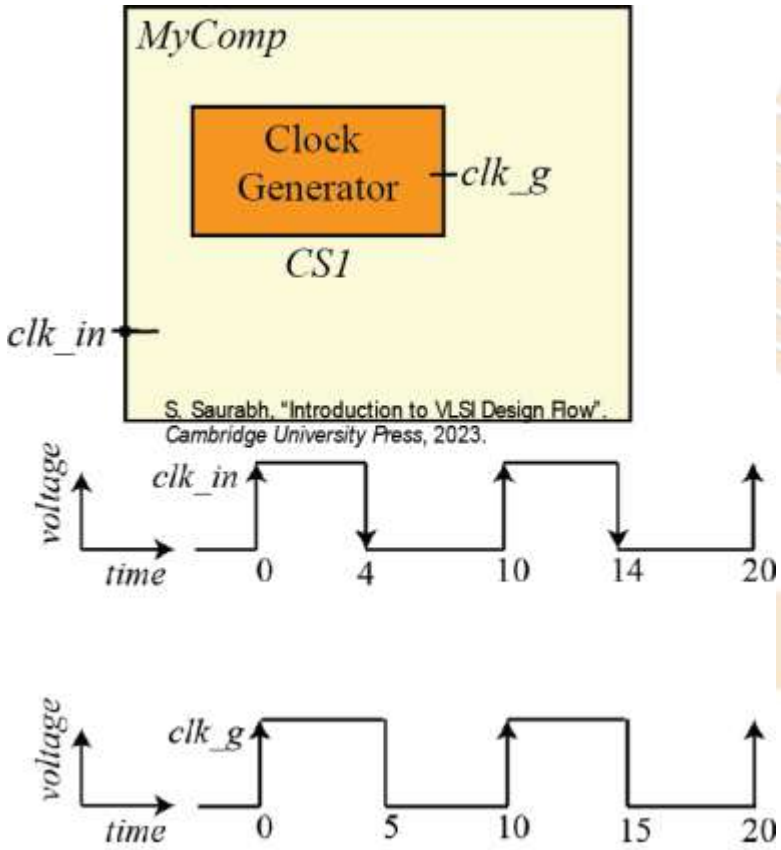


S. Saurabh, "Introduction to VLSI Design Flow". Cambridge University Press, 2023.



Primary Clock Source Definition

create_clock: defines the primary clock source in a design



current_design *MyComp*

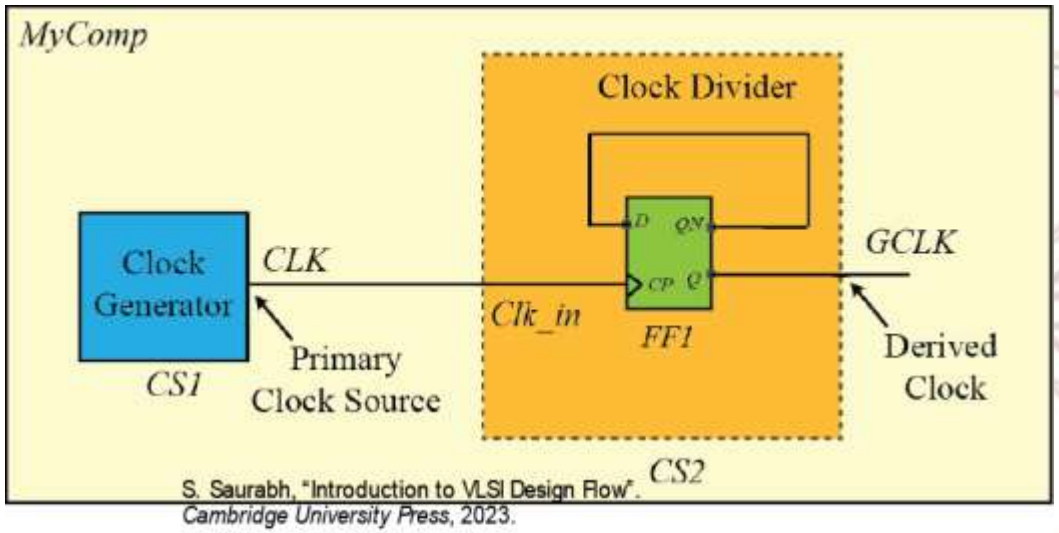
create_clock -name EXT_CLK -period 10 -waveform {0 4} [get_ports *clk_in*]

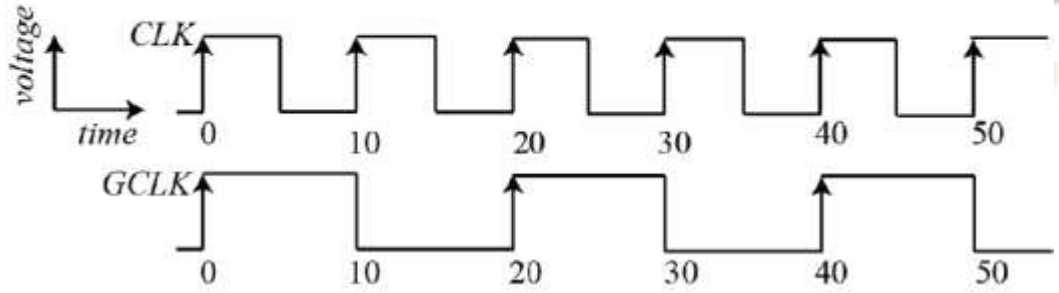
create_clock -name INT_CLK -period 10 [get_pins *CS1/clk_g*]

-waveform: time when the clock edges occur, starting from rise-edge

Derived Clock Source Definition

create_generated_clock: define derived clock sources



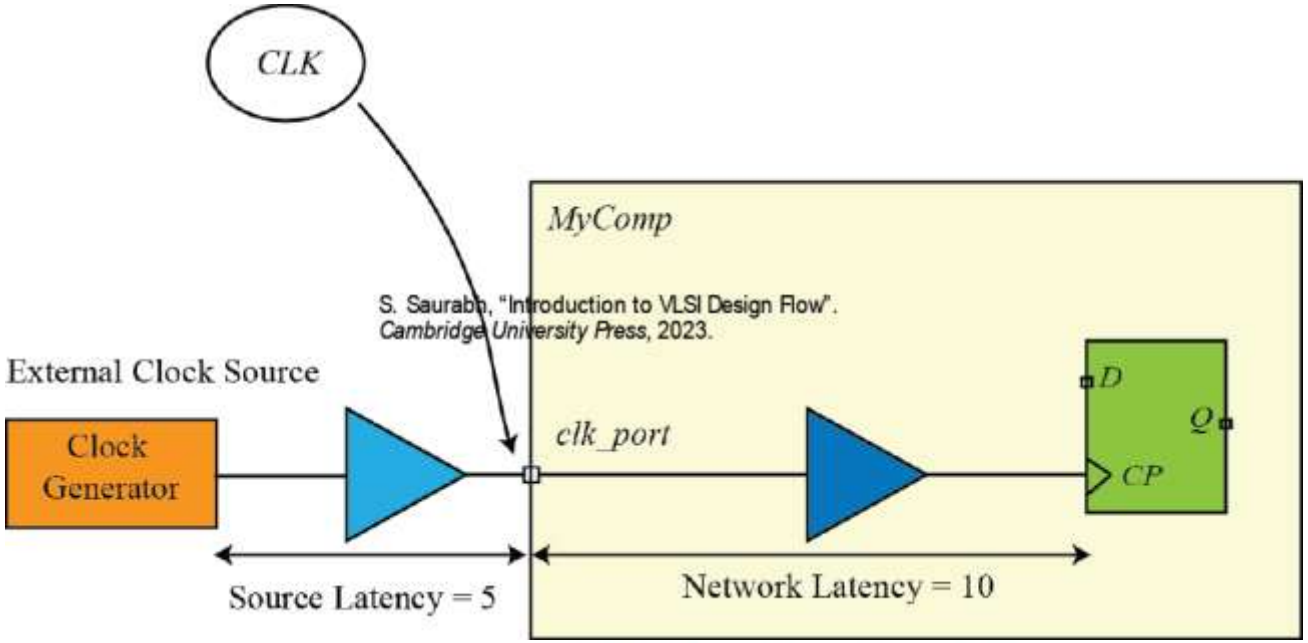


create_clock -name CLK -period 10 [get_pins *CS1/CLK*]

create_generated_clock -name GCLK -divide_by 2 –source [get_pins *CS1/CLK*] [get_pins *CS2/GCLK*]

Attributes of Clock Signal: Latency

set_clock_latency: specify clock latency




```
create_clock -name CLK -period 200 [get_ports clk_port]
set_clock_latency 5 -source [get_clocks CLK]
set_clock_latency 10 [get_clocks CLK]
```

Attributes of Clock Signal: Uncertainty

set_clock_uncertainty: unpredictable deviation of the clock edges from the ideal value

Clock uncertainty can be used to model:

- Jitter: temporal variation
- Skew: spatial variation
- Safety margins

```
create_clock -name CLK -period 200 [get_ports clk_port]
set_clock_uncertainty 15 -hold [get_clocks CLK]
set_clock_uncertainty 20 -setup [get_clocks CLK]
```

Attributes of Clock Signal: Transition

set_clock_transition: specify an estimated clock transition time

```
create_clock -name CLK -period 2000 [get_ports clk_port]
set_clock_transition 10 [get_clocks CLK]
```

References

- S. Saurabh, “Introduction to VLSI Design Flow”. Cambridge: *Cambridge University Press*, 2023.
- Bhasker, Jayaram, and Rakesh Chadha. *Static timing analysis for nanometer designs: A practical approach*. Springer Science & Business Media, 2009.