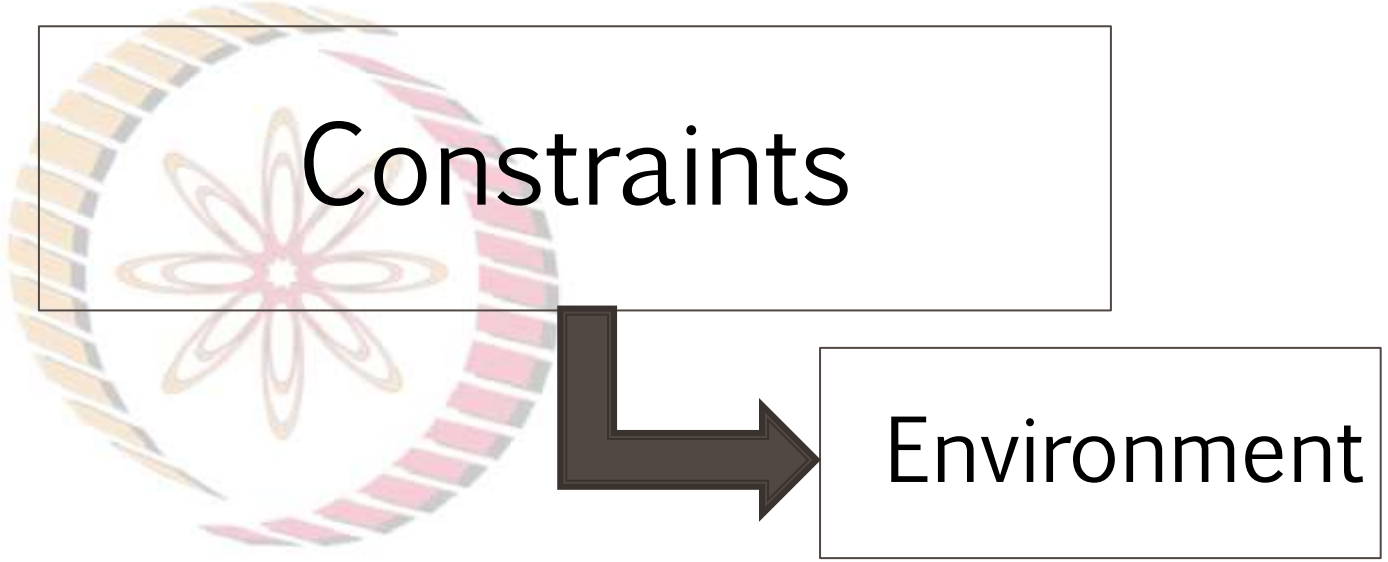
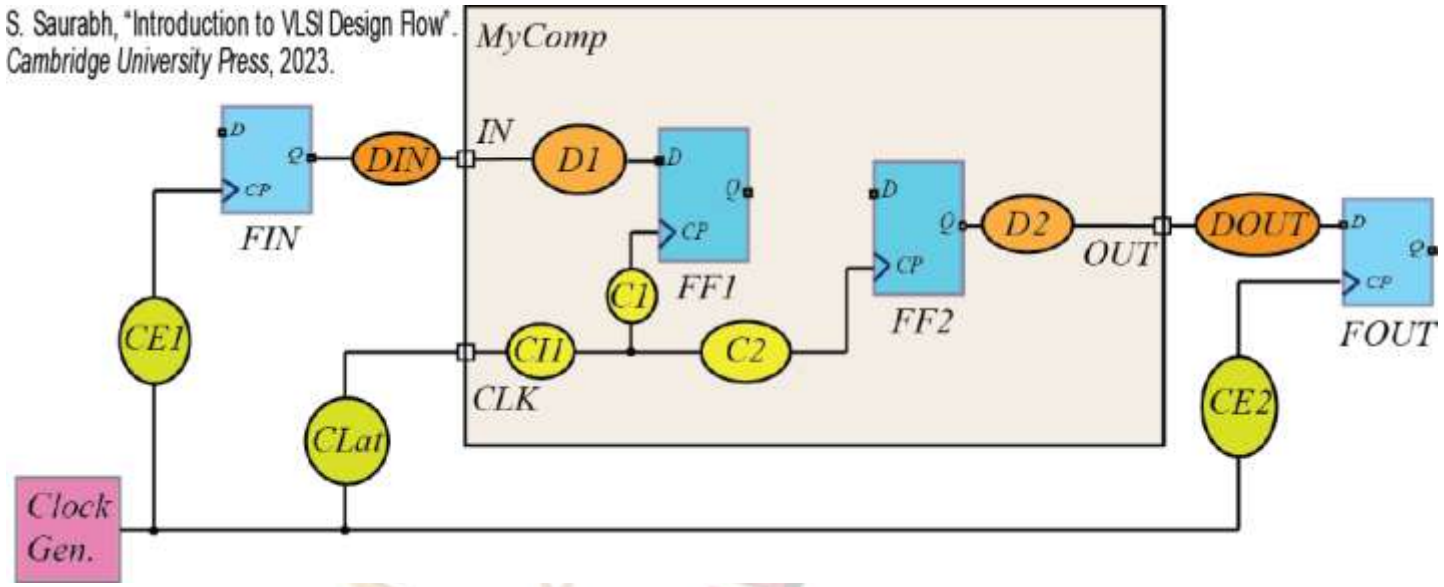
VLSI DESIGN FLOW: RTL TO GDS

Lecture 26
Constraints II

Sneh Saurabh
Electronics and Communications Engineering
IIIT Delhi



Static Timing Analysis: Environment of design

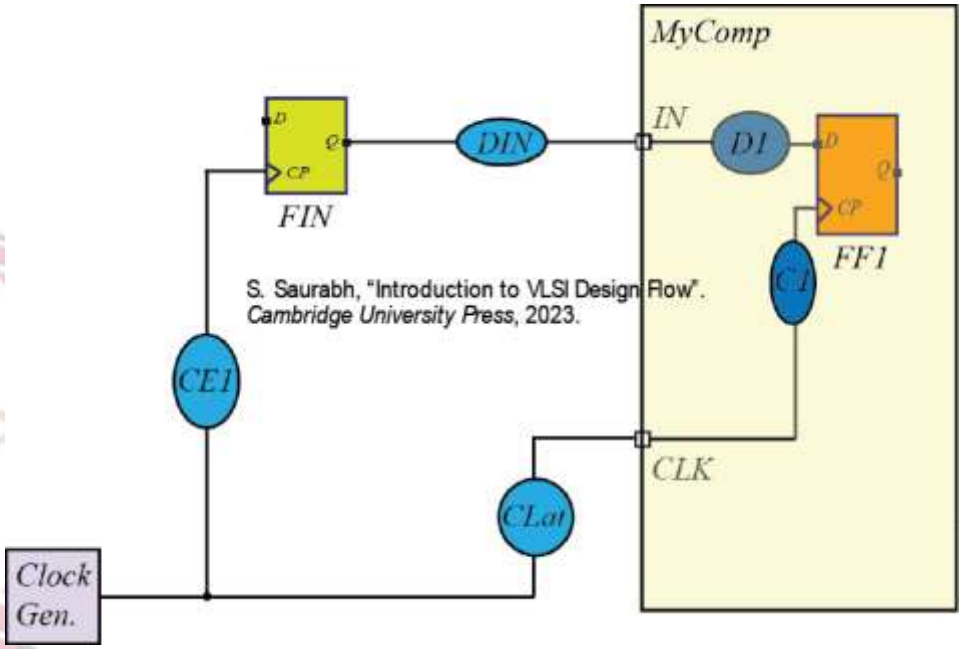


Environment of design puts additional constraints on the signal entering/leaving a design

- Signal entering the design at the input port encounters delay
- Signal leaving the design at the output port will encounter delay and get captured externally
  - Should meet setup/hold requirements at *FOUT*
  - Check for setup/hold must also be performed at the output port

Input Port Constraints: *set_input_delay*

- Signal gets delayed before entering the design
  - ➢ Lesser part of clock-period is available for the signal to reach flip-flop within the design
- Delay external to design at the input ports is modelled using ***set_input_delay***



- Value of input delay = Delay of $CE1$ + CP → Q delay of FIN + Delay of DIN

```
create_clock –name CLK –period 2000 [get_ports CLK_PORT]

set_input_delay –clock [get_clocks CLK]  100 [get_ports IN]
```

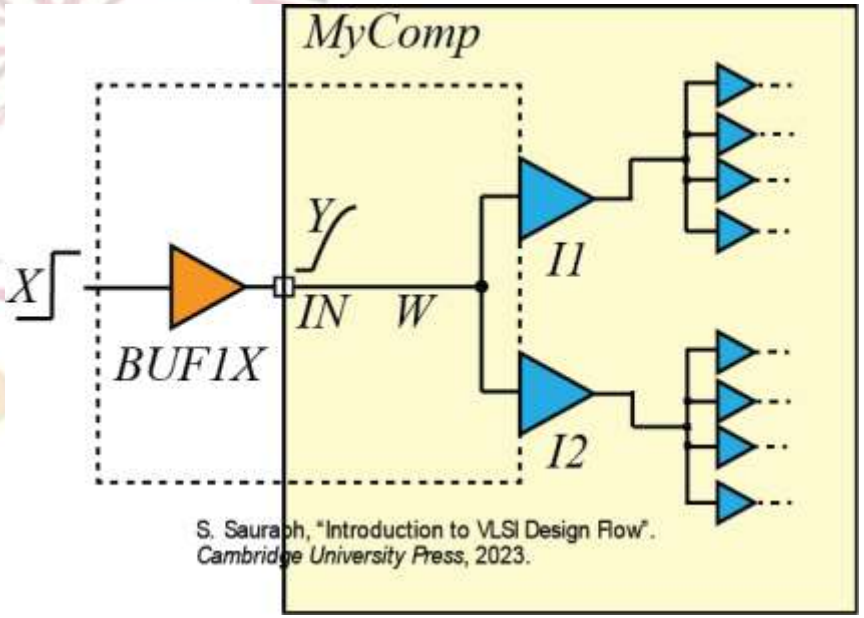
Transition at Input Port

- ***set_input_transition***: model slew of incoming signal

set_input_transition 10 -max -rise [get_ports *IN*]

- ***set_driving_cell :*** driver of inputs

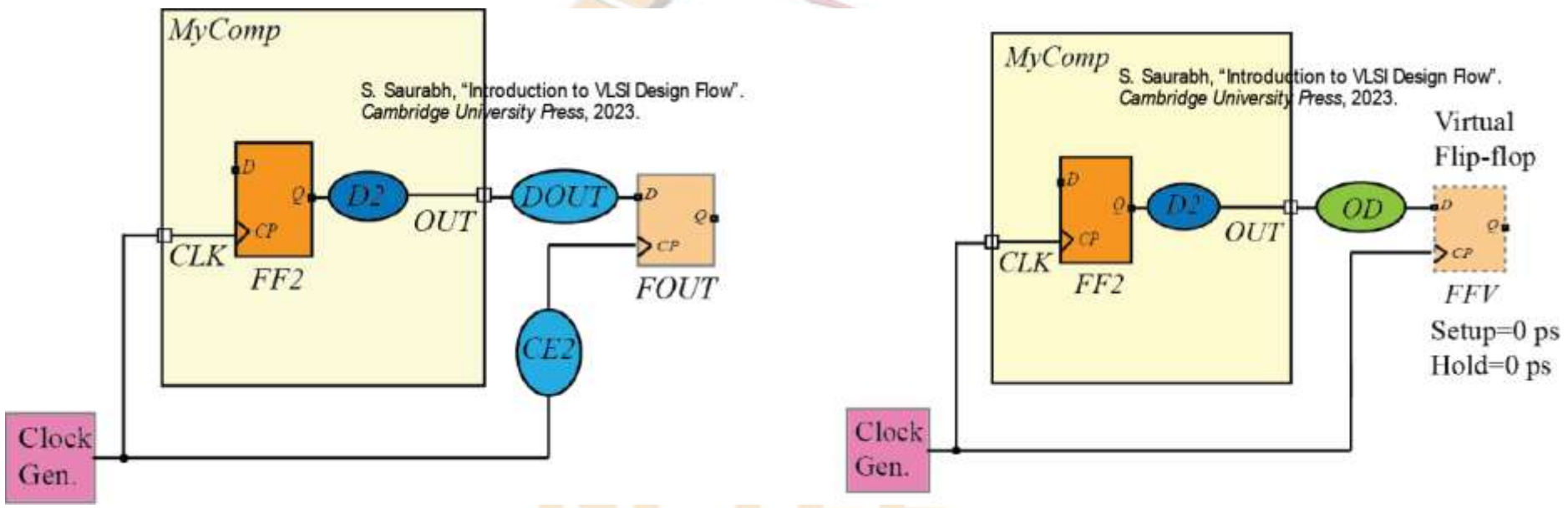
set_driving_cell -lib_cell *BUF1X* -library *tech14nm* [get_ports *IN*]



Output Port Constraints: *set_output_delay*

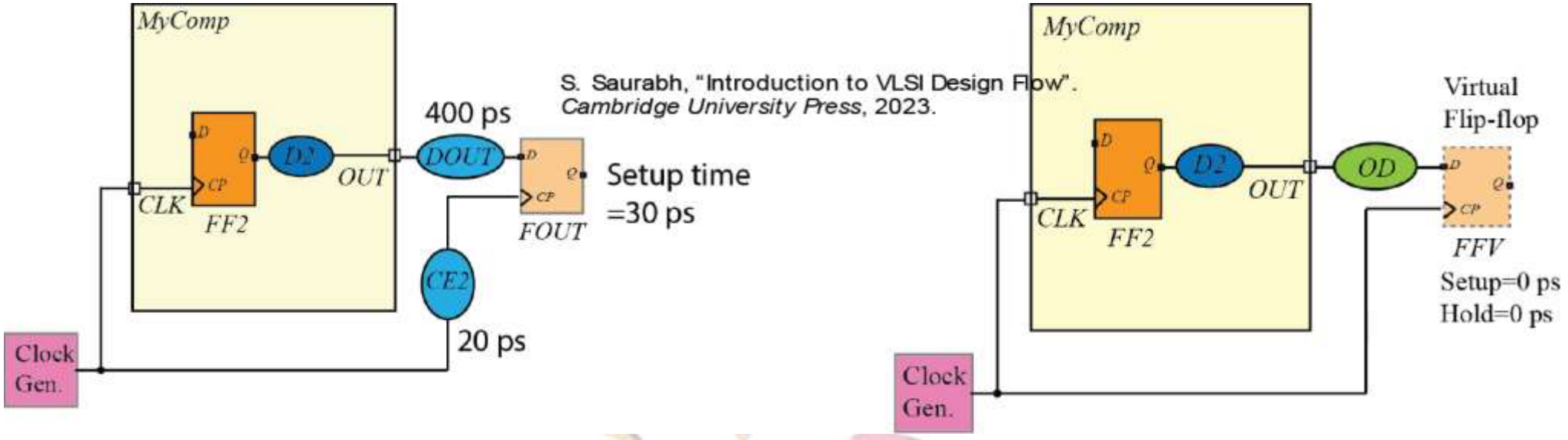
Output Delay: signal leaving a design must meet the setup/hold constraints of the flip-flop that captures that signal

- Constraints of the external flip-flop is modelled using ***set_output_delay***



- The delay of OD needs to be chosen such that the setup/hold requirements in the actual circuit and equivalent circuit match
- Delay of OD is specified in *set_output_delay* command

Illustration: *set_output_delay*



$$T_{int} + 400 < T_{clk} + 20 - 30$$

$$T_{int} + T_{OD} < T_{clk}$$

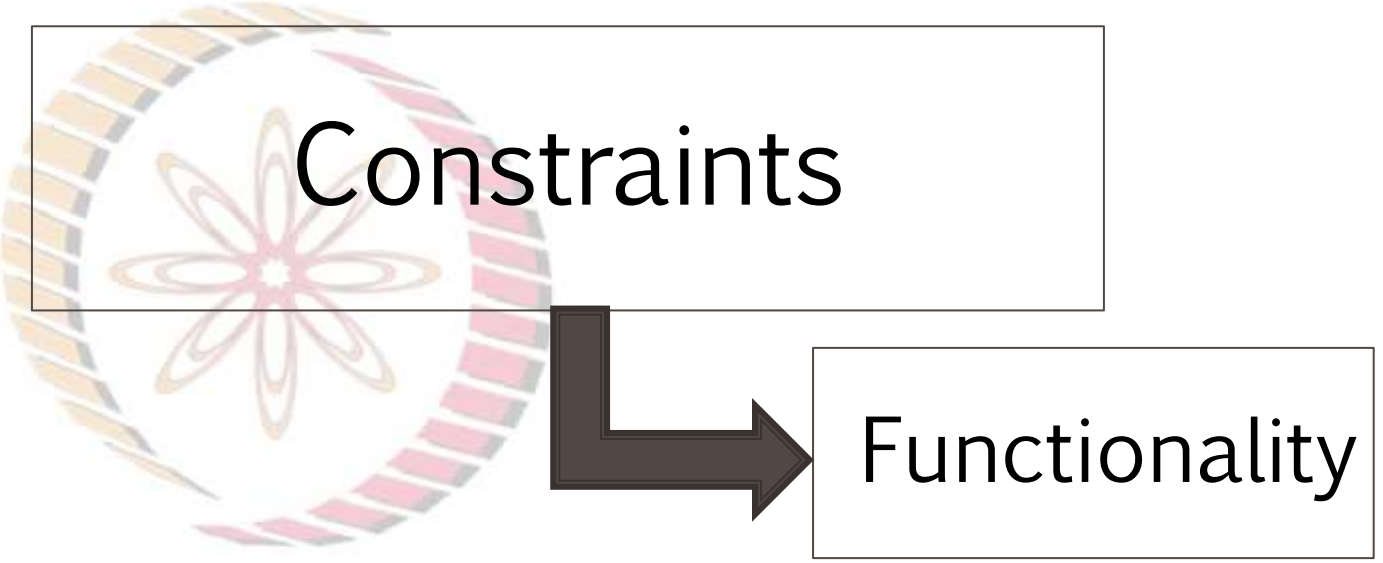
$$T_{OD} = 400 - 20 + 30 = 410$$

```
create_clock -name SYS_CLOCK -period 2000 [get_ports CLK]
set_output_delay 410 -max -clock [get_clocks SYS_CLK]  [get_ports OUT]
```

Load at Output Port

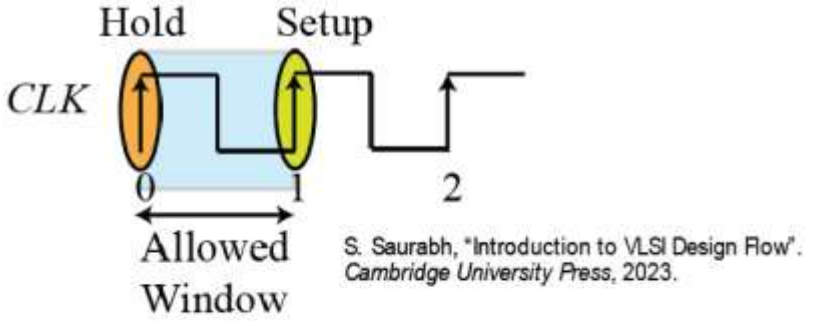
- *set_load*: load that will be driven by the output port

```
set_load 0.039 [get_ports OUT]
```

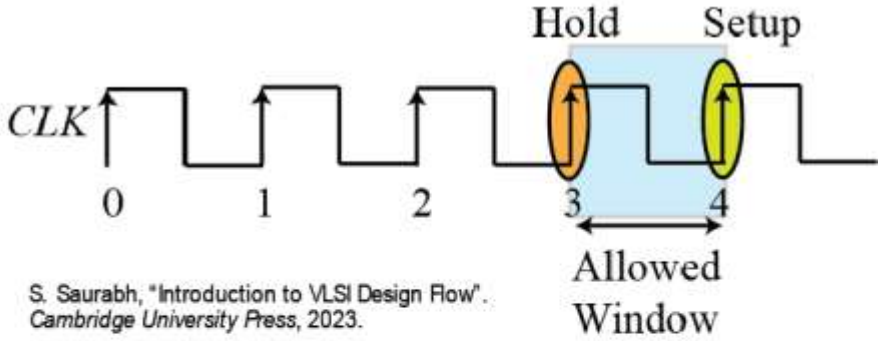


Timing Exceptions

- *set_false_path*: To make exceptions from analysing certain paths that may not be exercised
- *set_multicycle_path*: To inform the STA tool that certain path may take more than one cycle

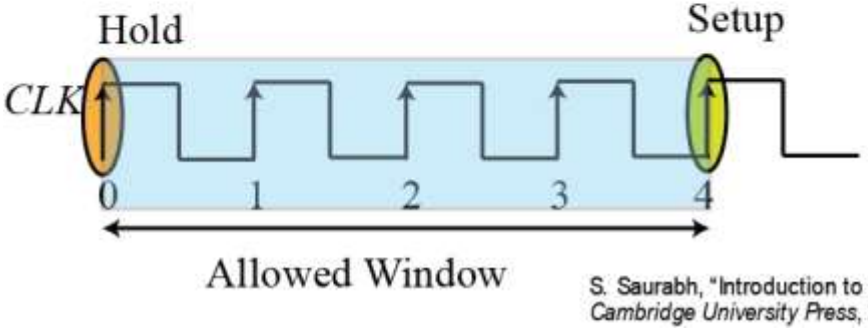


S. Saurabh, "Introduction to VLSI Design Flow". *Cambridge University Press*, 2023.



S. Saurabh, "Introduction to VLSI Design Flow". *Cambridge University Press*, 2023.

set_multicycle_path 4 -setup -from [get_pins *FF1/CP*] -to [get_pins *FF2/D*]



S. Saurabh, "Introduction to VLSI Design Flow". *Cambridge University Press*, 2023.

set_multicycle_path 4 -setup -from [get_pins *FF1/CP*] -to [get_pins *FF2/D*]

set_multicycle_path 3 -hold -from [get_pins *FF1/CP*] -to [get_pins *FF2/D*]

Constant Value to Port/Pin

- *set_case_analysis*: assign constant value to some port/pin

```
set_case_analysis 1 [get_ports SCAN_ENABLE]
```

```
set_case_analysis 1 [get_ports SLEEP_MODE]
```

References

- S. Saurabh, “Introduction to VLSI Design Flow”. Cambridge: *Cambridge University Press*, 2023.
- Bhasker, Jayaram, and Rakesh Chadha. *Static timing analysis for nanometer designs: A practical approach*. Springer Science & Business Media, 2009.