VLSI DESIGN FLOW: RTL TO GDS

Lecture 28
Timing-driven Optimizations

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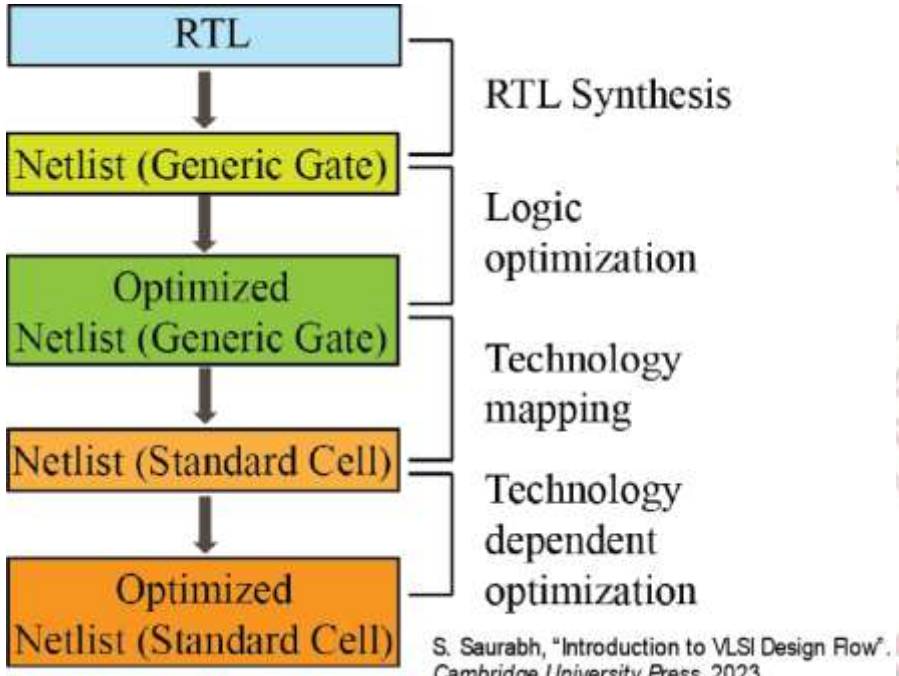
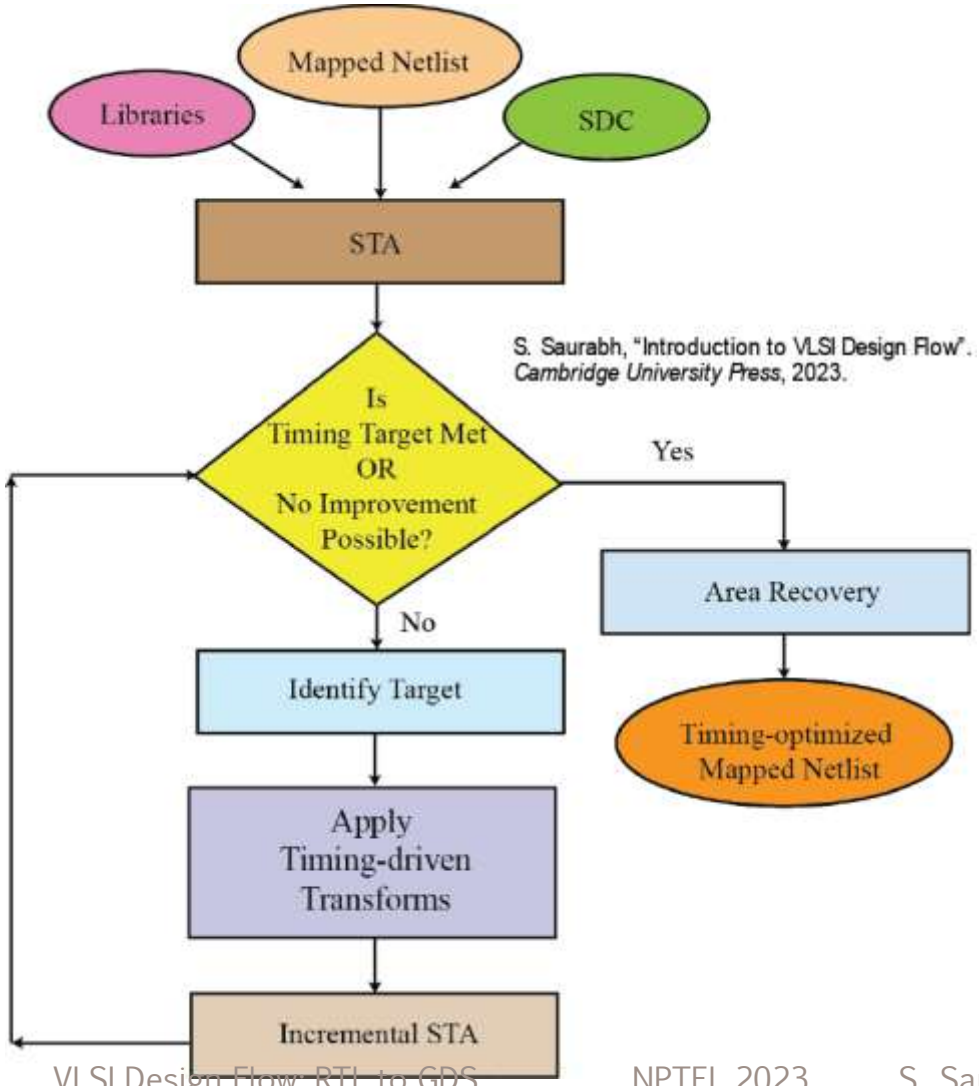
Lecture Plan



S. Saurabh, "Introduction to VLSI Design Flow". *Cambridge University Press*, 2023.

- Timing-driven Optimizations

Timing-driven Optimization: Flow



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Timing Driven Optimization: Resizing

- Libraries contain cells of same functionality and different sizes
  - ➢ Size of the cell increases, delay decreases

Resizing:

- Replace a cell *C1* with another cell *C2* that produces the same Boolean function but has a different size

Example: cell *C1* replaced with a functionally equivalent cell *C2* of a **larger size**

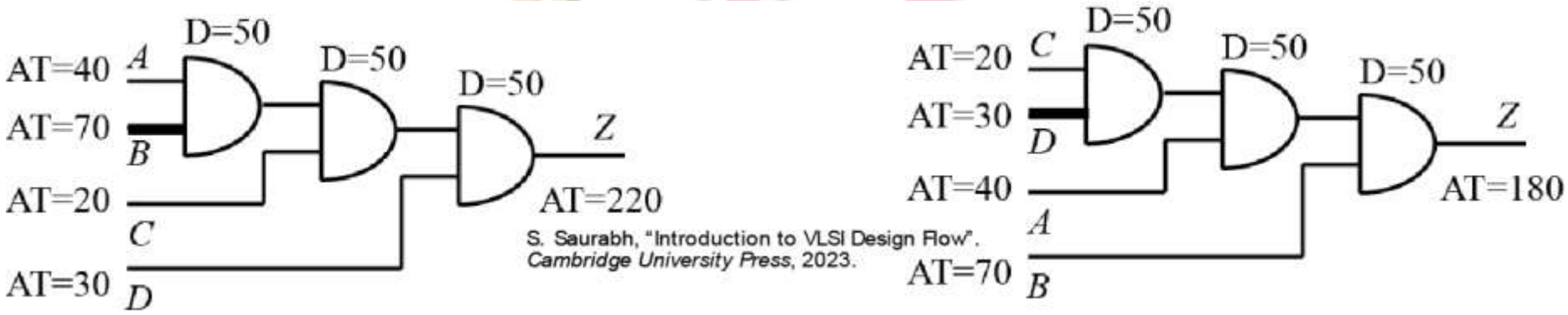
Effects:

1. Delay and output slew of *C2* can reduce
   - ➢ Delay of cells in the fanout of *C2* can also reduce
2. Delay and output slew of the driver of *C2* can increase
   - ➢ Delay of the cells in its fanout, including that of C2, can increase

Timing Driven Optimization: Restructure (1)

Rewiring:

- Timing critical signals are moved closer to the sink in a cone of logic to reduce the overall path delay



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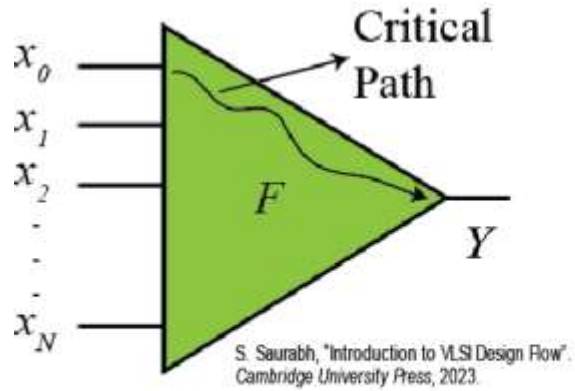
Timing Driven Optimization: Restructure (2)

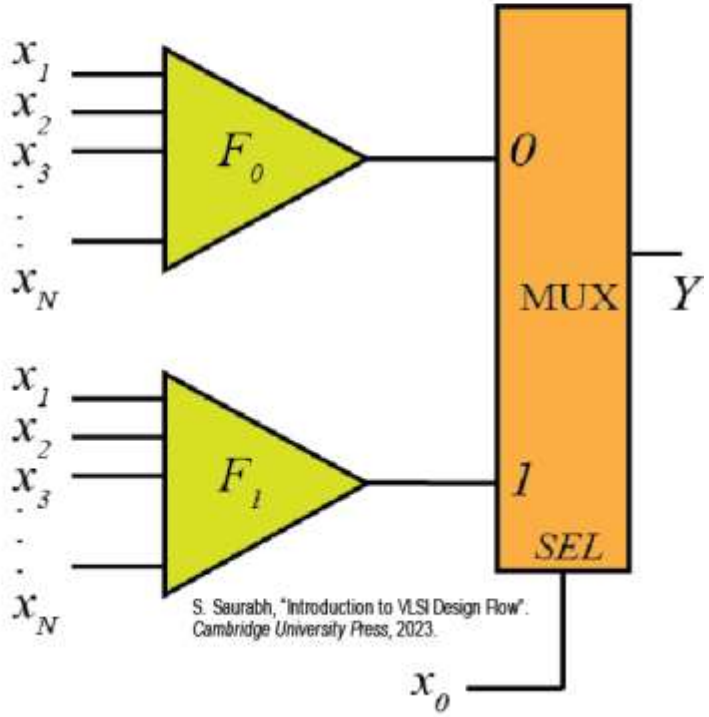


$$Y = F(x_0, x_1, x_2, \dots, x_N)$$

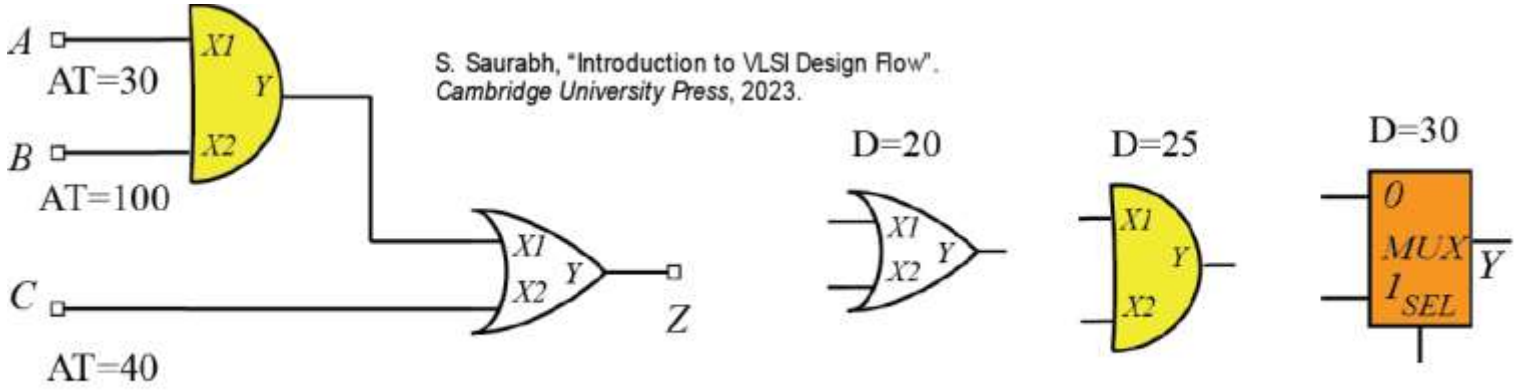
- Let x_0 be the signal that arrives last (AT of x_0 is greatest) and is on the critical path
- How to restructure the circuit such that the worst delay of the circuit improves?

Shannon Expansion

- $F_0 = F(0, x_1, x_2, \dots, x_N)$
- $F_1 = F(1, x_1, x_2, \dots, x_N)$



Restructure: Illustration

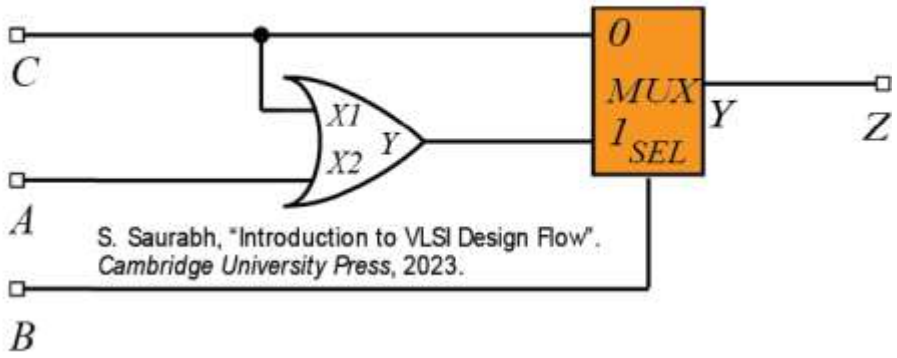


Arrival Time: 145 ps

$$Z = F(A, B, C) = AB + C$$

$$F_{B=0} = C$$

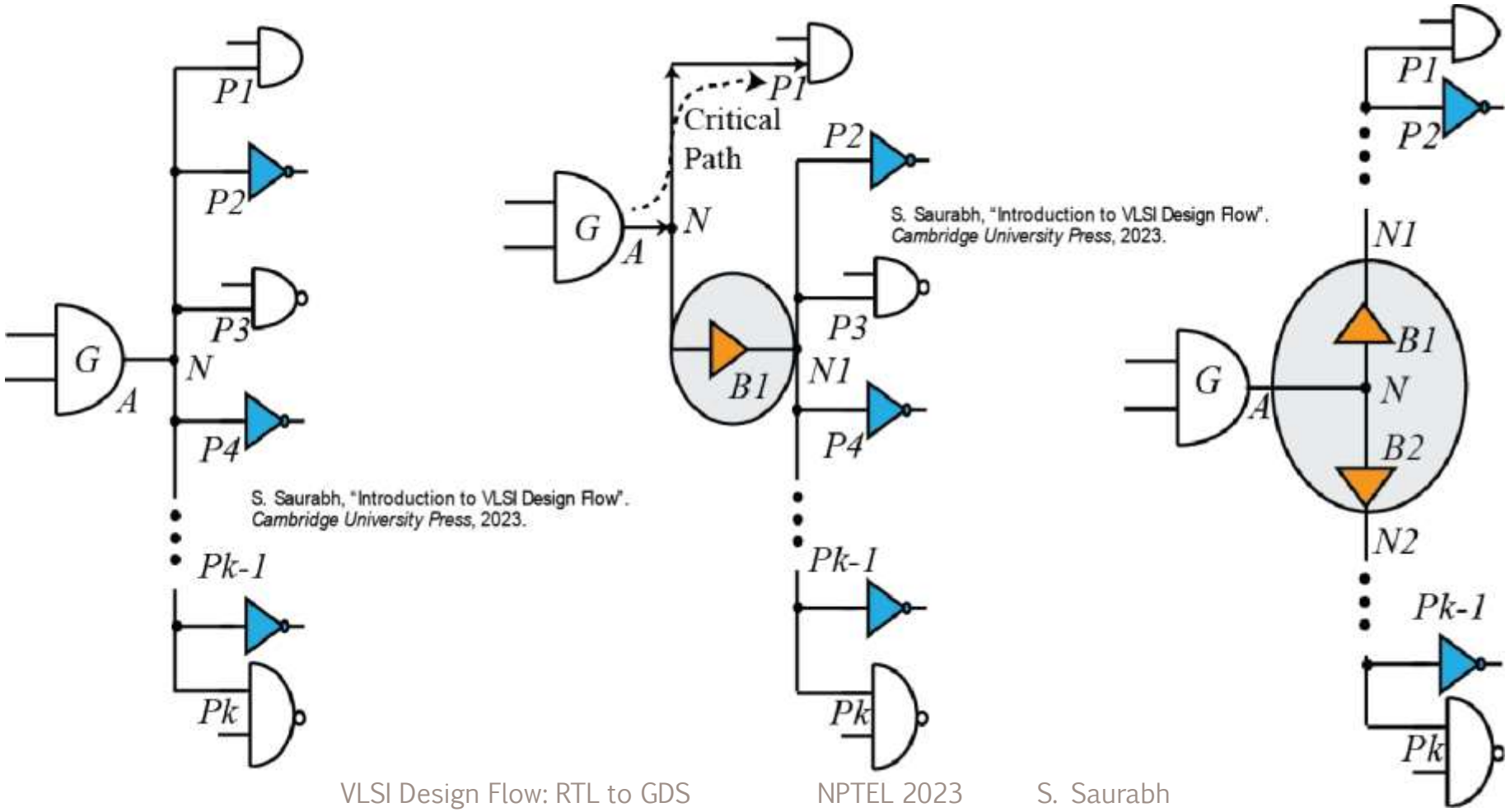
$$F_{B=1} = A + C$$



Arrival Time: 130 ps

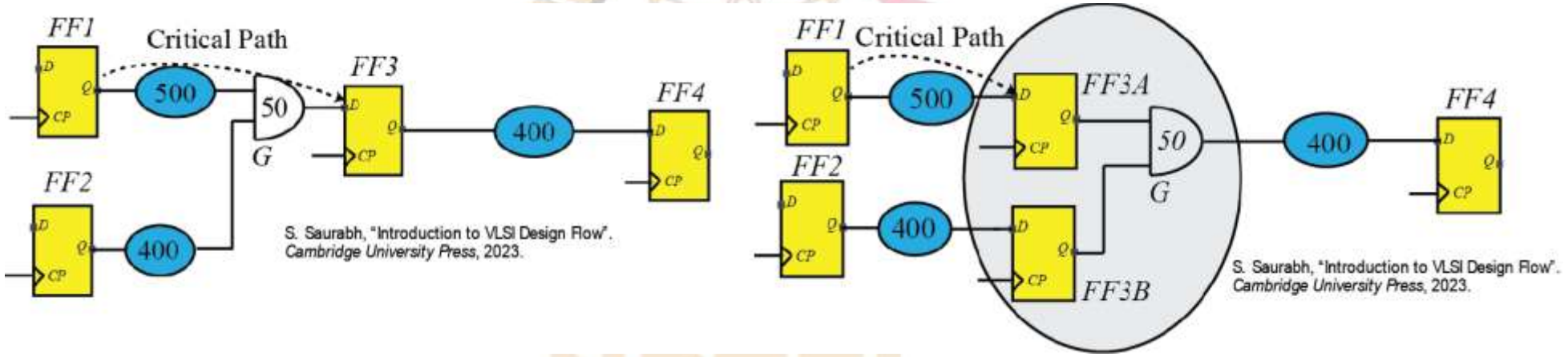
Fanout Optimization

Fanout optimization: inserting buffers in a high-fanout



Retiming

Retiming: balance the amount of logic between registers



References

- S. Saurabh, “Introduction to VLSI Design Flow”. Cambridge: *Cambridge University Press*, 2023.