VLSI DESIGN FLOW: RTL TO GDS

Lecture 36
Basic Concepts for Physical Design - II

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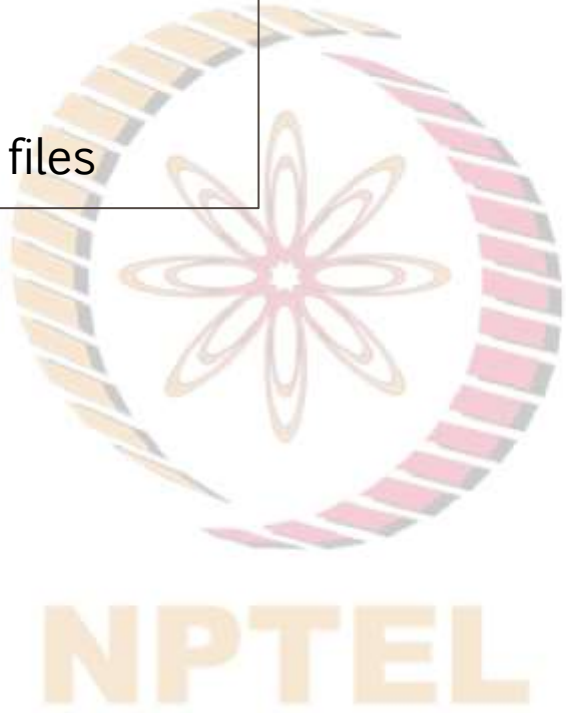
Lecture Plan

- Signal Integrity
- Antenna Effect
- Library Exchange Format (LEF) files



Signal Integrity

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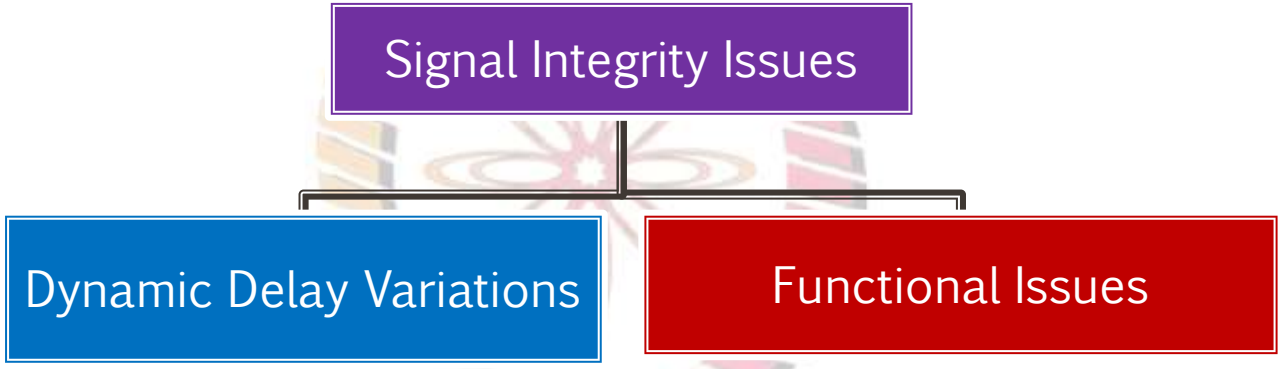
Effects of Coupling of Interconnects

Impact of coupling capacitance among interconnects

- Voltage in one interconnect can impact the voltage in the other
- Can create signal integrity problems in a circuit



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Signal Integrity

Dynamic Delay Variations

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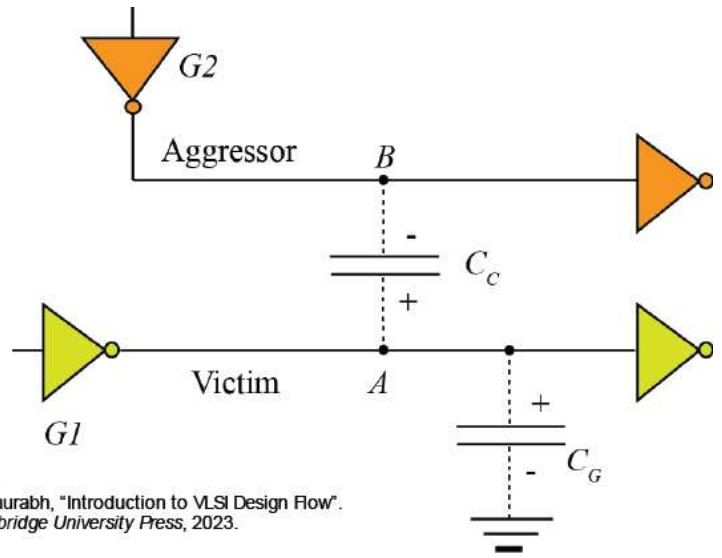
What is base delay?

Consider the portion of a circuit

- Let us assume A is the victim
  - ➢ The signal line at which we observe the signal integrity issue is known as the victim line
- Assume gate G1 (driver of the victim net A) makes a 0→1 transition at the output.
  - ➢ The driver G1 provides charge for the ground capacitor C_G to change from 0 to V_{DD}.



S. Saurabh, "Introduction to VLSI Design Flow". *Cambridge University Press*, 2023.

Case1: B is held constant to 0

- G1 needs to provide a charge for the coupling capacitance C_c to change from 0 to V_{DD}.
- Hence, G1 needs to charge $C_G + C_c$.

Case2: B is held constant to 1

- Initially charge on C_c is $-V_{DD}$ and finally 0
- Hence, G1 needs to charge $C_G + C_c$.

- The delay computed by assuming aggressors are held to constant logic is known as **base delay**.
- The base delay is same whether aggressor is at 0 or 1

- Base delay is obtained by ignoring SI effects

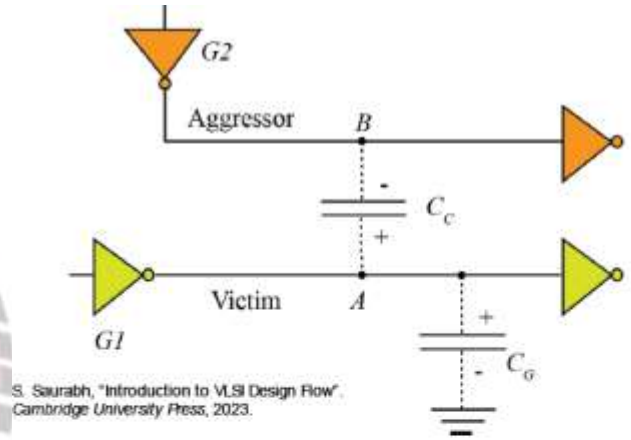
How is dynamic delay variations created?

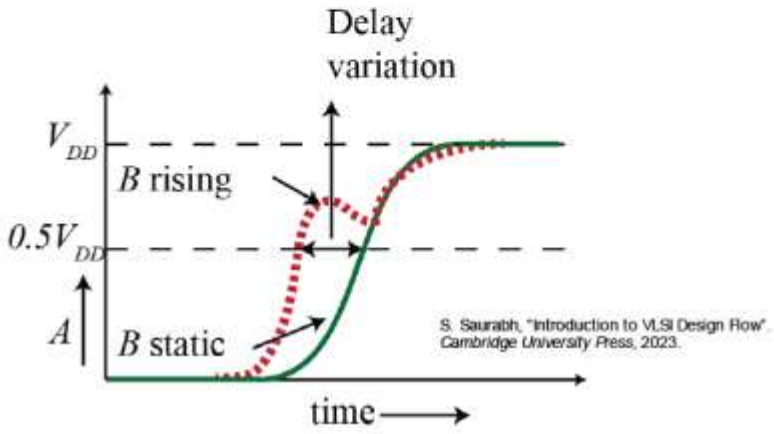
- Assume gate G1 (driver of the victim net A) makes a 0→1 transition at the output.

Case1: B also makes a 0→1 transition while A was transitioning:

- Voltage across C_c is 0 V, both initially and finally.
- Hence, less charge needs to be provided by G1 for charging C_c
- Delay of G1 will decrease.

- This effect is modeled as ***negative incremental delay*** over base delay





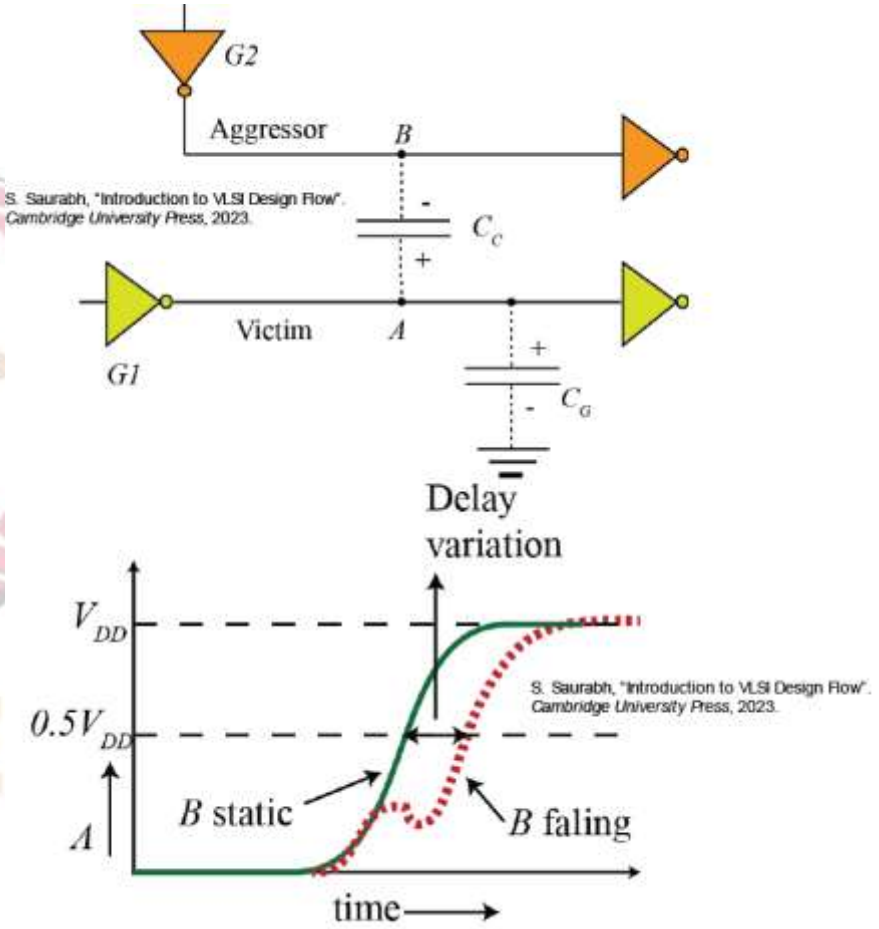
How is dynamic delay variations created?

- Assume gate G1 (driver of the victim net A) makes a 0→1 transition at the output.

Case2: B makes a 1→0 transition while A was transitioning:

- Voltage across C_c is $-V_{DD}$ initially and $+V_{DD}$ finally.
- Hence, in effect, $2C_c$ needs to be charged by G1
- Delay of G1 will increase.

- This effect is modeled as ***positive incremental delay*** over base delay



Signal Integrity

Noise or Glitches

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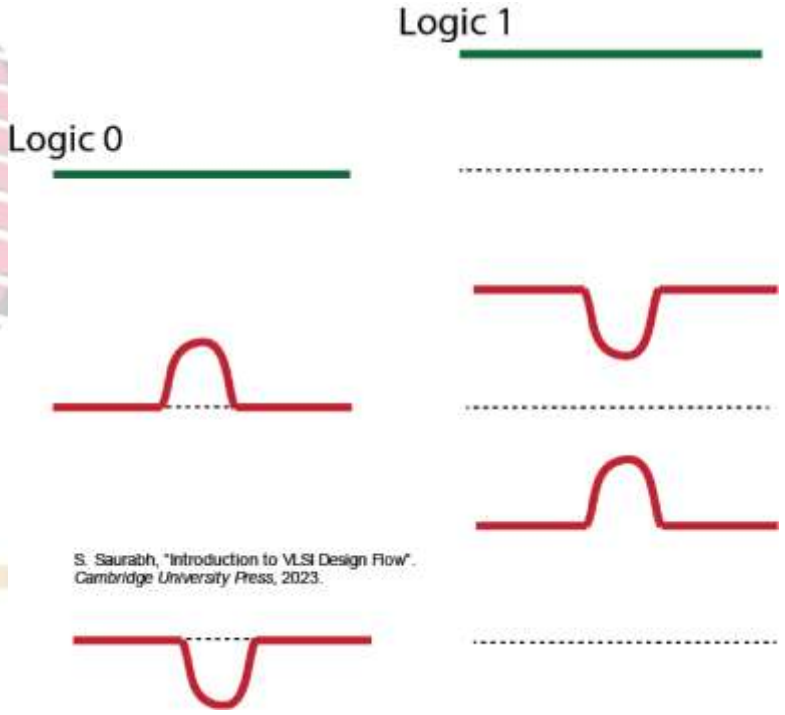
What is a Glitch?

- A glitch can occur in a victim net held at constant logic value due to a transition in the aggressor net.
- Glitches are also known as crosstalk noises

Depending on the value of the victim net and the type of transition at the aggressor nets, four types of glitches are possible:

a. Logic 0 has a rise glitch,
b. Logic 0 has an undershoot
c. Logic 1 has a fall glitch
d. Logic 1 has an overshoot.



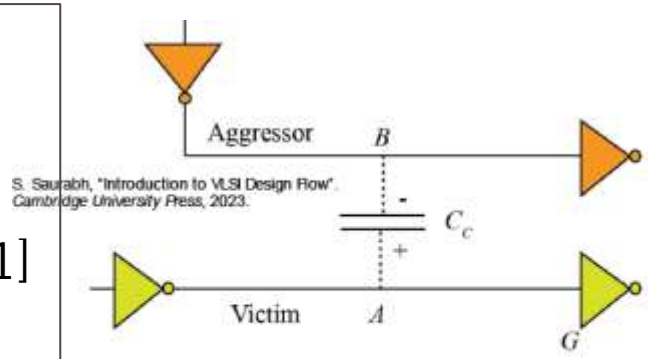
How are Glitches Created?

Consider the portion of a circuit

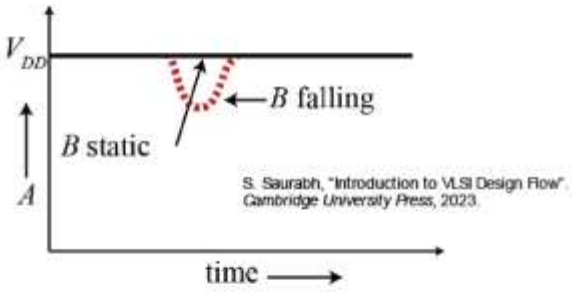
- Let us assume A is the victim
- Assume that A is at a steady state of V_{DD} [logic 1]
- Assume that line B is also at the steady state of V_{DD} [logic 1]
- Voltage across the coupling capacitor C_C is 0 V.

- Assume that the neighboring line B makes a quick transition from V_{DD} to 0 V
- The coupling capacitor C_C now gets charged to $+V_{DD}$ due to voltage difference in lines A and B
- The driver of the line A will supply this charge, and it will cause a temporary dip in the voltage of the line A

- Similarly, when the aggressor (line B) makes a 0 to V_{DD} transition, there can be a bump in the voltage of the victim (line A) that was held at logic 0



S. Saurabh, "Introduction to VLSI Design Flow", Cambridge University Press, 2023.



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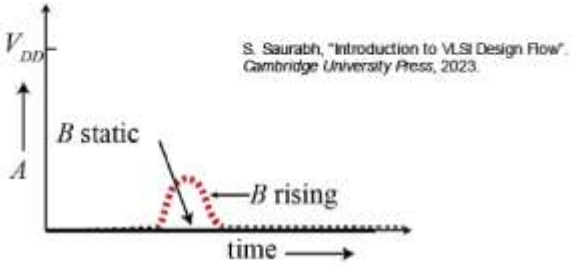

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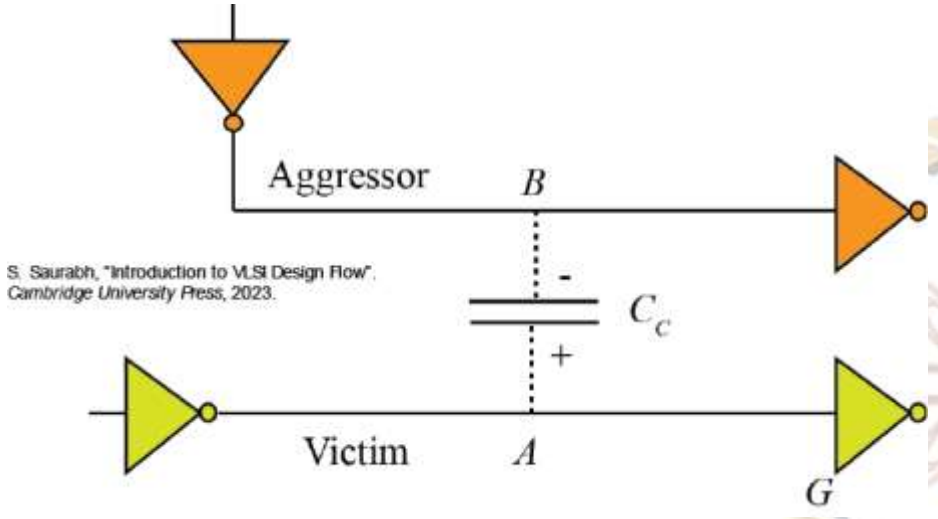
On what factors the magnitude of glitches depend?



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Slew of the aggressor net

- Glitch increases when the aggressor transitions quickly.

Coupling capacitance between the aggressor and the victim net:

- Glitch increases with the increase in the coupling capacitance.

Ground capacitance of the victim net

- Glitch decreases as the ground capacitance of the victim increases.

Strength of the driver of the victim net

- Glitch decreases as the strength of the driver of the victim net increases.

When does Glitches Cause Functional Problems?

- If the magnitude of the glitch is above a threshold, it can propagate to a sequential circuit element.
- Consequently, a wrong value can get latched (0 instead of 1 or 1 instead of 0), leading to a circuit failure.

- If the magnitude of the glitch is above a threshold, on clock/reset/control signal, a spurious transition can get triggered in a sequential element.

- Need to propagate glitches

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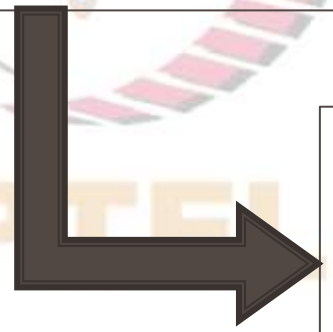
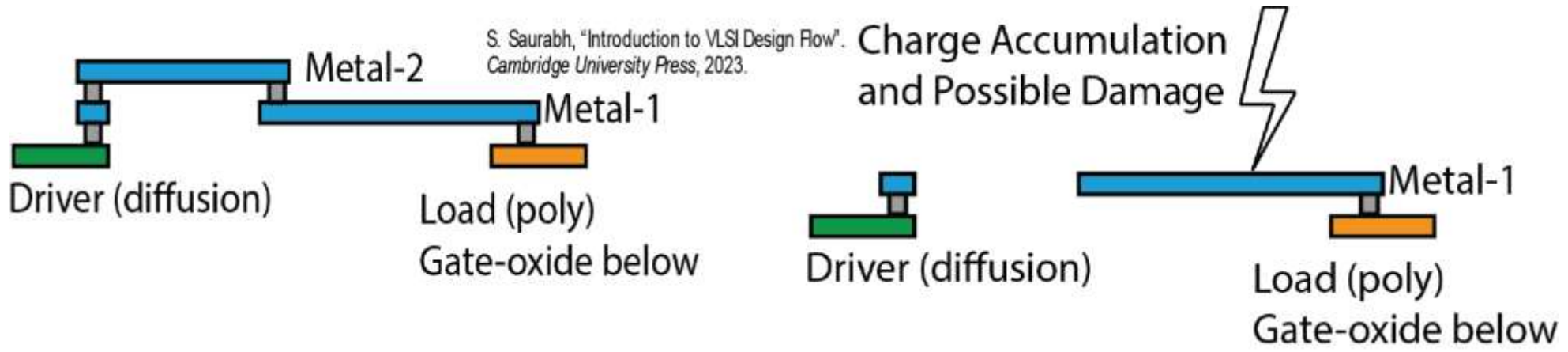
Basic Concepts for Physical Design



Antenna Effect

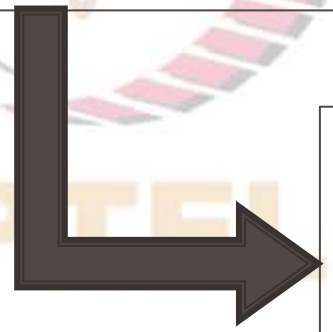
Antenna Effect: Cause



- During fabrication before addition of Metal-2, long Metal-1 connected to the gate can become charged and can destroy the gate

- **Antenna Ratio**: ratio of the conductor area to the gate oxide area
- High Antenna Ratio implies greater chance of damage
  - Antenna Rules defined to allow Antenna Ratio to be within limits
  - Design Goal: Fix Antenna DRC violations by keeping Antenna Ratio small

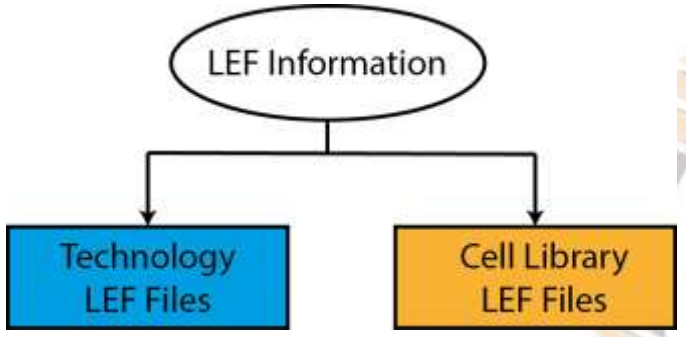
Basic Concepts for Physical Design



Library Exchange Format (LEF)

Library Exchange Format (2)

- LEF file generally divided into two files



Technology LEF files:

- Information about the available layers and vias, their properties.
- Sheet resistance and capacitance per unit square for various layers
- Placement and routing design rules
- Antenna rules

Cell Library LEF files:

- Abstract information of the cell layout relevant to the physical design,
  - Cell boundary, list of pins and their locations, and obstructions to placement and routing.

References

- J. M. Rabaey, A. Chandrakasan, and B. Nikolic. "Digital integrated circuit design: A Design Perspective", *Prentice Hall*, 2nd ed., 2002.
- J. Bhasker and R. Chadha. "Static Timing Analysis for Nanometer Designs: A Practical Approach". *Springer Science & Business Media*, 2009.
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