8. Consider the following synchronous circuit.
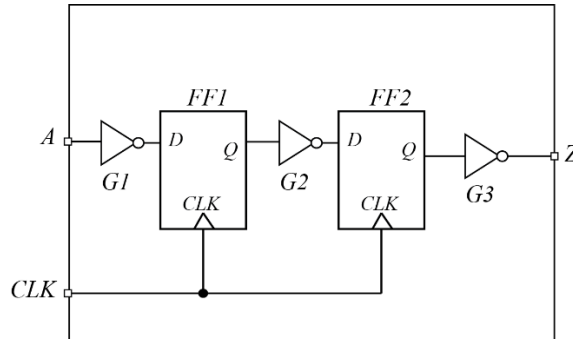
The following attributes are valid for the flip-flops FF1 and FF2: setup time=45 ps, hold time=10 ps, and CLK-to-Q delay=20 ps. The delay of each inverter is 50 ps. Ignore the wire delay.

Assume that we have define the following constraints in the SDC file (all time units are in picoseconds):

> create_clock -name CLK -period 1000 [get_ports CLK]
> set_input_delay -clock [get_clocks CLK] 150 [get_ports A]
> set_output_delay -clock [get_clocks CLK] 125 [get_ports Z]

What is the **setup slack** at the timing end-point FF1/D?
   a.   755 ps
   b.   700 ps
   c.   850 ps
   d.   905 ps

Solution:
   Clock period = 1000 ps [from the command create_clock]
   Arrival time at FF1/D=150 [i.e., from set_input_delay command] + 50 [i.e., delay of inverter G1] = 200 ps
   Required time = Clock period – setup time of FF1 = 1000 – 45 ps = 955 ps
   Setup slack = Required time – Arrival time = 955 -200 = 755 ps

Hence, option (a) 755 ps is correct.

9. For the question above, what is the **hold slack** at the timing end-point FF1/D?
   a.   200 ps
   b.   190 ps
   c.   0 ps
   d.   -190 ps
Solution:
   Arrival time at FF1/D=150 [i.e., from set_input_delay command] + 50 [i.e., delay of inverter G1] = 200 ps
   Required time = hold time of FF1 = 10 ps

Hold slack = Arrival time - Required time = 200-10 = 190 ps

Hence, option (b) 190 ps is correct.

10. For the question above, what is the **setup slack** at the timing end-point port Z?
    a. 800 ps
    b. 900 ps
    c. 805 ps
    d. 905 ps

Solution:

Clock period = 1000 ps [from the command create_clock]

Arrival time at Z = 20 [i.e., CLK-to-Q delay] + 50 [i.e., delay of inverter G3] = 70 ps

Required time at Z = Clock period – output-delay specified at Z = 1000 – 125 ps = 875 ps

Setup slack = Required time – Arrival time = 875 - 70 = 805 ps

Hence, option (c) 805 ps is correct.