VLSI Design Flow: RTL To GDS (NPTEL Course)

Lab Tutorial 10

Objective: To install OpenROAD tool.

OpenROAD: OpenROAD is an integrated chip physical design tool that takes a design from synthesized Verilog netlist to routed layout.

1. **Yosys:** for performing Logic Synthesis.

2. Floorplanning through Detailed Routing: using **OpenROAD**.

References:

1. Ajayi, Tutu, Vidya A. Chhabria, Mateus Fogaça, Soheil Hashemi, Abdelrahman Hosny, Andrew B. Kahng, Minsoo Kim et al. "Toward an open-source digital flow: First learnings from the openroad project." In Proceedings of the 56th Annual Design Automation Conference 2019, pp. 1-4. 2019.
2. Ajayi, Tutu, and David Blaauw. "OpenROAD: Toward a self-driving, open-source digital layout implementation tool chain." In Proceedings of Government Microcircuit Applications and Critical Technology Conference. 2019.

Website:

https://theopenroadproject.org/

OpenRoad Community:

https://gitter.im/The-OpenROAD-Project/community

Build OpenROAD locally in your machine:

1. Download repository

```
$ git clone --recursive https://github.com/The-OpenROAD-Project/OpenROAD.git
$ cd OpenROAD
```

2. Install dependencies

```
$ sudo ./etc/DependencyInstaller.sh
```

3. Build

```
$ mkdir build
$ cd build
$ cmake
$ make
$ sudo make install
```

4. Run tool

```
$ openroad
```