VLSI DESIGN FLOW: RTL TO GDS

Lecture 35
Basic Concepts for Physical Design - I

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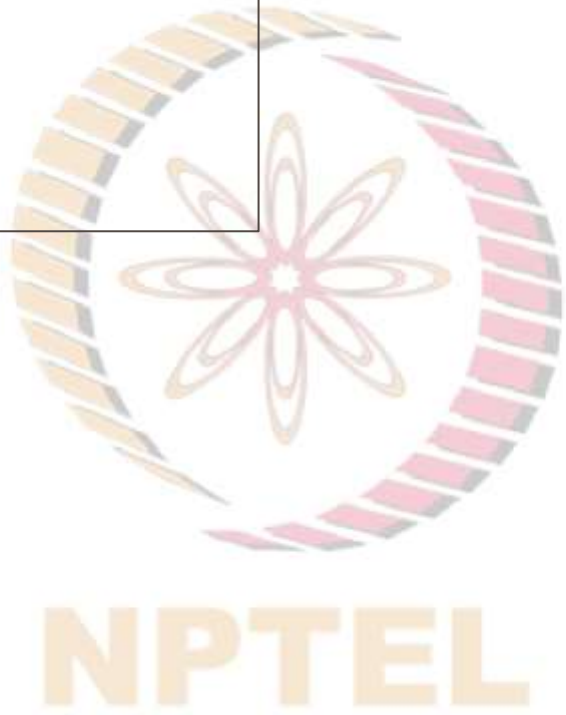
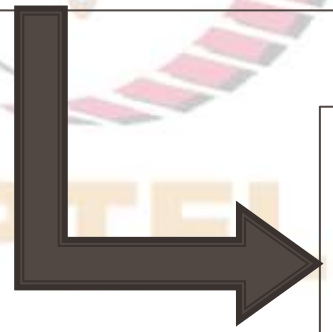
Lecture Plan

- Fabrication of IC
- Interconnects
- Parasitics in Interconnects



Physical Concepts for Physical Design



IC Fabrication

IC Fabrication

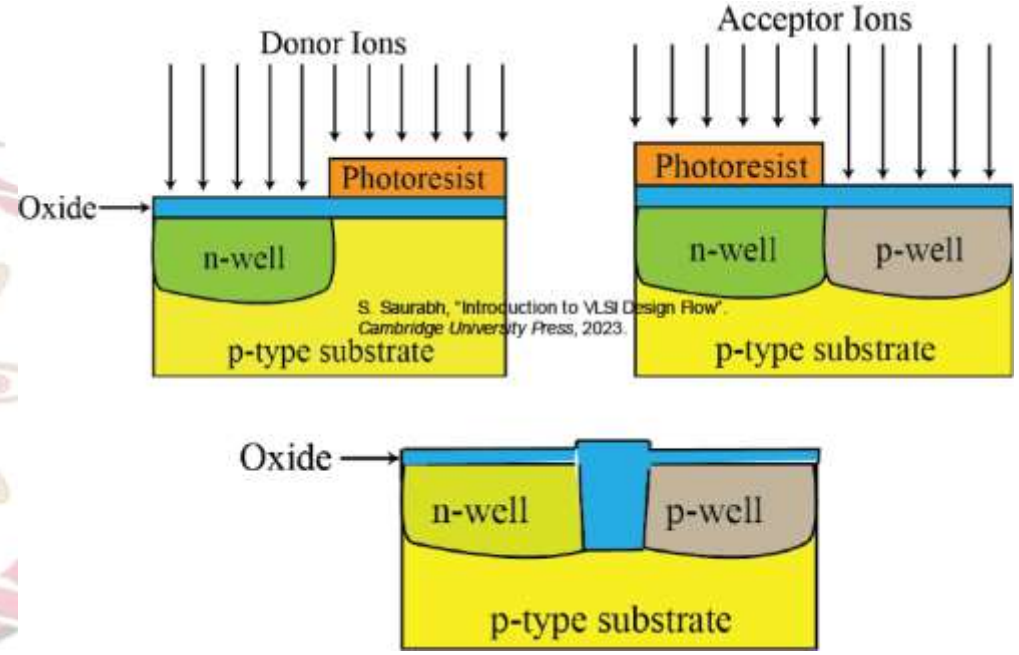
- Photolithography is the key step in fabrication

Two phases:

1. Front End Of the Line (FEOL) processes: active elements (transistors, diodes, capacitors)
2. Back End Of the Line (BEOL) processes: layers of wires

FEOL Processes (1)

- Doping with acceptor and donor atoms
- **Ion Implantation:**
  - ➢ Appropriate ions created, using arc discharge
    - accelerated/filtered using electric and magnetic fields
  - ➢ Bombard the substrate through a thin layer of screening silicon dioxide
- Annealing: activate dopants
- Threshold voltage adjustment implants



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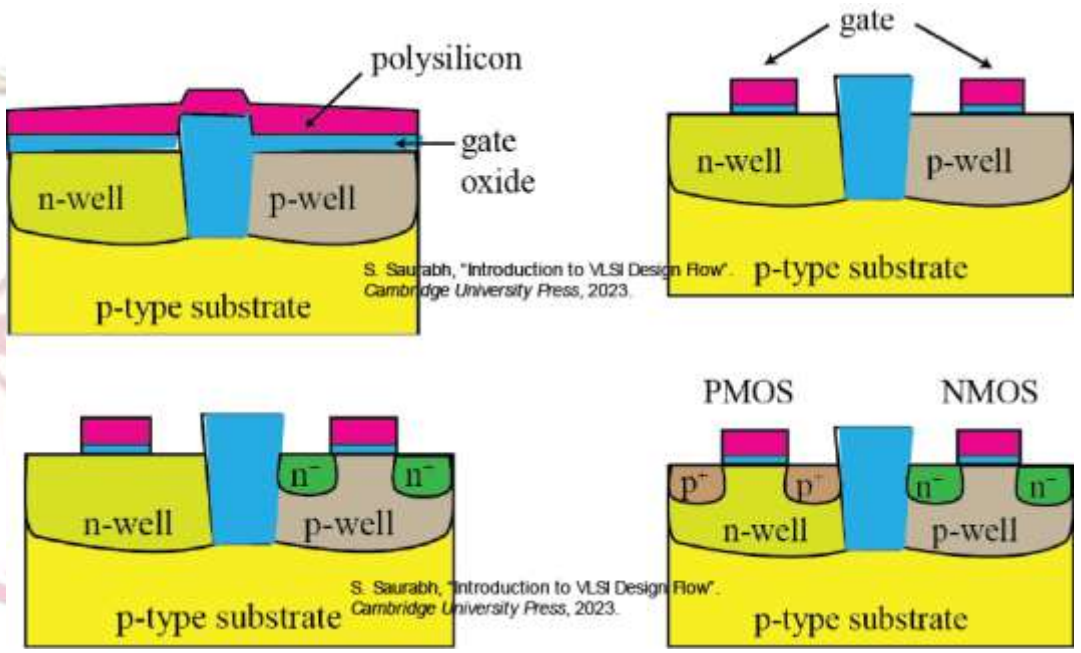
- **Isolation**: ensures that the transistors do not interact through the substrate
- Shallow Trench Isolation (STI)

FEOL Processes (2)

Transistor formation (gate, source and drain)

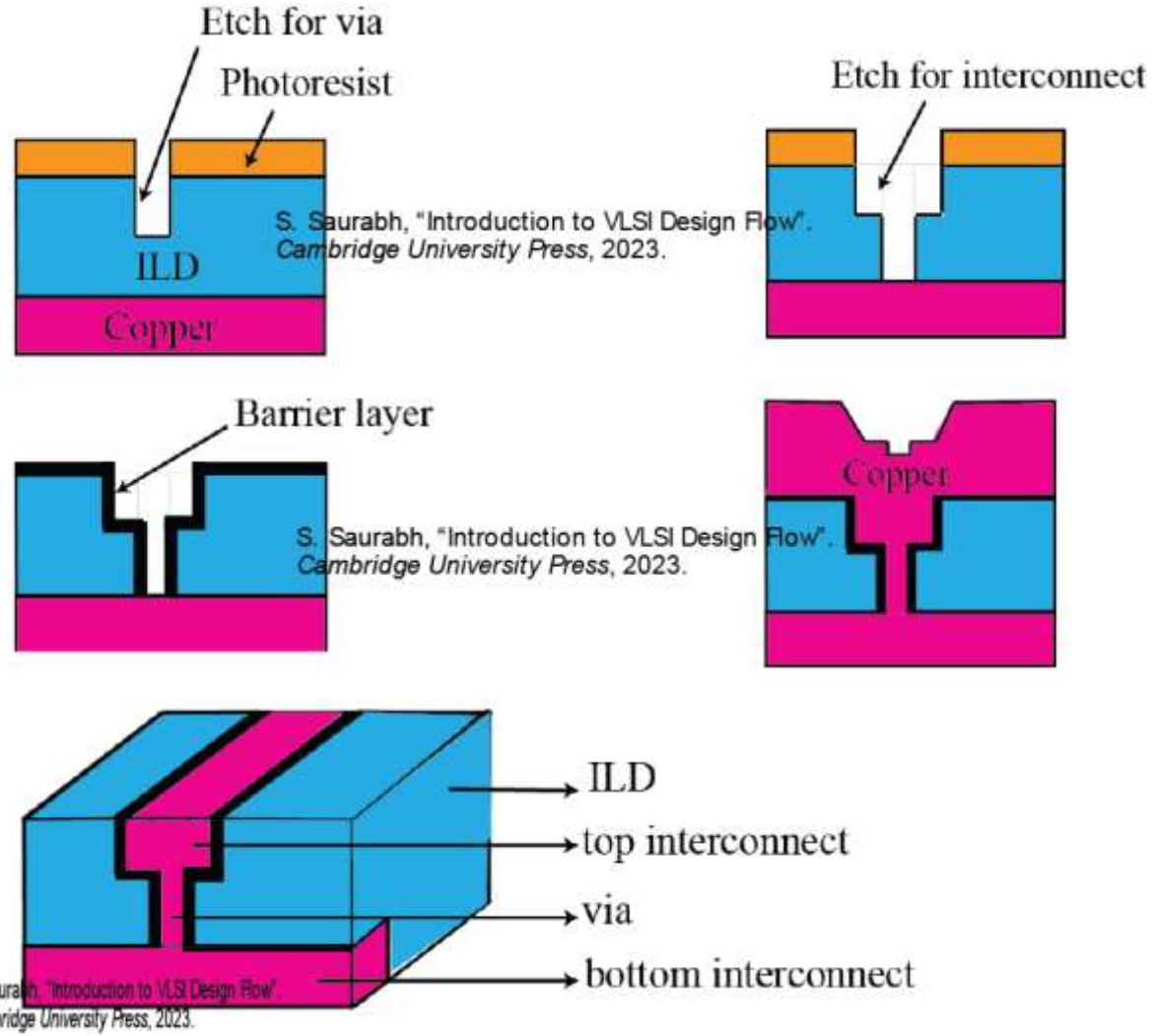
- High quality gate oxide growth/deposition over silicon channel
- Polysilicon deposition for gate contact
  - ➢ Chemical vapor deposition (CVD)
- Patterning
  - ➢ Local interconnect
- Source-drain Ion Implantation and annealing for NMOS and PMOS



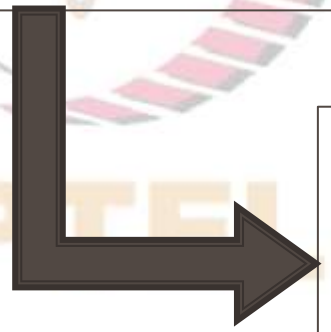
BEOL Processes (1)

Back End Of the Line (BEOL):

- Layers of Wires
- Inter Layer Dielectric (ILD)
- Copper
  - ➢ Dual Damascene Process
  - ➢ Repeated for each layer



Physical Concepts for Physical Design



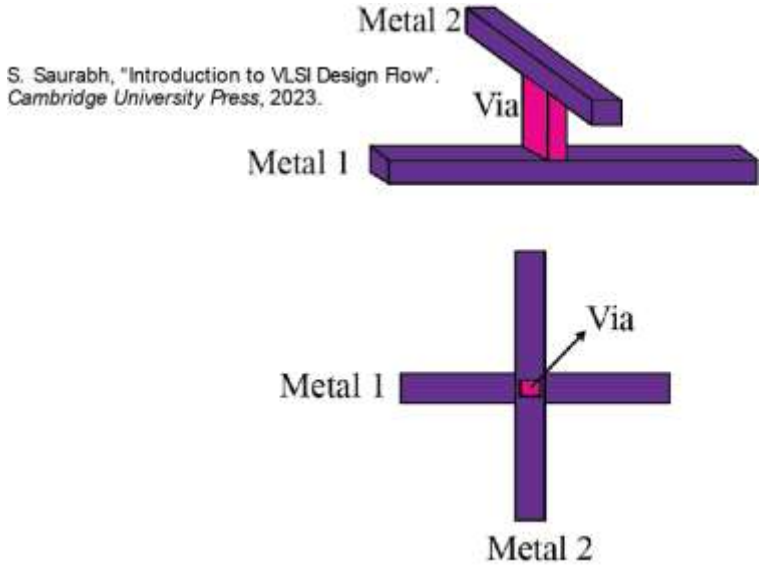
Interconnects/Wires

Interconnect Layers (1)

Metal Layers Two Types:

- **Wiring layers:** metal layers making interconnection
  - Parallel to wafer surface
- **Via Layers:** connects wiring layers
  - Perpendicular to wafer surface

- Interconnects have uniform thickness (height)
  - Can be represented as 2D polygons
- Shapes of wires in the layout decide where metal needs to be deposited during fabrication



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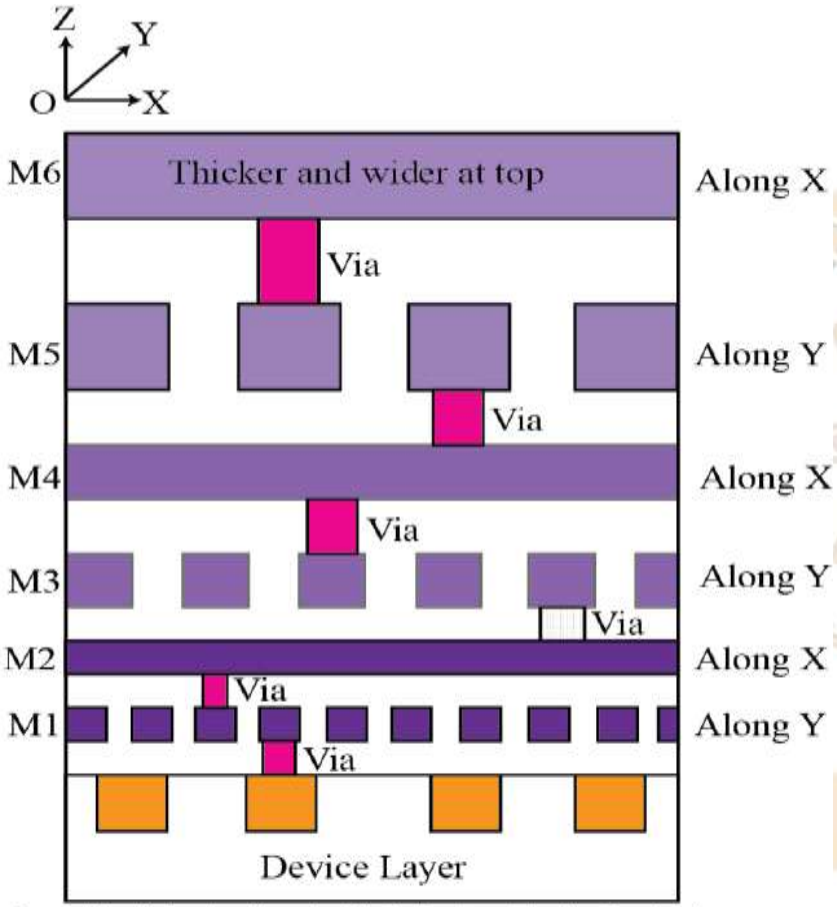
Interconnect Layers (2)



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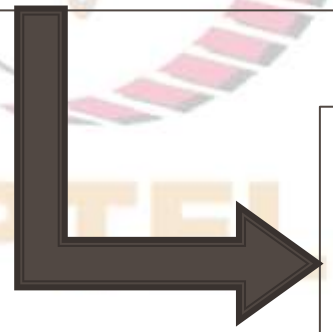
J. Ao, S. Dong, S. Chen, and S. Goto. "Delay-driven layer assignment in global routing under multitier interconnect structure." *Proceedings of the 2013 ACM International Symposium on Physical Design* (2013), pp. 101–107.

- High performance IC can use 15 metal layers
- Metal Layers are separated by dielectrics : generally SiO_2
  - ➢ Low-k material can also be used

- Height of wiring layers can be different in different layers
- In general: metal height increases from the bottom to the top of an IC

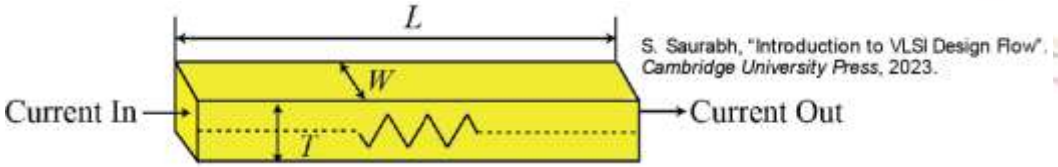
- Each wiring layer has a preferred direction: vertical or horizontal
- Each successive wiring layers alternate between vertical and horizontal direction
  - ➢ Can lead to increase in via count

Basic Concepts for Physical Design



Interconnect Parasitics

Interconnect: Resistance



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- Resistance:

$$R = \rho \frac{L}{TW}$$

- $R = R_S \frac{L}{W}$ where $R_S = \frac{\rho}{T}$ is called the sheet resistance
- Sheet resistance is defined in the library

- At high frequency, the resistance of an interconnect tends to increase
  - **Skin effect**: current tends to flow primarily on the conductor's surface
  - Important for wider and thicker wires at the top metal layers (clock lines that work at high frequency)

Interconnect: Capacitance

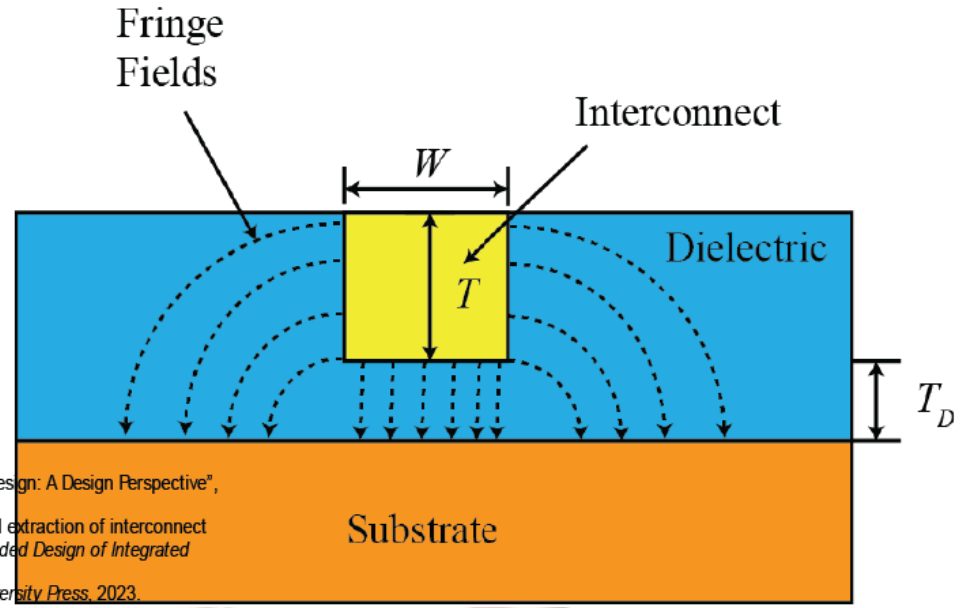
Origin of interconnect Capacitance:

- Interconnects lie within a dielectric material
- Electric potential of interconnects changes during circuit operation
  - Electric field and the stored charges in the surrounding dielectric material change.
  - Consequently, an interconnect exhibits substantial capacitance

Factors influencing Interconnect Capacitance:

- Depends on their geometry, environment (the location and geometry of other interconnects), and the property of the surrounding dielectric.
- The computation of interconnect capacitance is a nontrivial problem.

Interconnect: Capacitance of Strip



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Two Components:

1. **Parallel plate component:** $C_{pp} = \frac{\epsilon_d \epsilon_0}{T_D} WL$
2. **Fringe component:** field lines that emanate from the sidewalls

- Both these components can be added together
- With technology advancement, fringe capacitance is increasing

Multiple Interconnects: Capacitance

J. M. Rabaey, A. Chandrakasan, and B. Nikolic. "Digital integrated circuit design: A Design Perspective". *Prentice Hall*, 2nd ed., 2002.
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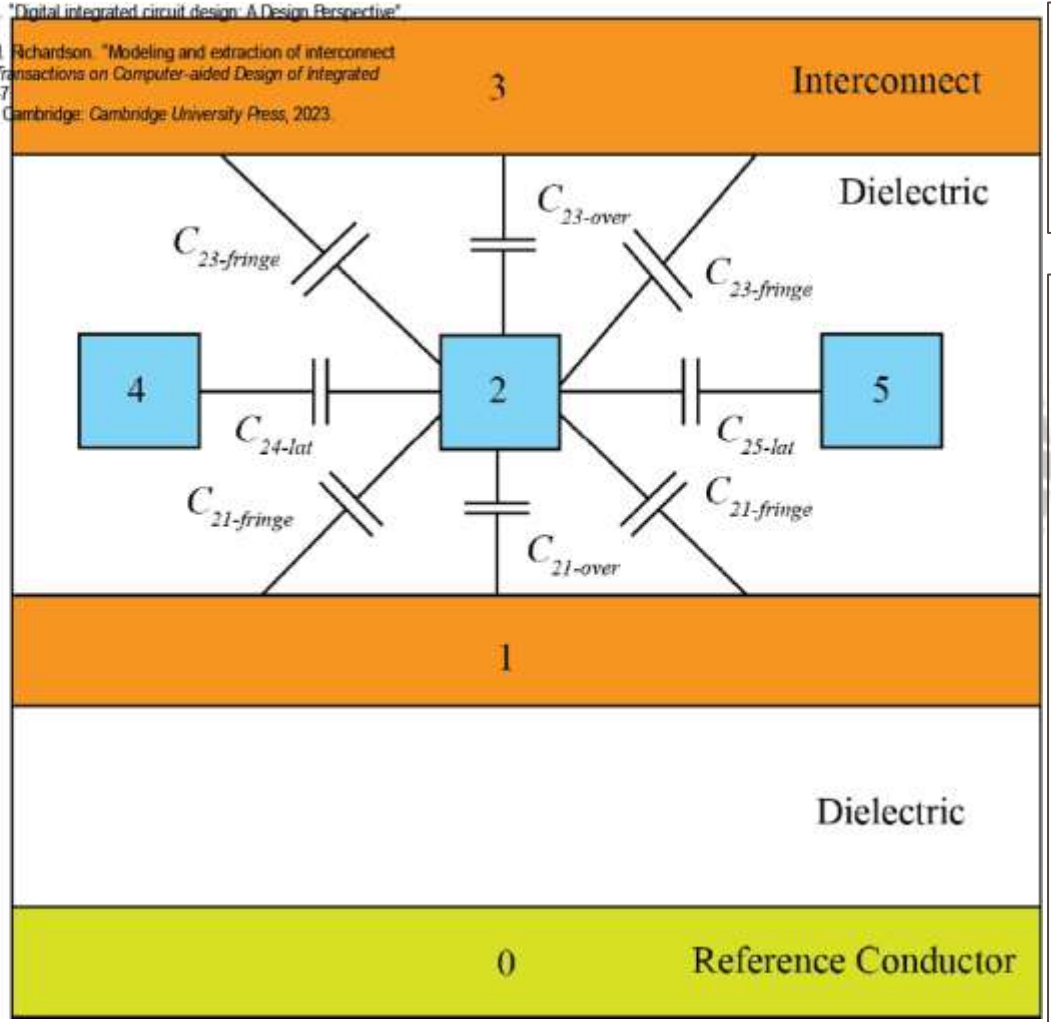

- Electric field lines emanating from an interconnect are modified by the neighboring interconnects in a complicated manner

Three major components of capacitance:

1. **Overlap capacitance**: due to the overlap between two conductors in different planes.
2. **Lateral capacitance**: formed by two parallel edges of nonoverlapping conductors in the same plane.
3. **Fringe capacitance**: between two conductors in different planes due to electric fields originating from the sidewalls

References

- J. M. Rabaey, A. Chandrakasan, and B. Nikolic. "Digital integrated circuit design: A Design Perspective", *Prentice Hall*, 2nd ed., 2002.
- N. D. Arora, K. V. Raol, R. Schumann, and L. M. Richardson. "Modeling and extraction of interconnect capacitances for multilayer VLSI circuits." *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems* 15, no. 1 (1996), pp. 58–67.
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