VLSI DESIGN FLOW: RTL TO GDS

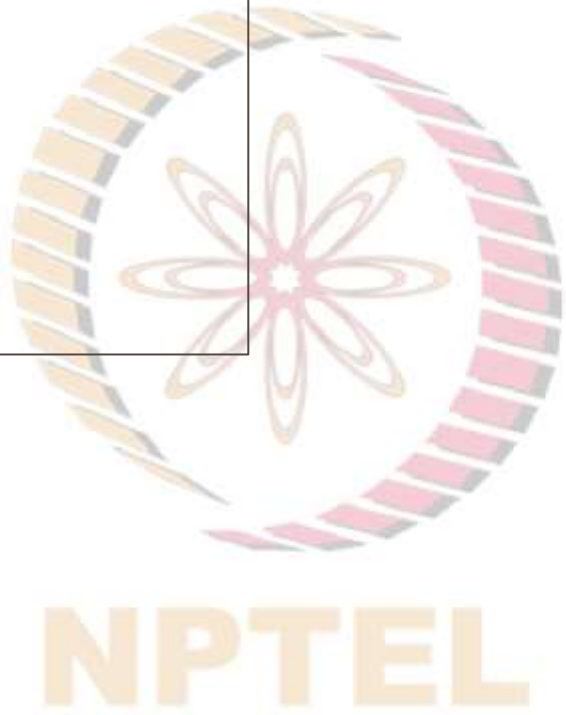
Lecture 1
Basic Concepts of Integrated Circuit: I

Sneh Saurabh
Electronics and Communications Engineering
IIIT Delhi

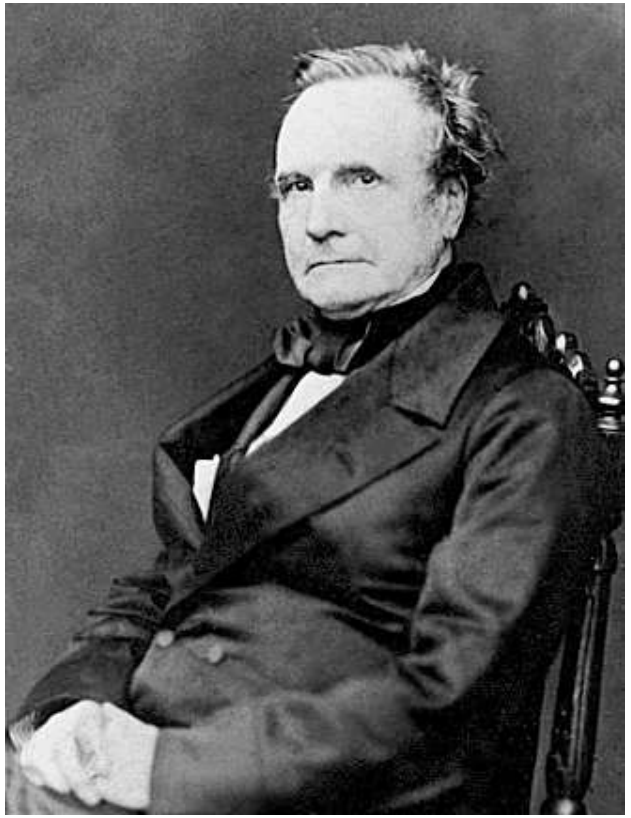
Lecture Plan

Basic Concepts of Integrated Circuit

- Historical Perspective
- Structure
- Fabrication
- Designing vs. Fabrication



Art of Copying …



Source: https://commons.wikimedia.org/wiki/File:Charles_Babbage_-_1860.jpg, See page for author, Public domain, via Wikimedia Commons

Charles Babbage, *On the Economy of Machinery and Manufactures*, Chapter 11, 1832

"…**sources of excellence** in the work produced by **machinery** depend on a principle…., and is one upon which the **cheapness** of the articles produced seems greatly to depend.

The principle alluded to is that of **COPYING**, taken in its most extensive sense."

VLSI: An Historical Perspective

VLSI: An Historical Perspective

Electronic Circuit:

- Various active and passive components
  - Connecting discrete components become expensive, time-consuming, and unreliable.

Integrated Circuit:

- Monolithic silicon chips containing several components
  - IC Technology

IC Technology:

- Several key inventions and discoveries
  - Photolithography

Increasing Integration:

- Small-Scale Integration, Large-Scale Integration, Very Large-Scale Integration

Moore's Prediction:

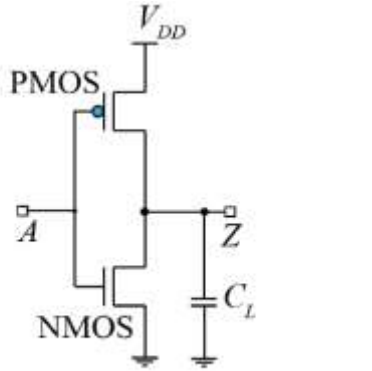
- Number of components in an IC realized at *minimum cost* will double every year
  - Later revised to double every two year

Shrinking Transistors:

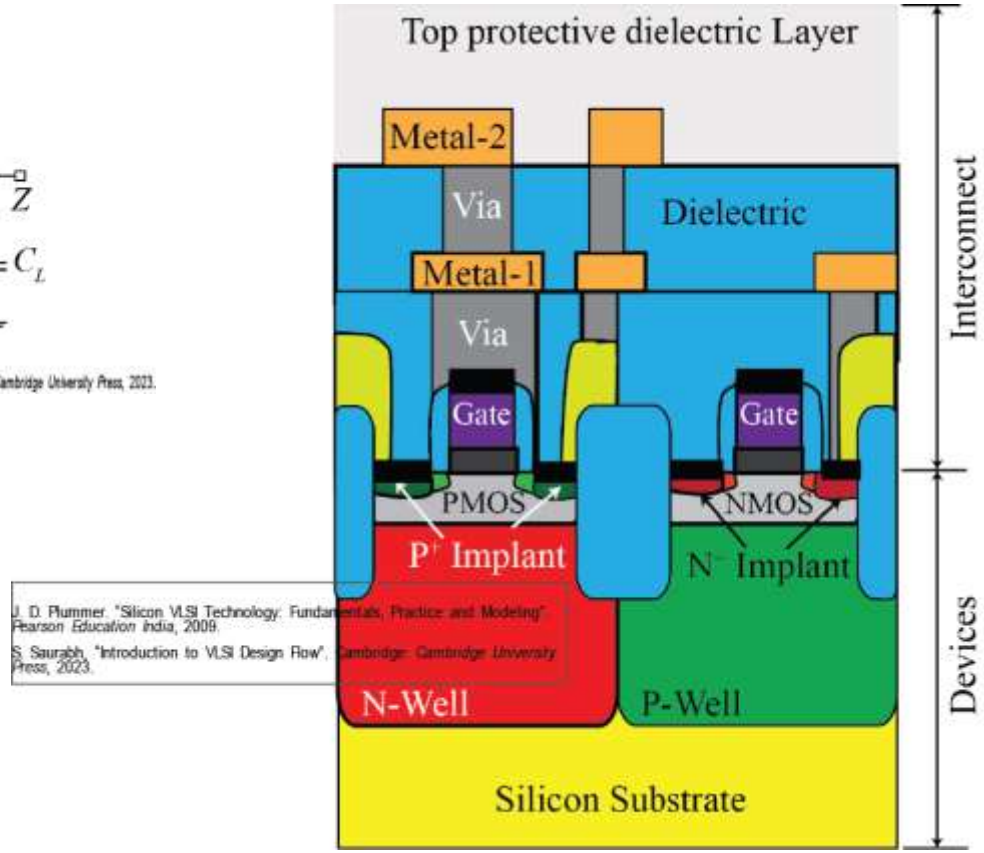
- Moore's prediction enabled by the shrinking sizes of transistors
  - 90 nm, 65 nm, 45 nm, 32 nm, 22 nm, 16 nm ….
- Improving the speed, energy efficiency and cost per transistor
- Designing an IC becomes more complicated

Structure of an Integrated Circuit

Structure of Integrated Circuit (1)



S. Saurabh, "Introduction to VLSI Design Flow", Cambridge: Cambridge University Press, 2023.



J. D. Plummer, "Silicon VLSI Technology: Fundamentals, Practice and Modeling", Pearson Education India, 2009.

S. Saurabh, "Introduction to VLSI Design Flow", Cambridge: Cambridge University Press, 2023.

- ICs are composed of multiple layers
- Diffusion layer, implant layer, metal layer etc.

- Bottom: devices
- Above devices: interconnect layers of metal separated by insulator
  - Can be more than 10 such metal layers
  - Via is used to make electrical connection between different layers

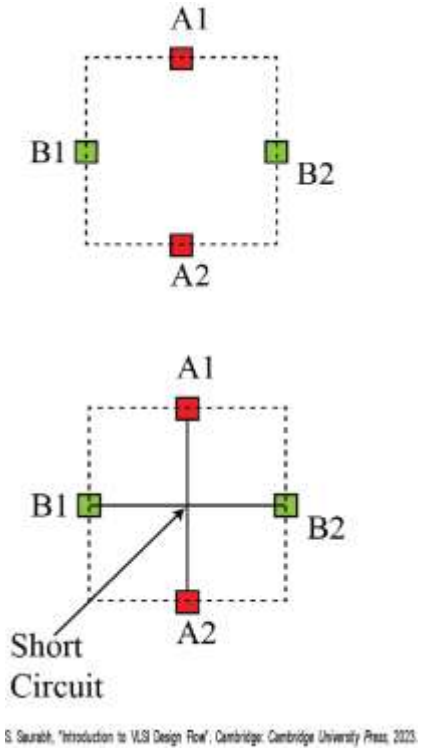
Structure of Integrated Circuit (2)

Problem:

Connect points A1 to A2 and B1 to B2 using wires.

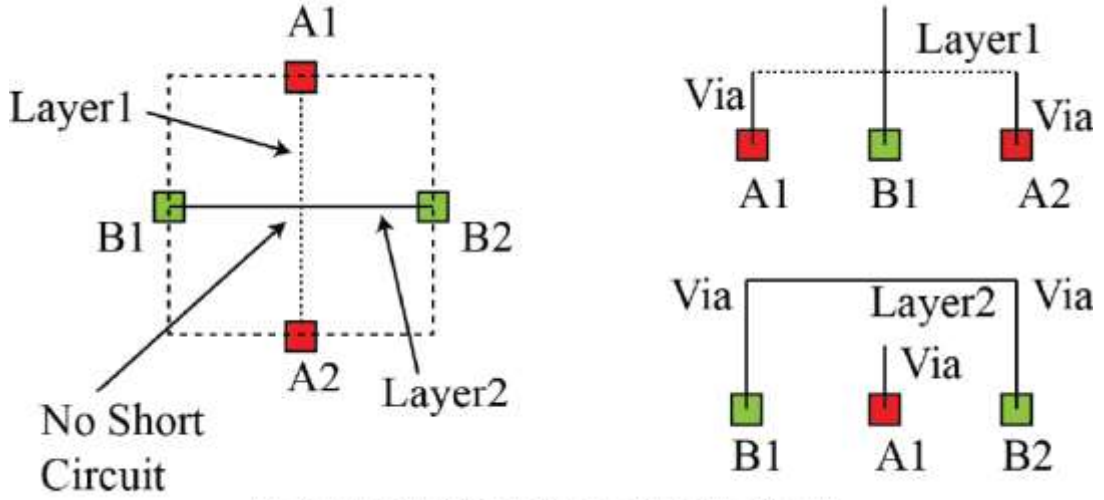
- Wires cannot go outside the rectangle shown.
- The wires are constrained to be in the plane containing A1, A2, B1, B2.

What happens when the constraint of wires being in the same plane is removed?



S. Saurabh, "Introduction to VLSI Design Flow", Cambridge: Cambridge University Press, 2023.

Structure of Integrated Circuit (3)



S. Saurabh, "Introduction to VLSI Design Flow". Cambridge: Cambridge University Press, 2023.

- Multiple layers are necessary to make connections between devices that would otherwise short when connected in a single layer
- Layers defined by mask and fabricated using photolithography

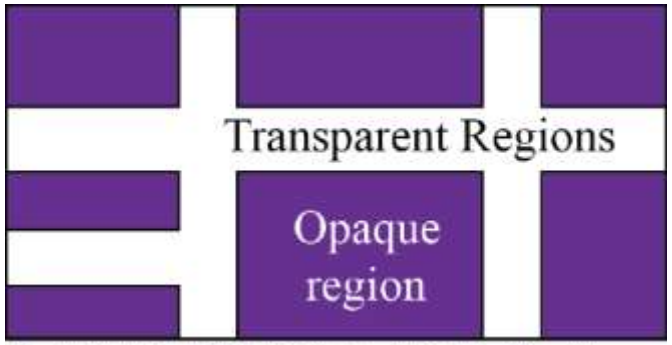
Photolithography

Photolithography (1)

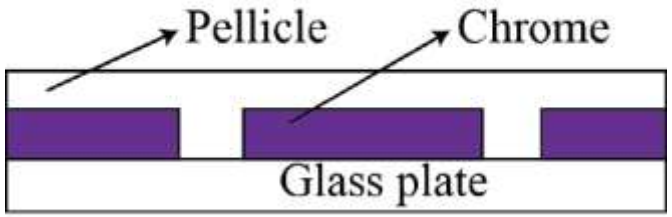
- Process of transferring geometric shapes that are defined on a *mask* to the surface of a silicon wafer

- Features marked on a glass plate with opaque chrome thin films
  - ➢ Also known as photomasks or reticles.

- For different layers of integrated circuits different masks are used
- Photolithography is carried out for each layer

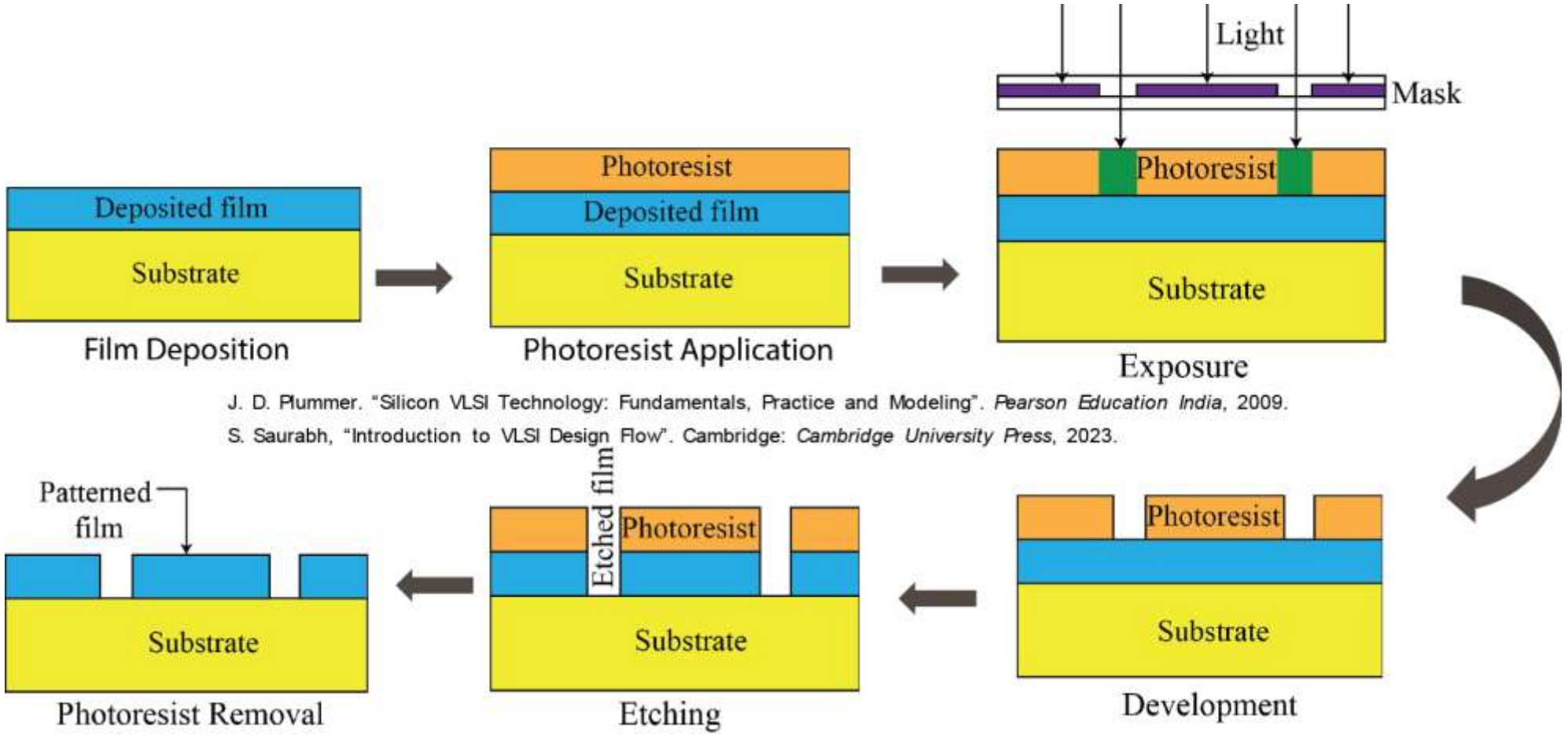


S. Saurabh, "Introduction to VLSI Design Flow". Cambridge: Cambridge University Press, 2023.



S. Saurabh, "Introduction to VLSI Design Flow". Cambridge: Cambridge University Press, 2023.

Photolithography (2)

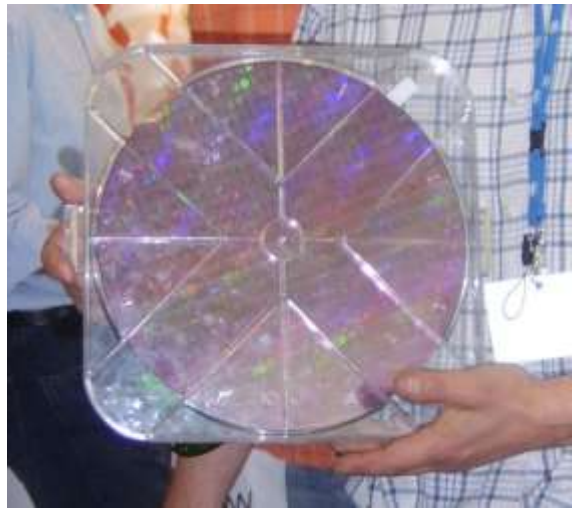


J. D. Plummer. "Silicon VLSI Technology: Fundamentals, Practice and Modeling". *Pearson Education India*, 2009.

S. Saurabh, "Introduction to VLSI Design Flow". Cambridge: *Cambridge University Press*, 2023.

Terminologies related to IC Fabrication

Silicon Wafer and Ingots



Source: https://commons.wikimedia.org/wiki/File:ICC_2008_Poland_Silicon_Wafer_1_edit.png FxJ, Public domain, via Wikimedia Commons

Silicon Wafer:

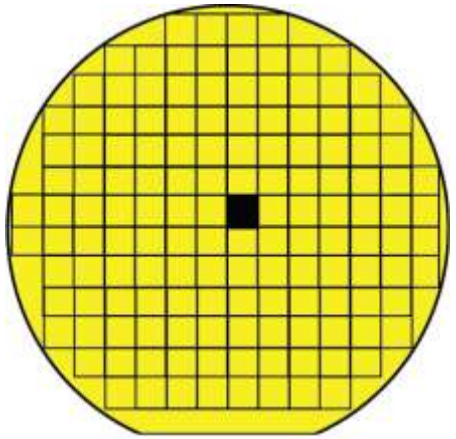
- A silicon wafer is a thin slice of silicon that serves as a substrate for an integrated circuit
- Currently, $300\ mm$ wafer are widely used

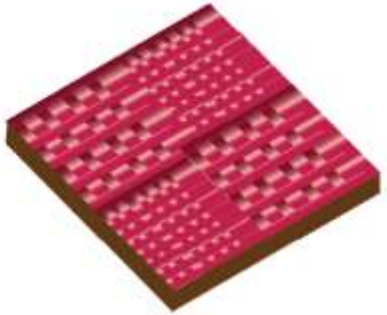
Silicon Ingots:

- Massive cylindrical single crystal of silicon
- Silicon ingots are mostly prepared using Czochralski (CZ) process
  - Pure seed crystal is pulled out from a highly pure melted silicon at 1425°C
- A **silicon wafer** is sliced out from ***silicon ingots***

Source: https://commons.wikimedia.org/wiki/File:Monokristalines_Silizium_f%C3%BCr_die_Waferherstellung.jpg, German Wikipedia, original upload 7. Okt 2004 by Stahlkocher

Dies and Chips





S. Saurabh, "Introduction to VLSI Design Flow". Cambridge: Cambridge University Press, 2023.

Dies:

- Slices of silicon wafer containing the complete circuit are called *dies*
- Hundreds of rectangular shaped integrated circuits are fabricated on a single silicon wafer

- Dies are sliced out from silicon wafers after fabrication and testing

Chips:

- After dies are sliced, they are encapsulated into a supporting case for protection against physical and chemical damage.
- Packaged dies are generally known as *chips*

Designing vs. Fabrication

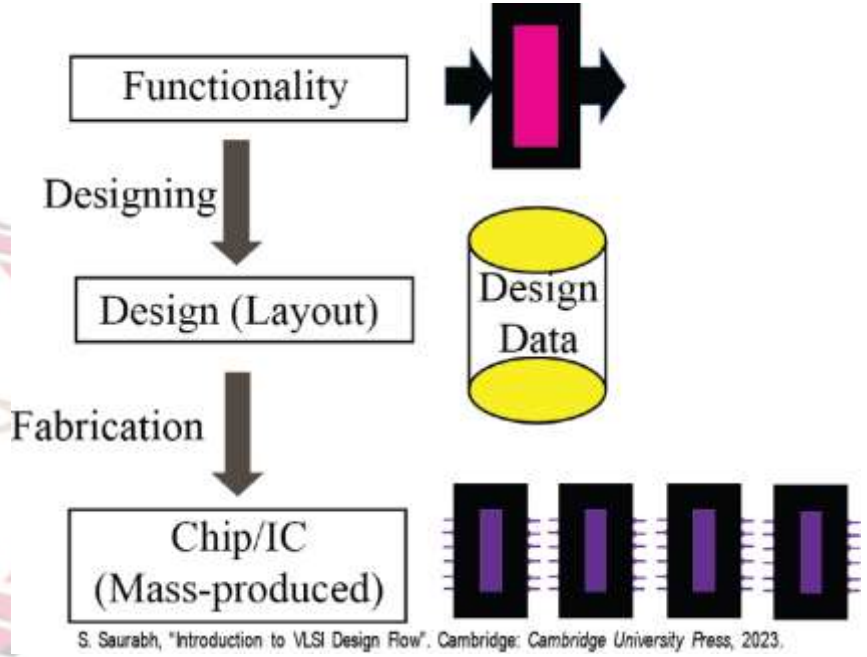
Designing vs. Fabrication

Designing:

- Determining the parameters and composition of a circuit that can achieve the desired functionality

Fabrication:

- It involves actual creation of integrated circuit for a given design (layout of various layers)



S. Saurabh, "Introduction to VLSI Design Flow", Cambridge: *Cambridge University Press*, 2023.

Semiconductor Foundries

Foundry:

- Semiconductor manufacturing plant where the fabrication of integrated circuits is done.
- Cost of setting-up and maintaining is very high.
- Sustainable only when the **facilities of foundry are utilized close to their full potential**

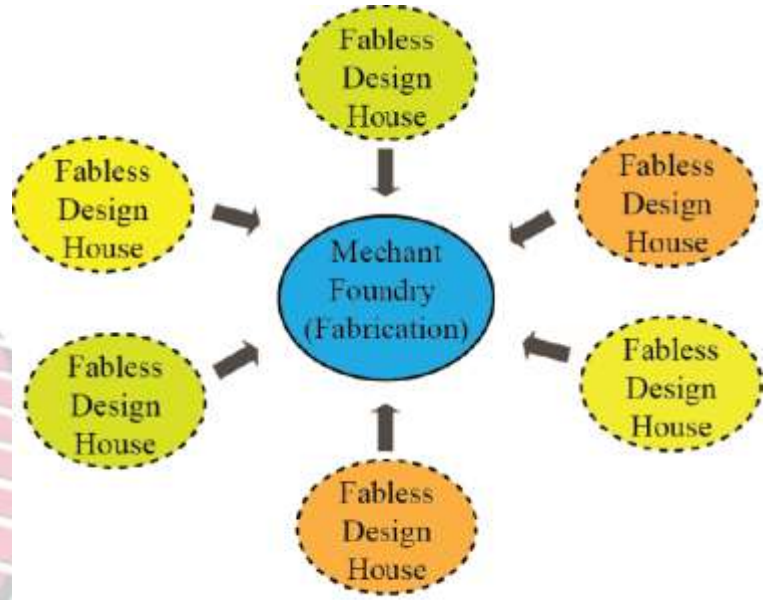
Semiconductor Industry: Business Model

Fabless Design Companies:

- Only designing, fabrication is outsourced
- Do not require to setup and maintain costly foundries.
- Example: Qualcomm, Nvidia, etc.

Merchant Foundries:

- Only fabrication (for others)
- Draws business from many companies and utilize foundry to full potential .
- Example: TSMC, UMC, GF, etc.



S. Saurabh, "Introduction to VLSI Design Flow". Cambridge: *Cambridge University Press*, 2023.

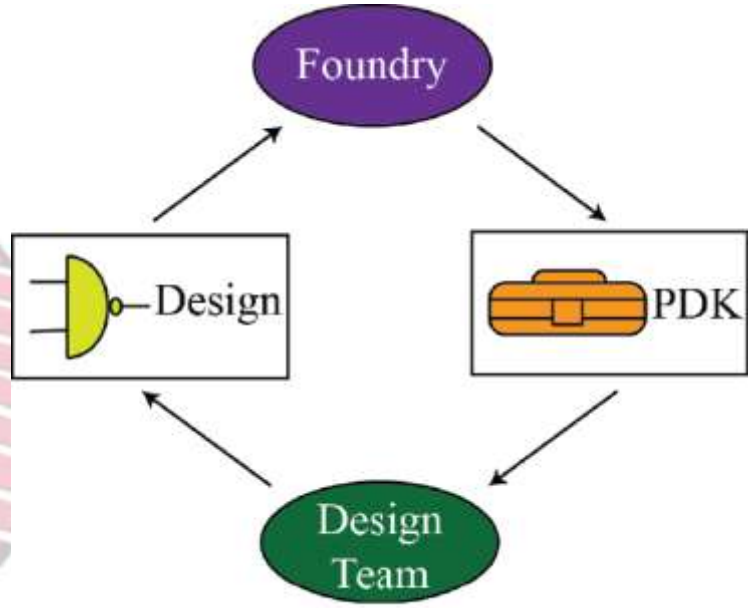
Integrated Device Manufacturers:

- Both designing and fabrication done in the same company
- Production is more efficient and cost-effective due to control over all the steps of the process.
- Example: Intel, Samsung

Sharing Information between Design and Fabrication

Design and Fabrication:

- Related Task
- Share Information:
  - Process Design Kit (PDK)
  - Design (Layout)



S. Saurabh, "Introduction to VLSI Design Flow", Cambridge: *Cambridge University Press*, 2023.

References

- J. D. Plummer. "Silicon VLSI Technology: Fundamentals, Practice and Modeling". *Pearson Education India*, 2009.
- S. Saurabh, "Introduction to VLSI Design Flow". Cambridge: *Cambridge University Press*, 2023.