VLSI DESIGN FLOW: RTL TO GDS

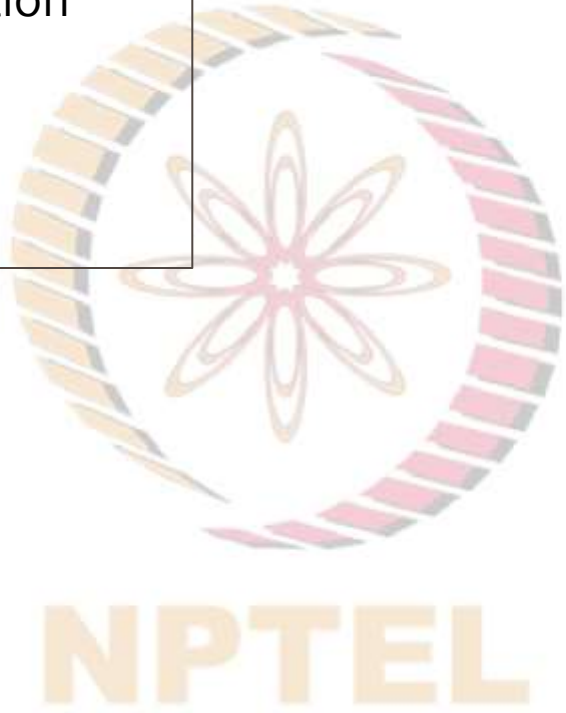
Lecture 29
Power Analysis

Sneh Saurabh
Electronics and Communications Engineering
IIIT Delhi

Lecture Plan

Power Analysis:

- Components of Power Dissipation
- Power Models in Library
- Estimating Power Dissipation

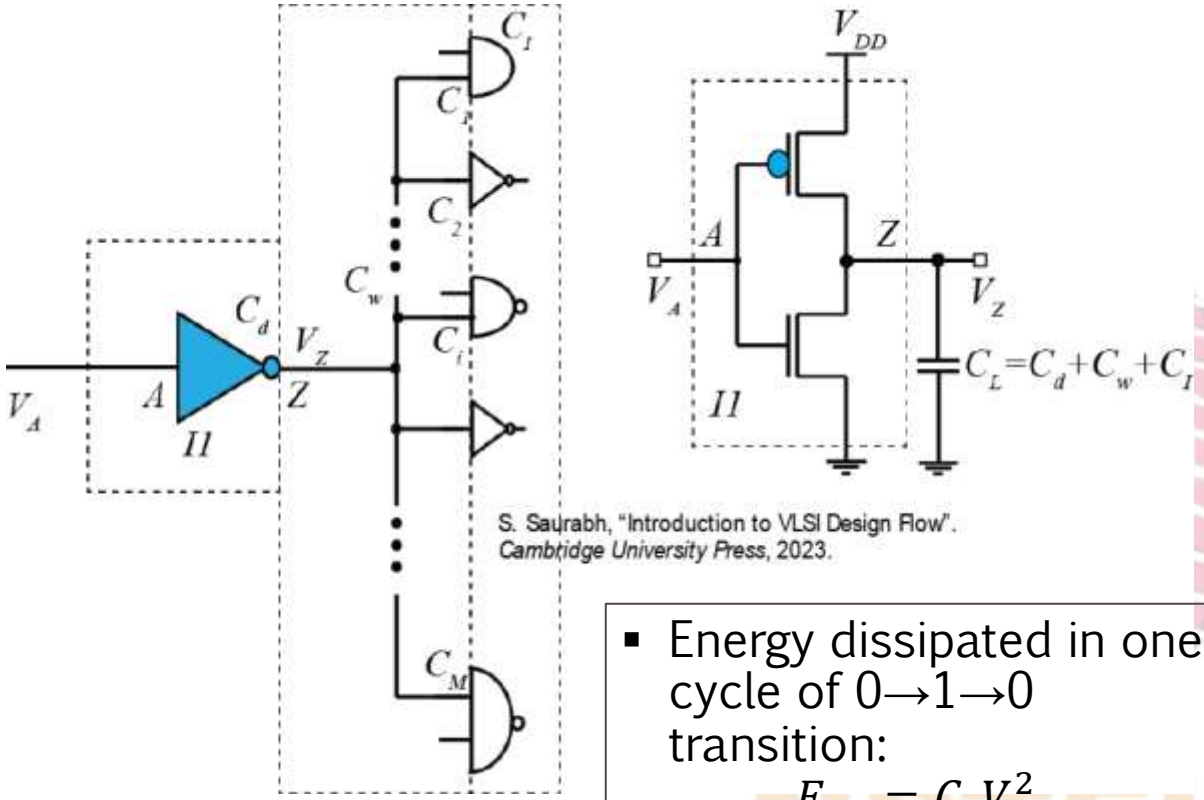


Components of Power Dissipation

Power dissipation is broadly of two types:

1. Dynamic Power Dissipation:
   - Occurs when a circuit performs computation actively
2. Static Power Dissipation:
   - When the circuit is powered on (supply voltages are applied), but it does not perform active computation

Dynamic Power Dissipation: Switching Power



S. Saurabh, "Introduction to VLSI Design Flow". *Cambridge University Press*, 2023.

- Energy dissipated in one cycle of 0→1→0 transition:

$$E_{sw} = C_L V_{DD}^2$$

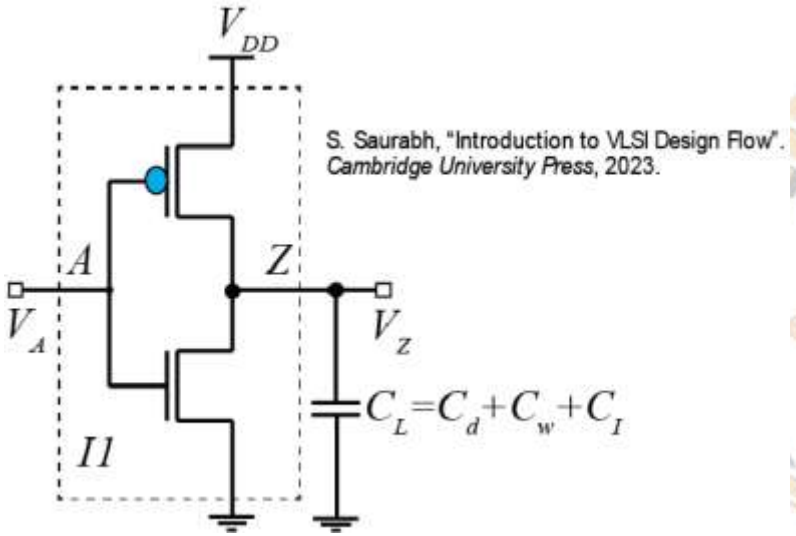
Switching power dissipated in a synchronous circuit:

$$P_{sw} = C_L V_{DD}^2 \alpha f_{clk}$$

where,

- f_{clk} =frequency of the clock in the circuit
- α =activity of the signal
  - define α = 1 when the output completes one cycle of transition (1→0→1) in one clock period

Dynamic Power Dissipation: Short circuit Power



S. Saurabh, "Introduction to VLSI Design Flow". *Cambridge University Press*, 2023.

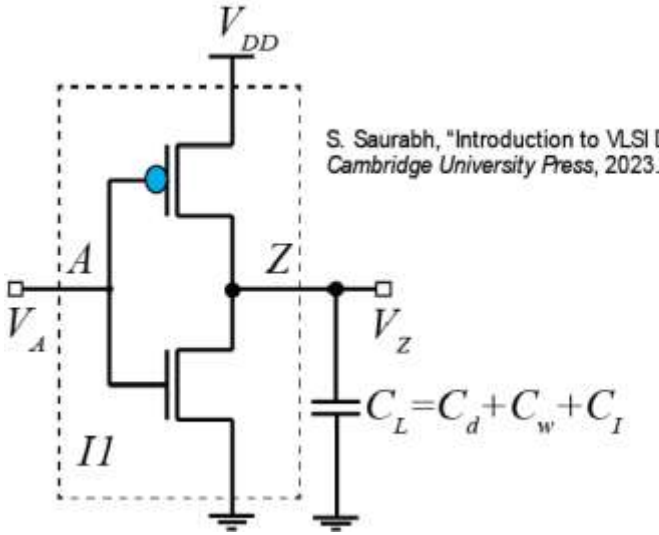
- Short circuit power dissipation:

$$P_{sc} = V_{DD} I_{SC}$$

- Power dissipated when short circuit condition occur:

$$P_{dyn} = P_{sw} + P_{sc}$$

Static Power Dissipation



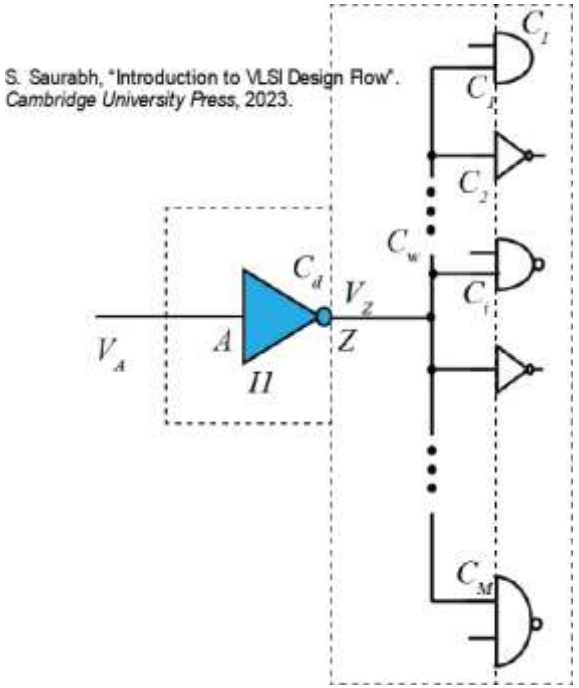
S. Saurabh, "Introduction to VLSI Design Flow". *Cambridge University Press*, 2023.

- Static power dissipation occurs because of:
  - Subthreshold current
  - Gate Leakage
  - Junction Leakage
- $P_{stat} = V_{DD} I_{leak}$

Total power dissipation in a circuit:

$$P_{tot} = P_{dyn} + P_{stat}$$

Technology Library Models: Dynamic Power



Energy dissipated in one cycle of 0→1→0 transition:

$$E_{dyn} = C_L V_{DD}^2 + V_{DD} I_{SC} \tau_{SC}$$

$$E_{dyn} = (C_d + C_w + C_I) V_{DD}^2 + V_{DD} I_{SC} \tau_{SC}$$

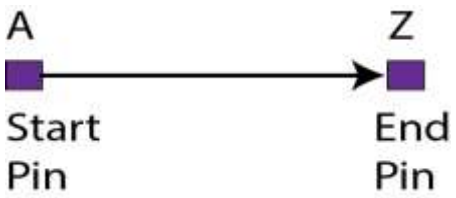
We can write:

$$E_{dyn} = C_d V_{DD}^2 + V_{DD} I_{SC} \tau_{SC} + (C_w + C_I) V_{DD}^2 = E_{int} + E_{ext}$$

- Energy dissipated inside a cell E_{int} is the property of the cell and modelled in the library
- Energy dissipated outside a cell E_{ext} depends on the environment (external load)
  - Tools can compute it after $(C_w + C_I)$ is known
- Power can be estimated using energy per transition by multiplying with activity and clock frequency

Non-linear Power Model (NLPM)

- Internal power dissipation depends on the output-load and input slew
- Modelled as two-dimensional table named **internal_power**
  - ➢ Referred to as Non-linear Power Model (NLPM)



- Rise and fall power can be represented as different arcs

- Values represent energy dissipated per transition

```
u_table_template(index_1) {
        variable_1 : input_net_transition ;
        variable_2 : total_output_net_capacitance ;
        index_1( "10, 20, 30" ) ;
        index_2( "1.2, 5.0,15.0, 37.5) ;
}
....
pin(Z) {
        internal_power()              {
                related_pin           : “A" ;
                rise_power(index_1) {
                   values( "4, 5, 7, 12,   ...3x4 table);
                }
                ...
        }
}
```

S. Saurabh, “Introduction to VLSI Design Flow”.*Cambridge University Press*, 2023.

Technology Library Models: Static Power

- Static power dissipated inside a CMOS logic gate depends on the value (0 or 1) at its input pin
- Modeled using **when** condition in the library

```
cell (NAND2) {  ...
        cell_leakage_power : 125;
        leakage_power () {
                when : "!A & !B"; value : 20; }
        leakage_power () {
                when : "A & !B"; value : 150; }
        leakage_power () {
                when : "!A & B"; value : 200; }
        leakage_power () {
                when : "A & B"; value : 300; }  ...
```

S. Saurabh, "Introduction to VLSI Design Flow". *Cambridge University Press*, 2023.

Estimating Power Dissipation

$$P_{tot} = C_L V_{DD}^2 \alpha f_{clk} + V_{DD} I_{SC} + V_{DD} I_{leak}$$

where,

- $V_{DD} =$ supply voltage
- $C_L =$ load capacitance
- $f_{clk} =$ frequency of the clock in the circuit
- $\alpha =$ activity of the signal

- Computing power dissipation is a challenging problem.
  - ➢ Capacitance estimation
  - ➢ Accounting for the activity of signals

Activity of a signal depends on:

- Application being run on an IC
- Logical structure and the circuit topology

Estimation of Activity

Simulation-based Techniques (Vector-based Technique):

- Perform simulation using test bench.
- Simulator generates the output response for all the nets [value change dump (VCD) files]
  - Convert a VCD file into a format from which the activity measures can be easily extracted [switching activity interchange format (SAIF)]
  - Provide the SAIF file to the power analysis tool
  - Tools can also assume default activity [such as 0.2]

Probabilistic Techniques (Vector-less Technique):

- Propagate the activity measures through the circuit by considering the logic function of the gates encountered in the path
- Example: Assume that static probabilities of signals A and B are $P_1^A = 0.5$ and $P_1^B = 0.3$
  - If they propagate through an AND gate: $P_1^{A.B} = P_1^A . P_1^B = 0.5 \times 0.3 = 0.15$
  - If they propagate through an OR gate: $P_1^{A+B} = 1 - (1 - P_1^A)(1 - P_1^B) = 1 - 0.5 \times 0.7 = 0.65$

References

- N. H. Weste and D. Harris. “CMOS VLSI Design: A Circuits and Systems Perspective”. *Pearson Education India, 2015*.
- S. Saurabh, “Introduction to VLSI Design Flow”. Cambridge: *Cambridge University Press*, 2023.