VLSI DESIGN FLOW: RTL TO GDS

Lecture 8
Overview of VLSI Design Flow: VI

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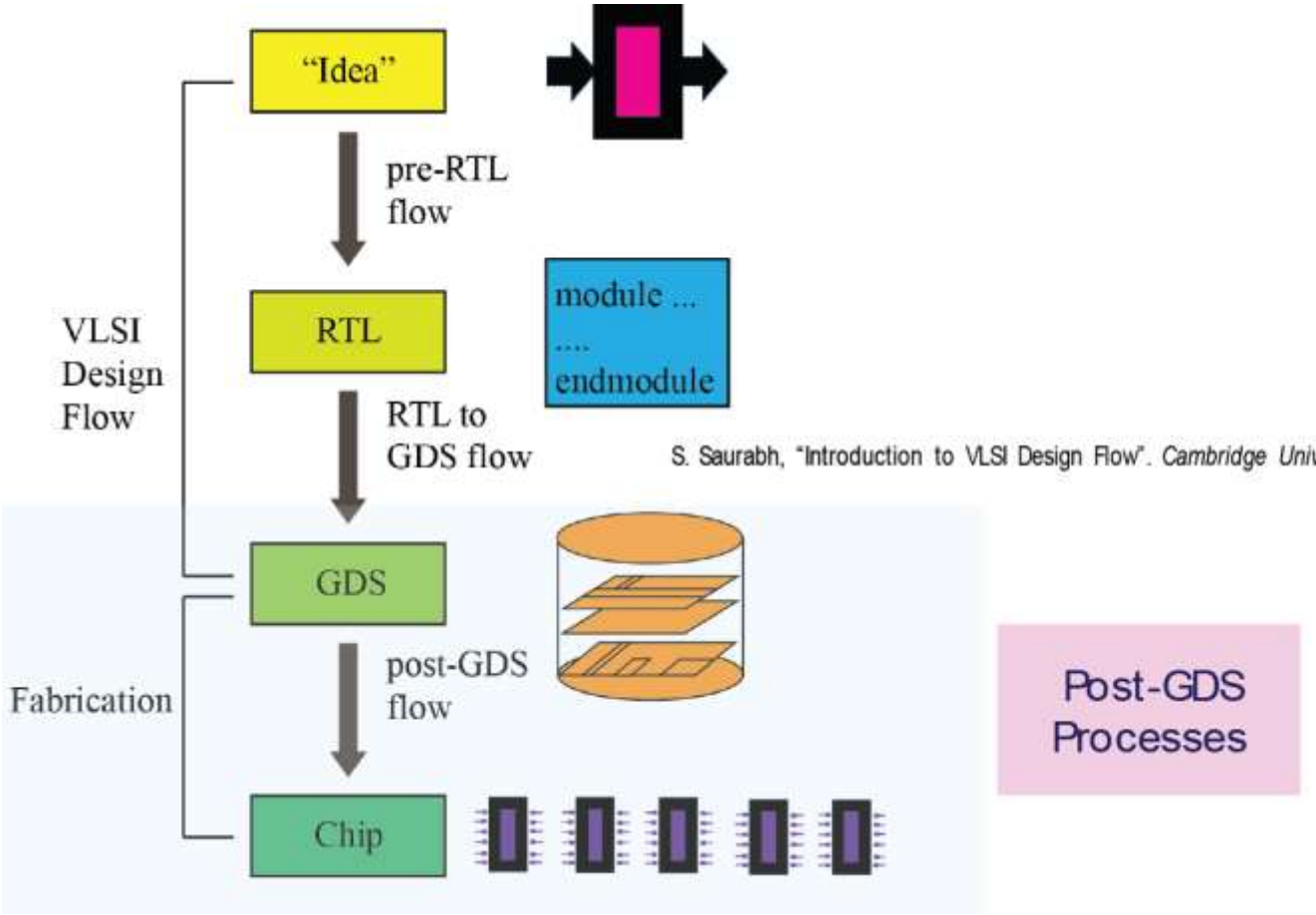
Lecture Plan



Post-GDS Processes

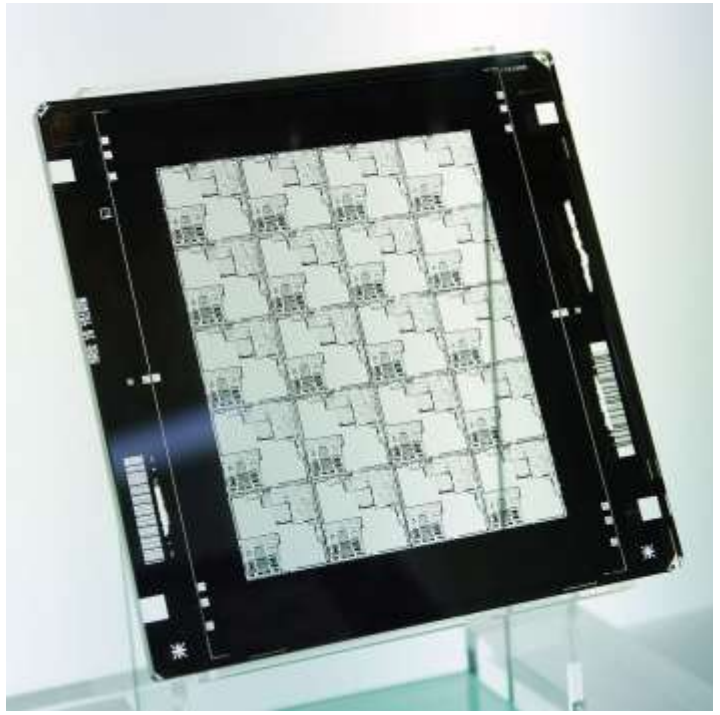
Mask Fabrication

- Mask is the replica of the patterns on a given layer of the layout created on a substrate (glass) for transferring pattern during photolithography

- We need to fabricate mask before fabricating the corresponding IC

Mask fabrication typically involves following steps:

- Data preparation
- Mask writing and chemical processing
- Quality checks and adding protections

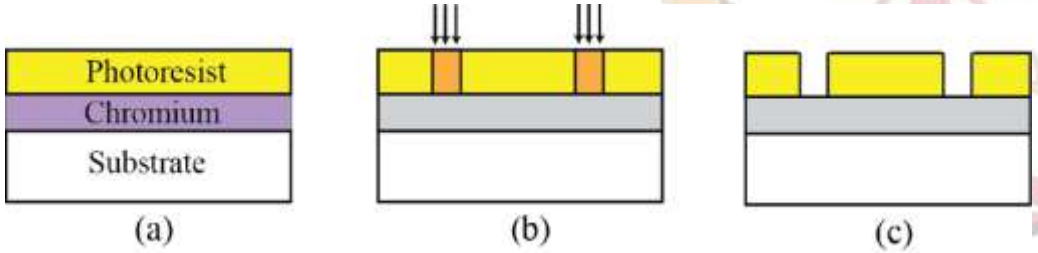


Source: https://commons.wikimedia.org/wiki/File:Semiconductor_photomask.jpg Peellden, CC BY-SA 3.0 <https://creativecommons.org/licenses/by-sa/3.0>, via Wikimedia Commons

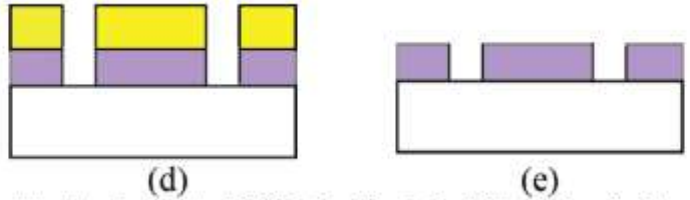
Mask Writing, Quality Checks and Protection

Data preparation:

- Translate the layout-specified mask information to a format comprehended by a mask writing tool
  - ➢ Convert complicated polygons to simpler rectangles and trapeziums (fracturing)
- Augment mask data to enhance resolution



S. Saurabh, "Introduction to VLSI Design Flow". *Cambridge University Press*, 2023.



S. Saurabh, "Introduction to VLSI Design Flow". *Cambridge University Press*, 2023.

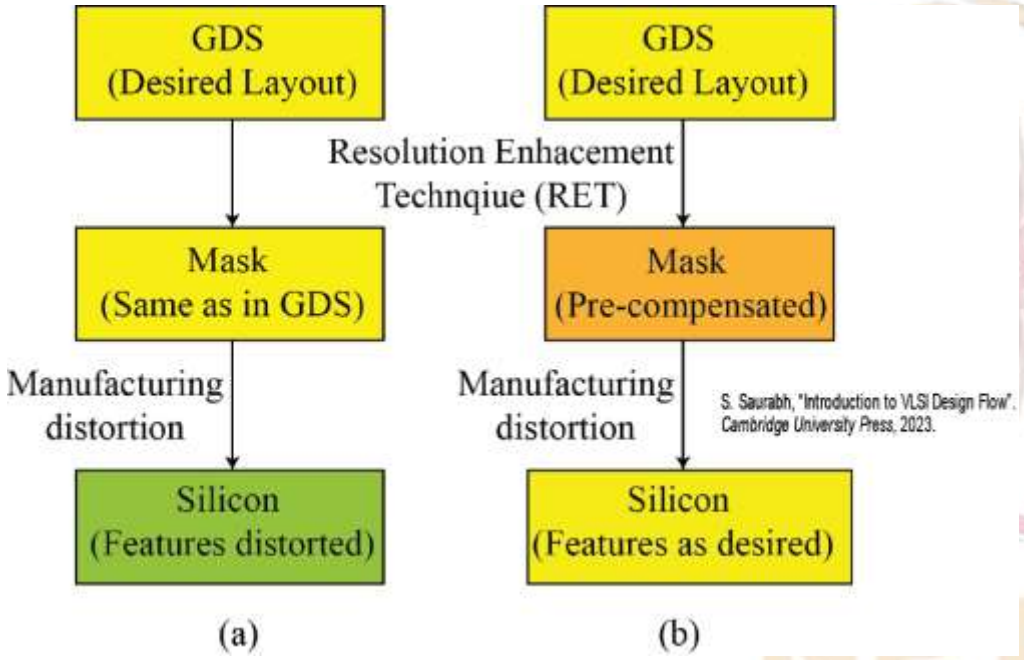
Mask Writing

- Start with chromium and photoresist coated on glass or quartz (**blank**)
- Pattern written on the ***blank*** by exposing to LASER or electron beam
- Photoresist is developed, chromium is etched and then photoresist is stripped

Quality checks and protection

- Inspect for defects by scanning its surface and comparing it with the reference image
- If a defect is beyond tolerance, we repair it with the help of LASER
- Finally, protective cover called **pellicle** is applied

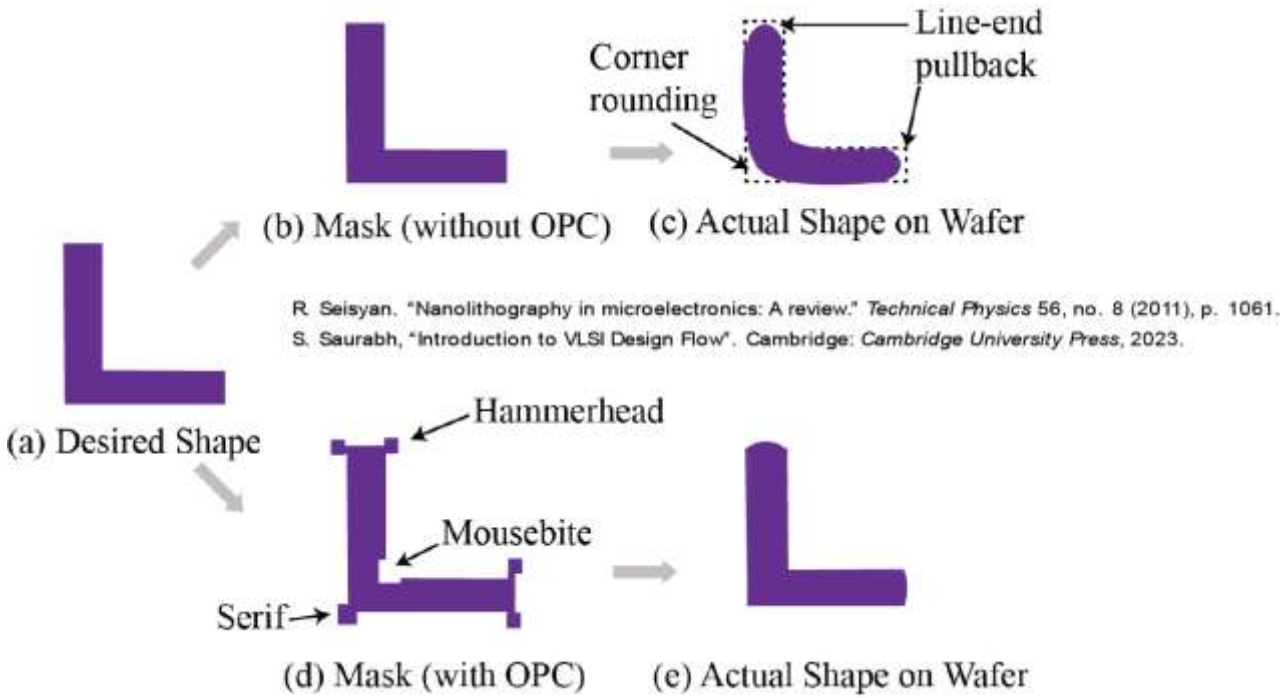
Resolution Enhancement Techniques (RET)



- If mask is patterned exactly as in GDS, then features obtained on silicon is distorted
  - Due to physical effects such as diffraction

- Resolution Enhancement Techniques (RET): mask is pre-compensated such that the features obtained on the mask is same as is desired
  - Examples: Optical Proximity Correction (OPC) and Double/Multi-Patterning

RET: Optical Proximity Correction (OPC)



R. Seisyan. "Nanolithography in microelectronics: A review." *Technical Physics* 56, no. 8 (2011), p. 1061.
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- Printing mask patterns smaller than the light wavelength produces distortions
- E.g.: rounding of corners and line-end pullback.

Optical Proximity Correction (OPC)

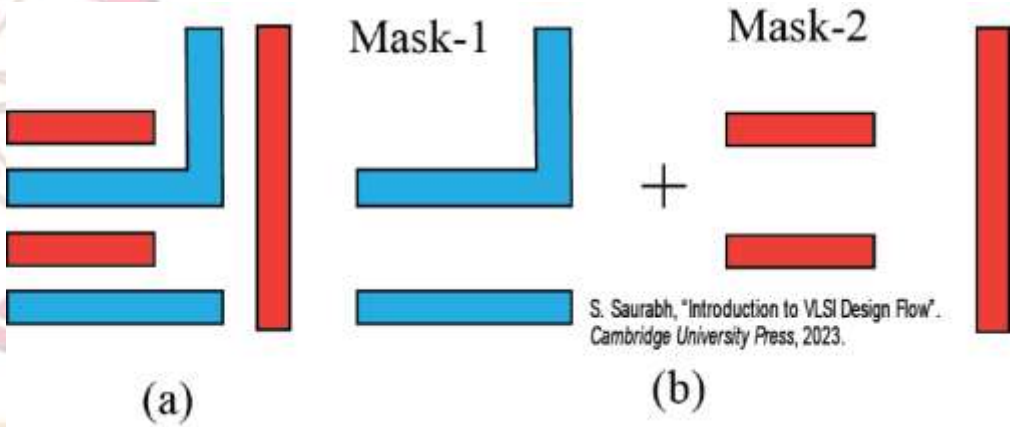
- Add appropriate serifs, hammerheads, and mouse bites to the mask
- Improves the resolution of photolithography by compensating errors due to diffraction etc.

RET: Double- or Multiple-patterning

- Limited resolution of photolithography, pose problems in printing closely spaced features on a die (leads to overlaps)
- We can solve the problem by increasing the spacing between features printed at a time

Double- or Multi-patterning

- Decompose a closely spaced layout into two or more layouts (assign colors to features)
- We use different masks and different exposures for layout features of different colors.
- Each exposure needs a lower resolution due to decreased feature or pattern density.



Wafer Fabrication and Die Testing

Wafer Fabrication

- Actual fabrication of design on the silicon wafer is carried out
- Based on photolithography
- Consist of hundreds of individual process steps

- Fabrication is done layer by layer
  - **Front End Of the Line (FEOL) processes:** fabricate circuit elements such as resistors, capacitors, diodes, and transistors on the lower layers
  - **Back End Of the Line (BEOL) processes:** make interconnections using metallic layers at the top of the wafer

Die Testing

- Each die is tested and compared with the expected pattern
- Bad dies are marked and not packaged

Packaging

Packaging

- We encapsulate a die in a supporting case known as a package to form a chip.

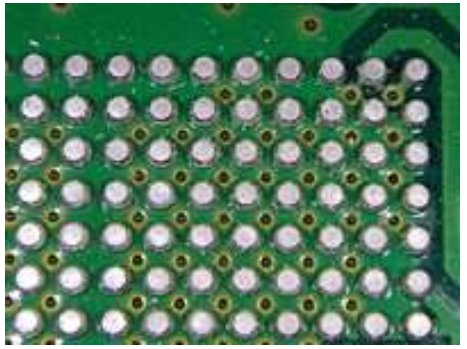
Functions of a package

1. Package provides pins for connecting to external environment
   - ➢ Characteristics of the package have great impact on the delay of the signal entering/leaving the chip
   - ➢ Needs to be carefully designed
2. Package allows dissipation of heat and must be carefully designed
3. Package prevents from mechanical damage and corrosion

Various types and materials are used for package

Dual in-line package (DIP)

Source: https://commons.wikimedia.org/wiki/File:Three_IC_circuit_chips.JPG



Ball grid array (BGA)

Source: https://commons.wikimedia.org/wiki/File:Solder_ball_grid.jpg Janke at English Wikipedia, CC BY-SA 3.0 <https://creativecommons.org/licenses/by-sa/3.0>, via Wikimedia Commons

Final Testing and Binning

Final Testing

- Final testing is done to check if packaging is fine
- Burn-in testing: infant mortality

Finished/Tested chips

- Can be sent to market directly for sale
- Can be integrated with other chips to form a product and then sent to market for sale

Binning

- Classification based on characteristics such as maximum frequency and power dissipation
- Statistical variations in performance
- On-chip delay measurement circuitry
- Assign performance-based price points to different bins.

References

- S. Saurabh, “Introduction to VLSI Design Flow”. Cambridge: *Cambridge University Press*, 2023.
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