VLSI DESIGN FLOW: RTL TO GDS

Lecture 2
Basic Concepts of Integrated Circuit: II

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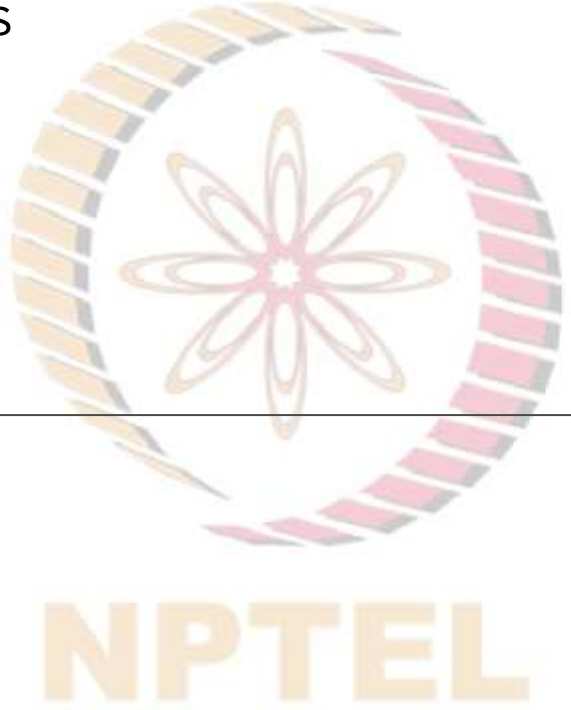
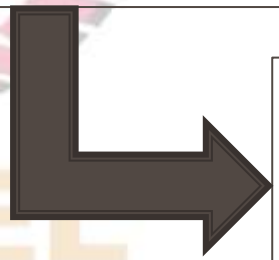
Lecture Plan

Basic Concepts of Integrated Circuit

- Types of Integrated Circuits
- Design Styles
- Economics
- Figures of Merit



Introduction: Some Basic Concepts



Different VLSI Design Flows

Different VLSI Design Flow

What is VLSI Design Flow?

- Methodology to design an IC such that it delivers the required functionality or behavior.

What decides VLSI Design Flow?

- The VLSI design flows depends on the type of integrated circuits:
  - Scope of application
  - Design Styles

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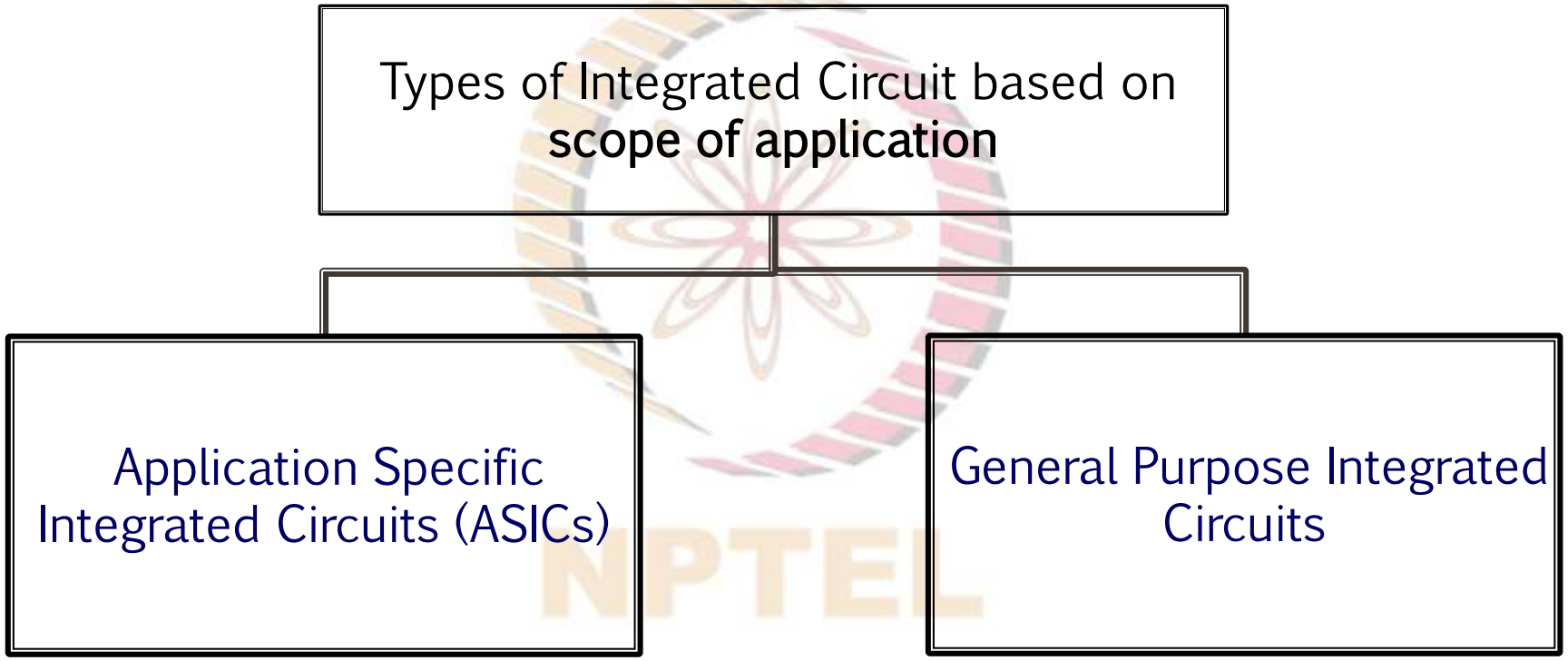
Types of Integrated Circuits

Types of Integrated Circuit



Types of Integrated Circuit

	Application Specific Integrated Circuits (ASICs)	General Purpose Integrated Circuits
Functionality	A chip designed to perform as a particular end system	A chip designed to perform as a wide range of end-system
Examples	IC for digital camera, audio/video processor, security chip etc.	Microprocessors, memory, FPGA
Programmability	Not software programmable to perform a wide variety of different tasks	Usually software programmable to perform a wide variety of different tasks
Volume of production	Less	More

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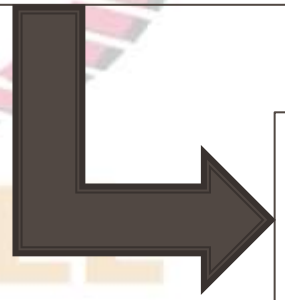
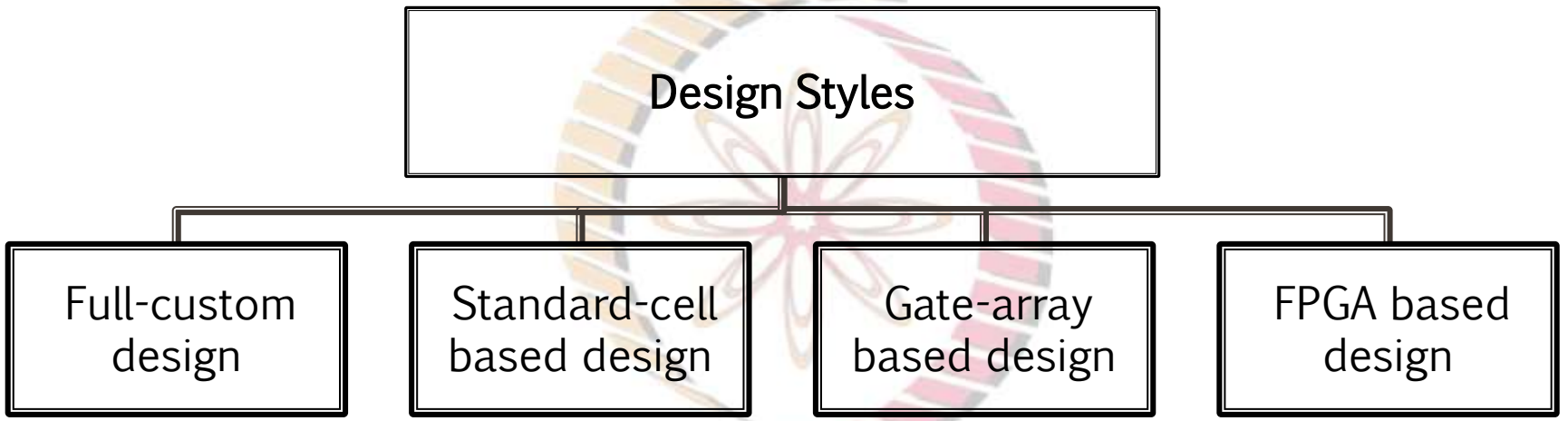


Types of Design Styles

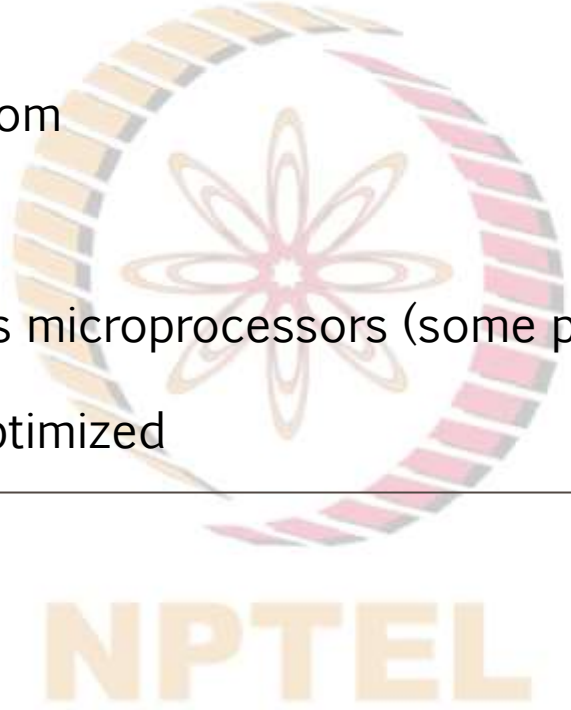
Types of Design Styles



- FPGA: Field Programmable Gate Array

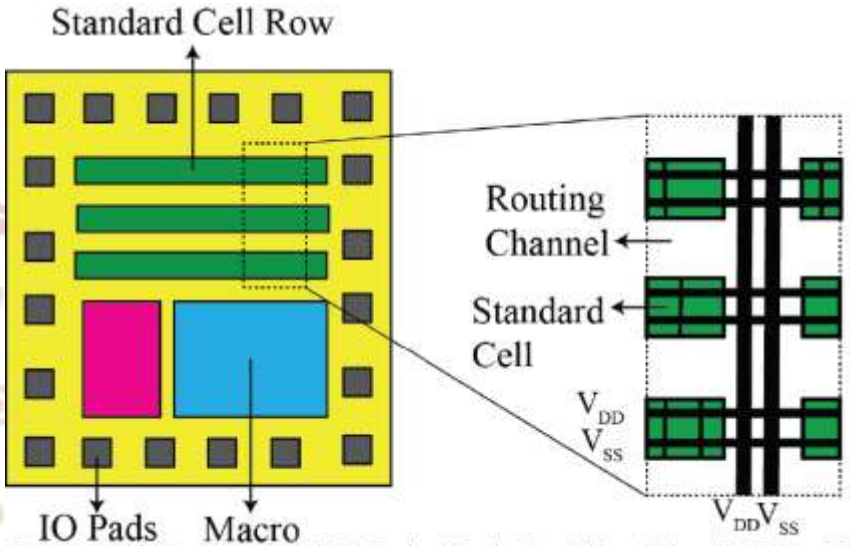
Full-custom design

- Layout of transistors and interconnects are design specific
- Huge design effort
- Very few designs are full-custom
- Analog mixed/signal designs
- High volume products such as microprocessors (some portion)
- Merit: design can be highly optimized



Standard-cell based design

- **Standard Cells**: simple cells such as AND, NAND, flip-flop etc. that are optimally designed and modeled in a library, fixed height
- **Macros: c**omplex cells such as full-adder, multiplier, memory etc.
- Allows high degree of automation



S. Saurabh, "Introduction to VLSI Design Flow". *Cambridge University Press*, 2023.

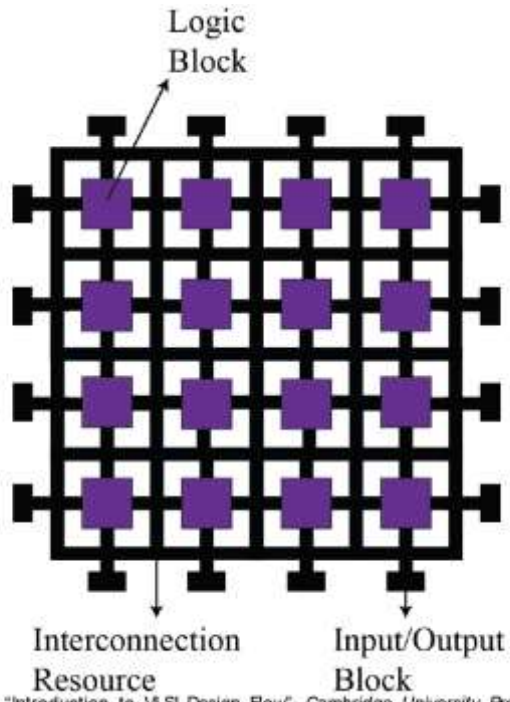
- Rows of standard cells with interconnection in between
- Custom blocks can also be embedded in a design
- Types, locations and interconnections of standard-cells are design specific
  - All layers have different masks for different designs

Gate-array based design

- Transistors are predefined on an IC in the form of a gate array
- Base cell or primitive cells: smallest element that is repeated to form a gate array
- Designer define only the interconnection between transistors:
  - Top-most layers of the masks are design specific

- Fixed functionality of the base cell may make implementing some functions such as memory difficult or inefficient
- Some custom blocks can be embedded in the IC to obtain special functionality such as memory, micro-controller etc.

FPGA based design



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- IC hardware is fixed
- Designer obtain the desired functionality by programming
  - Programming changes the interconnections between the elements of the circuits

- FPGA consist of array of logic blocks, I/O blocks and routing channels
- Logic blocks can be programmed to perform different functions such as AND, OR, adder etc.
- FPGA boards may also have embedded microprocessors, analog components and blocks performing special functions such as DSP block
- Xilinx (AMD), Altera (Intel)

Design Styles (Summary)

	Full-custom design	Standard-Cell based design	Gate-array based design	FPGA based design
Description	Design specific customization at the level of transistors and layout	Pre-characterized cells/macros instantiation and interconnect design specific	Transistors predefined on wafer, interconnect design specific	Programming logic blocks and interconnect
Design effort	Highest	High	Lower	Lower
Custom Mask Layers	All	All	Top few layers	None
Performance, Power, Area	Best	Very Good	Comparatively Inferior	Comparatively Inferior

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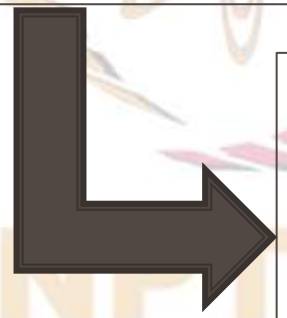


Economics of Integrated Circuit

Economics of Integrated Circuits: Components

Fixed Product Cost

- Cost of designing
  - Depends on size/complexity of design
- Software tools
- Hardware
- Cost of masks
  - Depends on number of layers

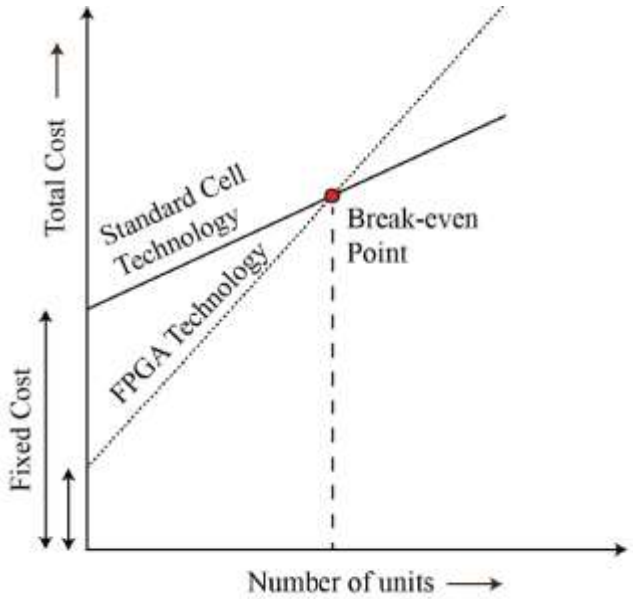
Variable Product Cost

- Cost of wafer
- Cost of die
  - ➢ Depends on size of die
  - ➢ Yield

$$Total\ product\ cost\ =\ Fixed\ product\ cost\ +\ Variable\ product\ cost \times Number\ of\ Product$$

Economics of Integrated Circuits: Comparison

	Standard-cell based design	FPGA-based design
Fixed Cost	High: designing cost, tools, mask	Low: tools for programming
Variable Cost	Low: cost of die (small die size, higher yield)	High: cost of die (large die size, low yield)



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For small volume FPGA is better, for large volume standard-cell based design is better.

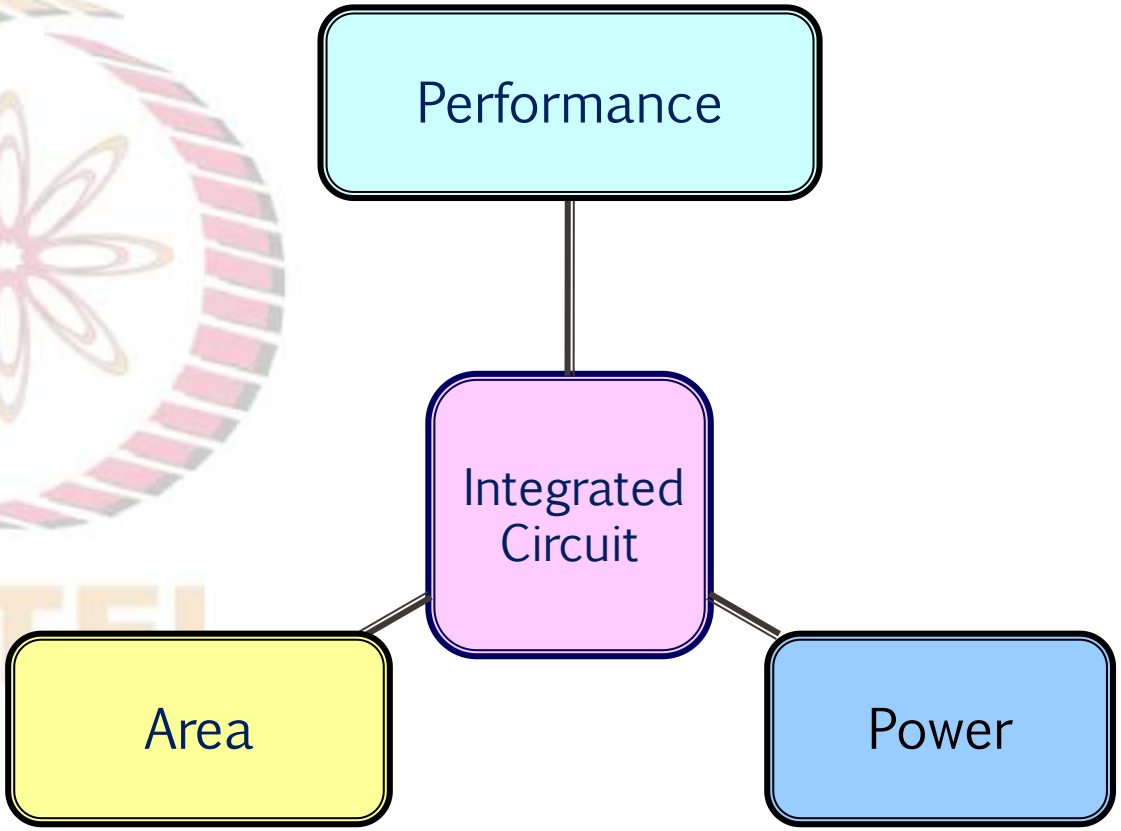
Introduction: Some Basic Concepts

Figures of Merit

Figures of Merit (FoMs) (1)

- How do we assess the "*goodness*" of an IC?

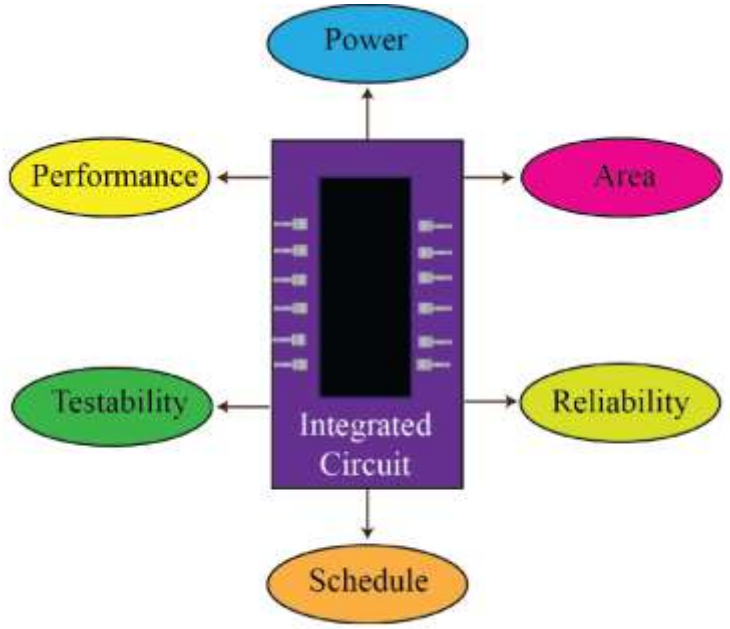
- **Power, Performance, Area (PPA) measure**
  - Power: sum of static and dynamic power consumed by an IC
  - Performance: maximum frequency of clock at which an IC will work
  - Area: area of the die for an IC
- Example: $(1\ W, 2.0\ GHz, 1\ mm^2)$



Figures of Merit (FoMs) (2)

- Other FOMs:
  - Testability
  - Reliability
  - Schedule

- Figures of Merit are also called Quality of Result (QoR) measure
- Improving one measure might adversely affect other measure(s)
  - Some measures might be required to be **traded-off**



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- Mathematical optimum FoM for a given design is rarely known or achieved
- Goal of a design flow is to find one of the feasible solutions with acceptable FoM

References

- S. Saurabh, “Introduction to VLSI Design Flow”. Cambridge: *Cambridge University Press*, 2023.
- M. J. S. Smith. “Application-Specific Integrated Circuits,” vol. 7. *Addison-Wesley Reading*, MA, 1997.