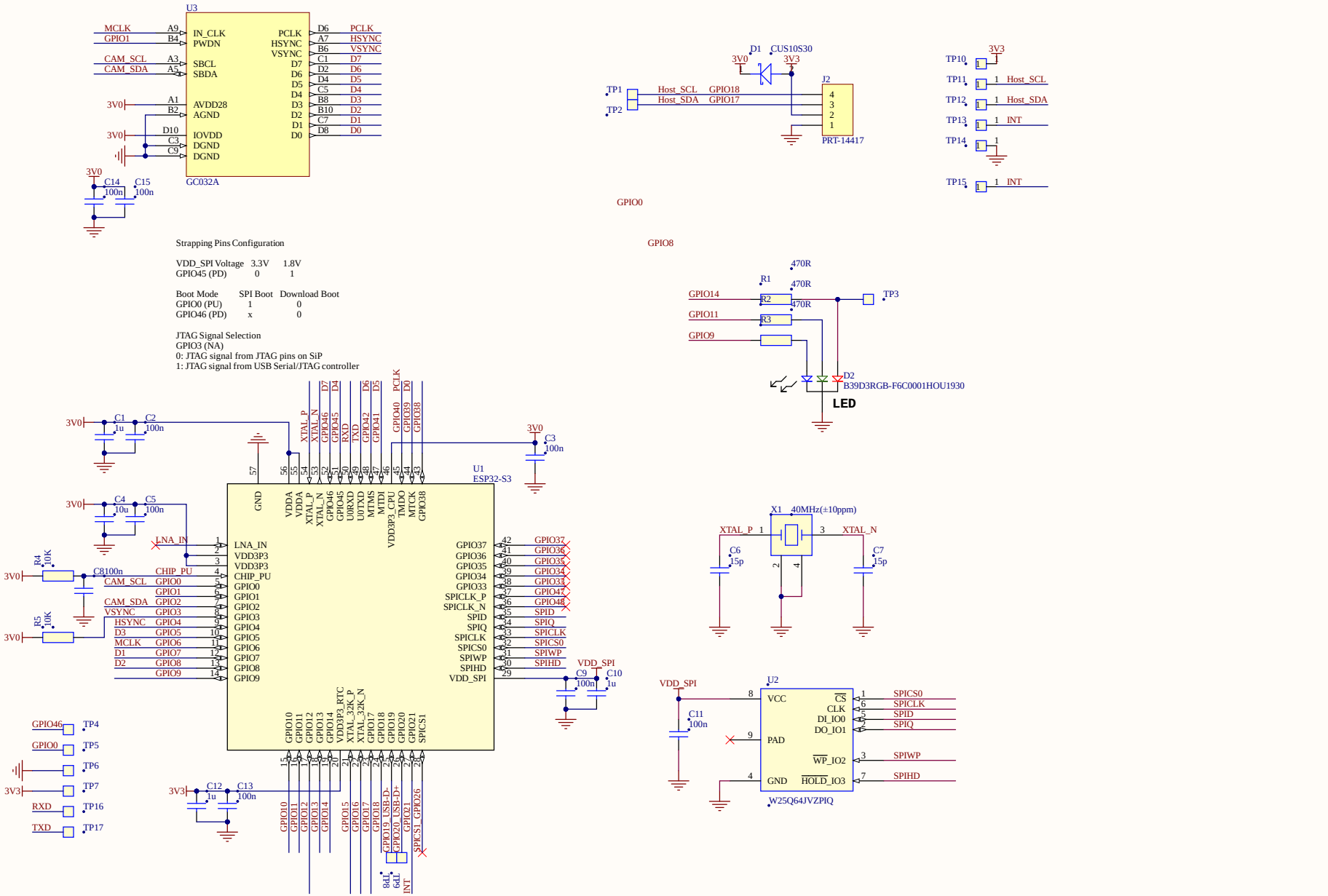
U3
GC032A
MCLK
GPIO1
CAM_SCL
CAM_SDA
IN_CLK
PWDN
SBCL
SBDA
AVDD28
AGND
IOVDD
DGND
PCLK
HSYNC
VSYNC
D7
D6
D5
D4
D3
D2
D1
D0
C14 100n
C15 100n
Strapping Pins Configuration
VDD_SPI Voltage 3.3V 1.8V
GPIO45 (PD) 0 1
Boot Mode SPI Boot Download Boot
GPIO0 (PU) 1 0
GPIO46 (PD) x 0
JTAG Signal Selection
GPIO3 (NA)
0: JTAG signal from JTAG pins on SiP
1: JTAG signal from USB Serial/JTAG controller
U1
ESP32-S3
C1 1u
C2 100n
C3 100n
C4 10u
C5 100n
C8 100n
R4 10K
R5 10K
LNA_IN
CHIP_PU
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO8
GPIO9
GPIO35
GPIO36
GPIO37
SPICLK_P
SPICLK_N
SPID
SPIQ
SPICLK
SPICS0
SPIWP
SPIHD
VDD_SPI
C9 100n
C10 1u
C12 1u
C13 100n
TP4
TP5
TP6
TP7
TP16
TP17
RXD
TXD
D1 CUS10S30
J2
PRT-14417
Host_SCL
Host_SDA
TP1
TP2
TP10
TP11
TP12
TP13
TP14
TP15
INT
GPIO0
GPIO8
R1 470R
R2 470R
R3 470R
GPIO14
GPIO11
GPIO9
TP3
D2
B39D3RGB-F6C0001HOU1930
LED
X1 40MHz(±10ppm)
C6 15p
C7 15p
U2
W25Q64JVZPIQ
C11 100n
Title
Size A3
Number
Revision
Date: 5/29/2023
Sheet of
File: E:\钟寿虎\TCR_V2.0\Sheet1(1)(1).SchDoc
Drawn By: