A guide to using FETs for voltage-controlled circuits, Part 5

Ron Quan - July 03, 2018

See Part 1, Part 2, Part 3, and Part 4 of this series.

The final part of this series will start with bias servo circuits for automatic set up. The FETs pinch off or threshold voltage can vary widely for the same part number. Depending on the fabrication wafer lot chosen, these voltages can vary 2 or 3 to one. To bias them correctly for a predetermined drain-to-source resistance, the user must hand-adjust and calibrate the bias voltage across the gate and source. We can more easily bias the gate to source voltage with a matched dual FET or matched quad FET array. One FET from the dual or quad device is used as a reference for precisely biasing the gate of the remaining FET(s) for a predictable drain to source resistance.

With a bias servo circuit, the drain to source resistance is always set correctly regardless of which matched FETs are used. For example, if you set the bias servo circuit to provide a 10KΩ drain-t--source resistance, R_{ds}, you can plug in a different batch of dual FETs such as LSK489, LSK389, etc. and you will still have the same R_{ds}. See **Figure 40**, a Wah-Wah variable band pass filter circuit with a bias servo circuit.

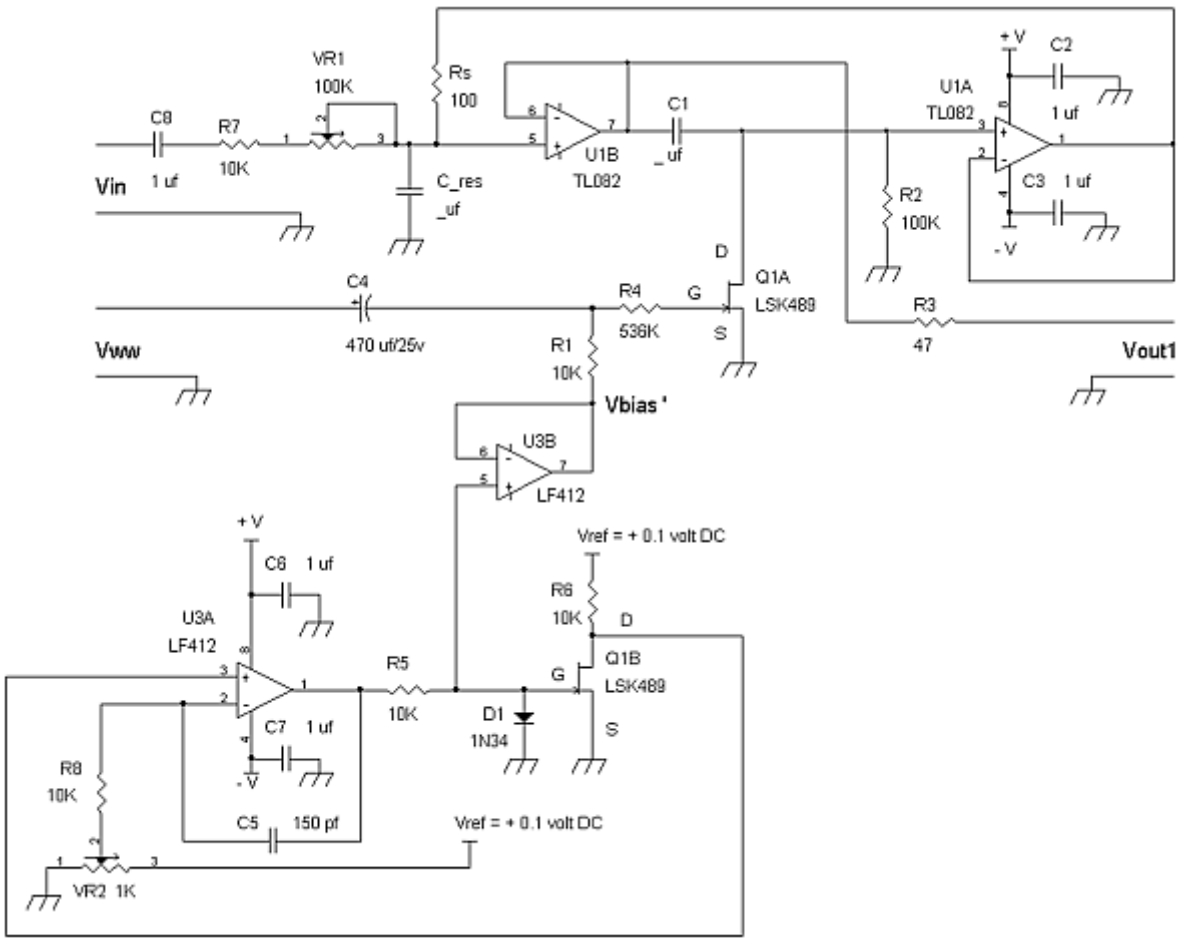

Figure 40 Incorporating a feedback or servo biasing circuit, U3 and Q1B, provides the correct gate voltage to an FET for a known drain-to-source resistance.

By using a reference FET, Q1B with a small DC bias voltage, Vref = +100 mV DC and a known load resistor, R6, we can bias Q1B to any drain to source resistance, R_{ds} by setting the voltage to R8 via potentiometer VR2 pin 2. The small DC voltage, Vref is set to +100 mV DC to ensure that the Q1B is still in the triode or ohmic region. If we set VR2's slider voltage = Vset to provide half the voltage, or +50 mV, this will cause the bias servo circuit to turn on Q1B until its drain voltage is also +50 mV DC. If we get half of the +100 mV = 50 mV at the Q1B's drain via the 10KΩ series resistor R6, this means the drain to source resistance is also 10KΩ. Because the bias servo circuit is a negative feedback circuit whatever voltage we set at VR2's slider, which is coupled to U3A's (-) input, its (+) input must follow that voltage by the virtual short circuit across the input terminals. Since the (+) input terminal is connected to the Q1B's drain, its drain voltage must match the voltage at VR2's slider. Compensation capacitor, C5, ensures that the circuit does not oscillate. For better noise rejection, C5 can be as large as 1 uf.

With Vset = voltage at pin 2 of VR2, the general equation that solves for Q1A's R_{ds} is:

$$R_{dsQ1A} = R6 / [\frac{Vref}{Vset} - 1] = R_{dsQ1A} = R6 / [\frac{0.1\ v}{Vset} - 1]$$

$$R_{dsQ1A} = 10K\Omega / [\frac{0.1\ v}{Vset} - 1] \text{ and have Vset} \rightarrow 50 \text{ mv}$$

$$R_{dsQ1A} = 10K\Omega / [\frac{0.1\ v}{0.05\ v} - 1] = 10K\Omega / [\ 2 - 1\ ] = 10K\Omega$$

When the reference voltage Vref is small like 100 mV, we should choose an op amp for very small

input offset voltages. The TL082/TL062/LF353 op amps have maximum offset voltages of 10 mV, which is not recommended. An LF412 can be used, which has a lower 3 mV input offset voltage. Of course, other low offset voltage op amps can be used (**Figures 41, 42,** and **43**).

Note: Diode D1 ensures that the reference FET's gate does not forward bias during turn-on. If the gate does forward bias, the bias servo circuit may be "stuck."

In terms of maximum input signal amplitude for low distortion, usually < 150 mV peak-to-peak will work. However, generally FETs such as the VCR 11 with a higher pinch off voltage can tolerate a higher input amplitude > 150 mV peak to peak.

Now let's look at **Figure 41**, the Wah-Wah voltage-controlled band-pass filter with distortion lowering feedback via Rfb and R4 with a bias servo circuit.

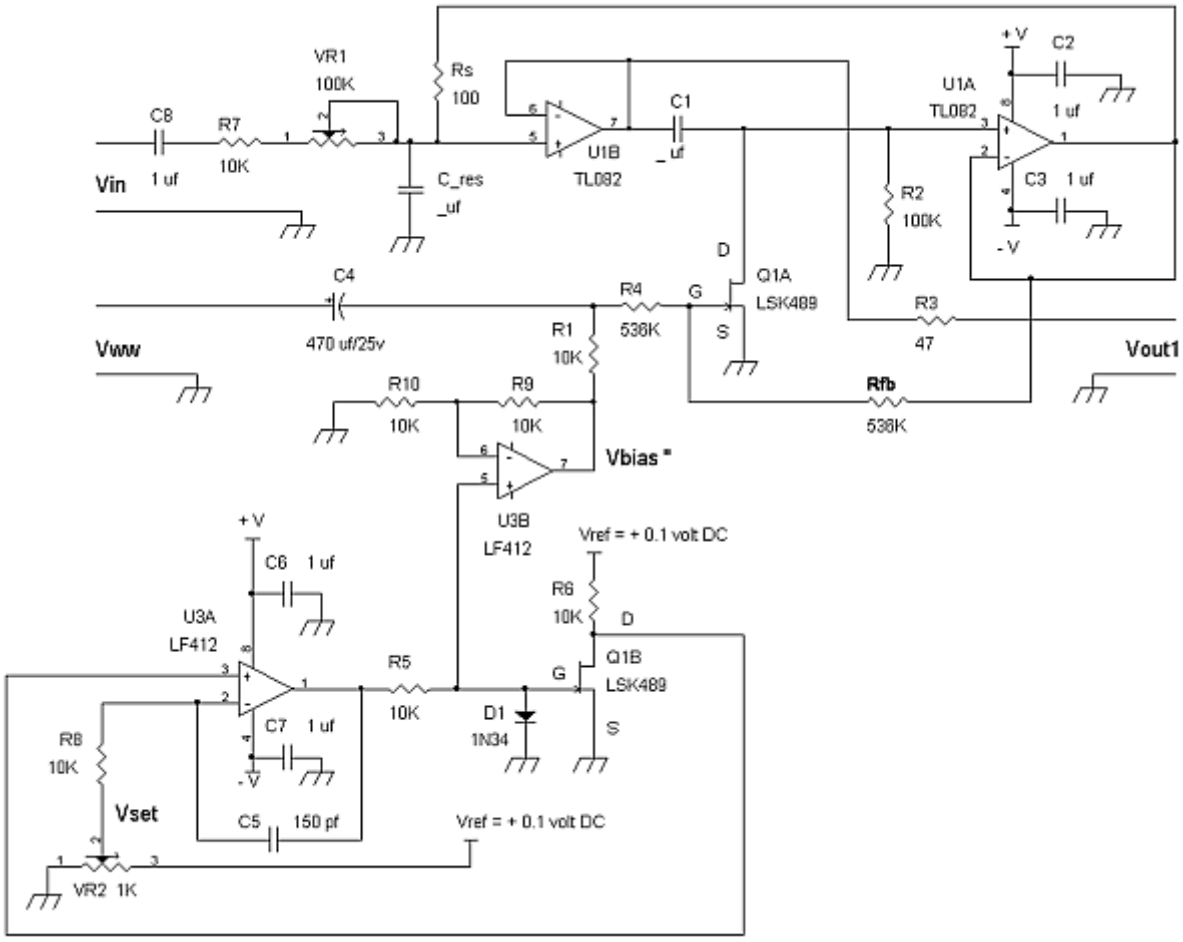

Figure 41 Automatic bias approximation when feedback is employed with the voltage-controlled resistor.

Because the distortion-lowering feedback network Rfb and R4 has about a 50% attenuation to the gate, amplifier U3B is set for a gain of 2 to compensate for this. Note that R1 <<R4 so that this 50% approximation holds.

Although increasing the gate voltage of Q1B approximates the same R_{ds} for Q1A, the drain to source resistance of Q1A is actually lower for the same gate voltages of Q1A and Q1B. The reason is that the resistor network, Rfb and R4 forms a negative feedback effect that slightly lowers Q1A's R_{ds}. That is $R_{dsQ1A} < R_{dsQ1B}$ by a little.

Nevertheless **Figure 41** still provides an easier way to bias the FETs when compared to doing it

manually. We will revisit a more accurate way to **Figure 41** later.

For now, let's see a bias servo circuit for the phase shifting system in **Figure 42**. It uses the same bias servo circuit as in **Figure 40**, but this time with MOSFETs for the voltage-controlled resistors. Note that D1 is connected in reverse to ensure the gate to source voltage does not go too negative for the N Channel enhancement devices upon turn on.

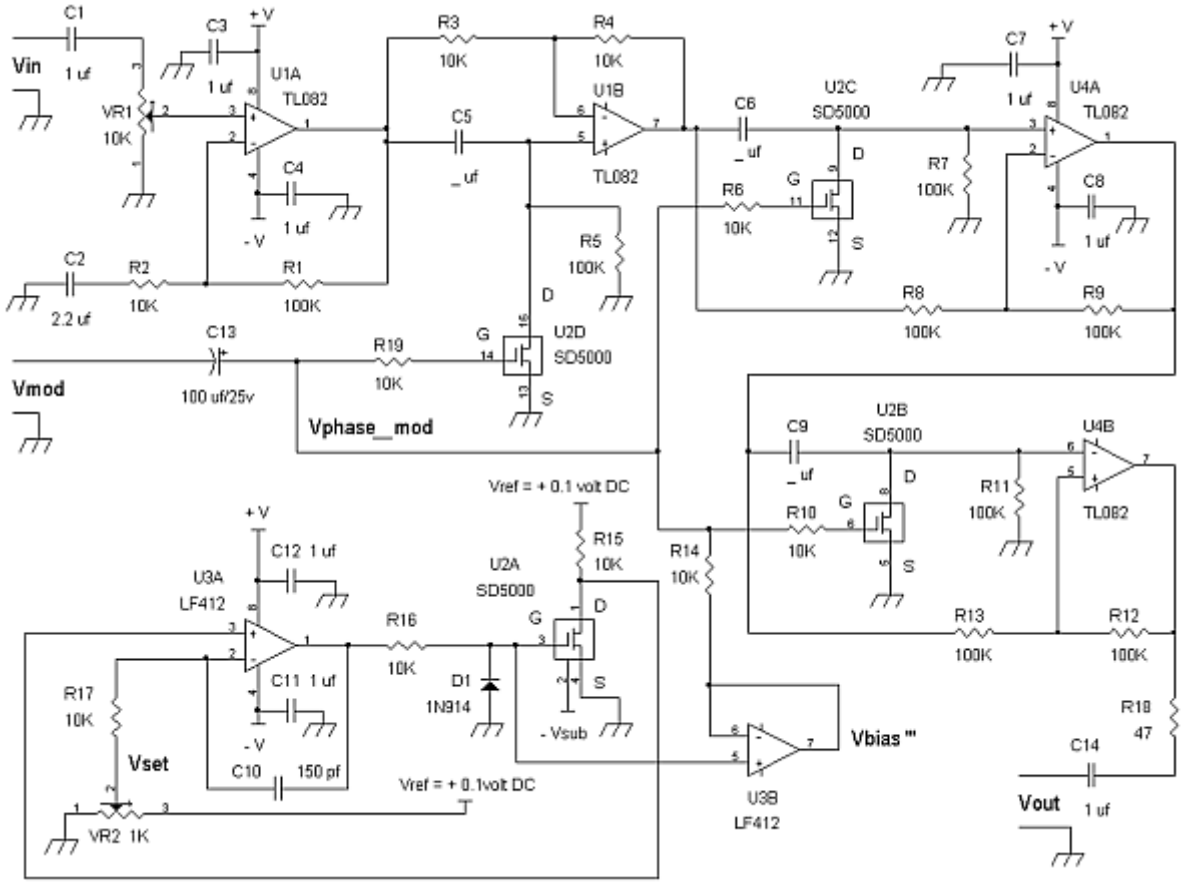

Figure 42 A three stage phase shifting system with a bias servo system.

The total phase shift from this circuit is:

$$\phi_{total} = -3[180 \text{ degrees} - 2\arctan(f/f_c)]$$

Where $f_c = 1/(2\pi RC)$ and $R = R_{ds} \,||\, R7 = R_{ds} \,||\, R5 = R_{ds} \,||\, R11$; $C = C5 = C6 = C9$

R_{ds} = drain to source resistances of U2B, U2C, and U2D, which are all equal.

$$R_{ds} = R15/\left[\frac{0.100\,v}{Vset} - 1\right], \text{ or with } R15 = 10K\Omega$$

$$R_{ds} = 10K\Omega/\left[\frac{0.100\,v}{Vset} - 1\right]$$

As an example, *Vset* = 0.033 v = voltage at pin 2 VR2, then

$$R_{ds} = 10K\Omega/\left[\frac{0.100\,v}{0.033\,v} - 1\right] = 10K\Omega/[\,3 - 1\,] = 5K\Omega$$

Note that –Vsub = −5 volts to −10 volts DC to ensure that the substrate is biased correctly.

Instead of using Vww, a modulating signal may be coupled to VR2 pin 2 with a 1000 uf electrolytic capacitor with its (+) terminal at pin 2 of VR2.

See **Figure 43**, an improved servo biasing circuit.

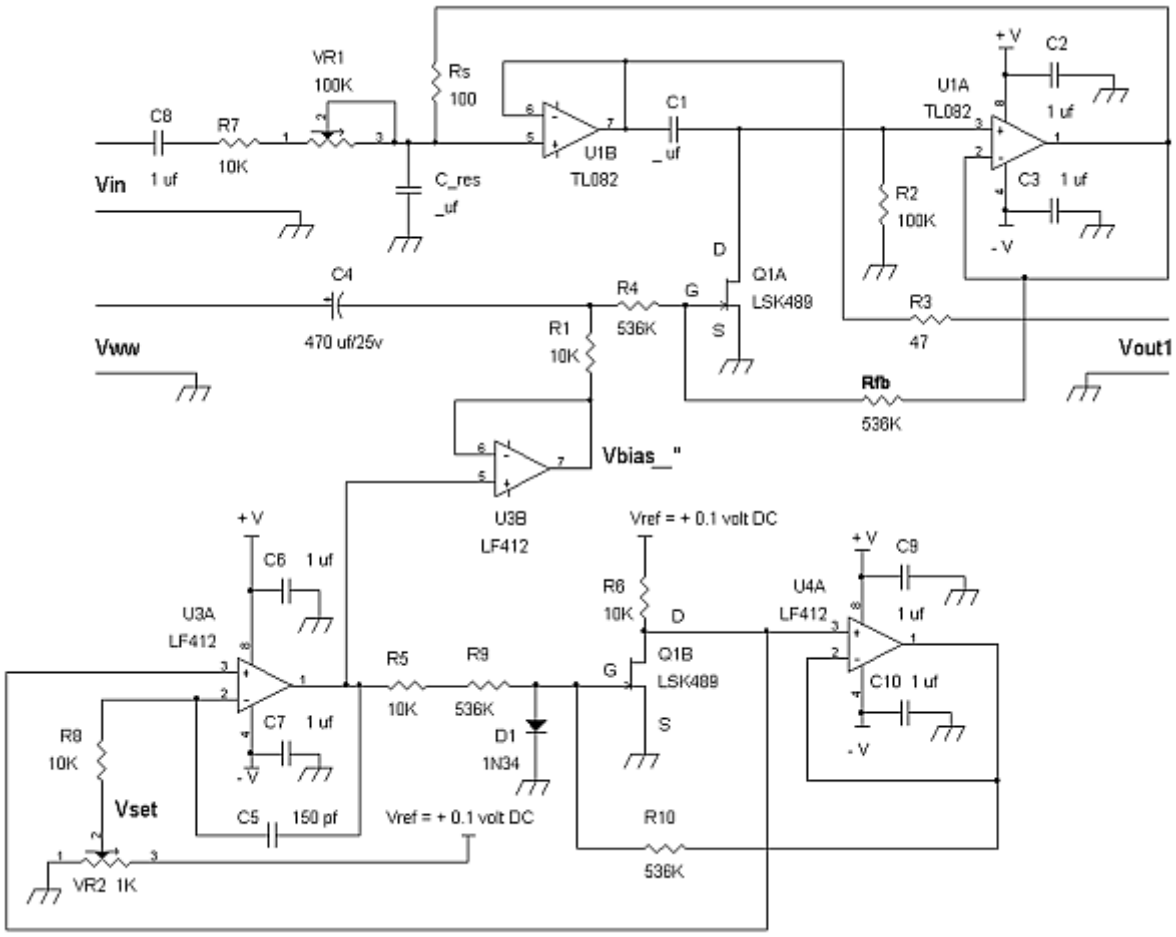

Figure 43 Improved servo biasing via replication of VCR's feedback circuit for Wah-Wah circuit.

To determine more accurately the R_{ds} of Q1A, the bias servo circuit replicates the feedback network via U4A that "copies" U1A, and R10 with R9 that copies Rfb and R4.

We should also note that even though this circuit can more precisely set the correct gate biasing voltage, the actual drain to source resistance for Q1A will be slightly lower due to a negative feedback effect from Rfb and R4. So, we will use "~" for approximately instead of "="

The biasing is set by the VR2's slider voltage at its pin 2, Vset such that:

$$R_{ds\_Q1a} \sim R6 \,/\, \left[\frac{0.100\ v}{Vset} - 1 \right], \text{ and with } R6 = 10K\Omega$$

$$R_{ds\_Q1a} \sim 10K\Omega \,/\, \left[\frac{0.100\ v}{Vset} - 1 \right]$$

For another example, $Vset = 0.075$ v

$$R_{ds\_Q1a} = 10K\Omega \,/\, \left[\frac{0.100\ v}{0.075\ v} - 1 \right] = 10K\Omega \,/\, [\ 1.33 - 1\ ] = 30K\Omega$$

Again, instead of using Vww, a modulating signal (< 20 mV peak to peak to ensure that the bias servo circuit is within its range for Vset) may be coupled to VR2 pin 2 with a 1000 uf capacitor.

Note: *Lower distortion may be achieved by setting the FET's drain to source resistance to a higher value. For example, we set R6 to 51KΩ instead of 10KΩ , and set* R_{ds_Q1a} *to be in the > 100KΩ range.*

For P Channel JFET devices with **Figures 41 and 43**, use a negative Vref such as – 100 mV DC and reverse diode D1's connections. And for P Channel MOSFETs using **Figure 42**, use a negative Vref such as – 100 mV DC and reverse diode D1's connections.

Final tips and thoughts

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DMOS devices have the advantage of very low drain-to-gate capacitance. For working with these devices in a dual inline package (DIP) such as the SD5000 series, make sure to bias the substrate pin via a resistor (e.g., 1KΩ to 10KΩ) with a voltage source more negative or lower than any of the voltages that appear at any other pins. As an example, if the minimum source voltage is ground, the substrate voltage should be −2 volts to −9 volts. If the AC signal across the drain and source is small such as < 150 mV peak to peak, then it may be possible to just tie the substrate terminal to the source terminal of the FET that has the lowest source potential.

There are some DMOS FETs that have very low gate capacitance and are not protected by internal zener diodes that would otherwise add more gate capacitance. DMOS devices such the SD211 and SD214 come with a shorting wire. The gate and source leads are soldered first to a circuit that provides a DC path from gate-to-source, and then you can remove the shorting wire. With the shorting wire intact, you can solder a 10KΩ resistor across the gate and source leads before removing the shorting wire, but before soldering the DMOS FET to the circuit.

This paper has covered some basic voltage-controlled circuits. These can be used in more complex systems such as guitar effects pedals. For example, the voltage-controlled resistor circuits with feedback shown in Figures 8 to 15 can be also used as symmetrical clipping circuits by overdriving the input signal. Voltage controlled attenuator circuits without feedback (e.g., by removing R3 in Figures 8 to 15) can be used as non-symmetrical clippers by again overdriving the input signal. These clipping circuits can be incorporated into electric guitar fuzz pedals.

Appendix A

MOSFET equations for cancelling distortion in voltage controlled resistors

Given the general MOSFET equations below, we will find a way to add a portion of the drain-t--source voltage back with the control voltage to cancel out nonlinearities of the FETs' drain to source resistance.

$$I_d = \frac{k'}{2}\frac{W}{L}\,[\,2(Vgs - V_{th})Vds - (Vds)(Vds)] \qquad \text{(1-AP)}$$

$k' = \mu_n C_{ox}$

$C_{ox} = \varepsilon_{ox} / t_{ox}$

W = width of the MOS device

L = channel length of the MOS device

In equation (1-AP) the part that we want to eliminate is the $(Vds)(Vds)$ term. If this is cancelled out we will be left with a drain current relationship relative to the constants k', W, Vgs, and V_{th} along with a variable Vds. However, once we take the slope or derivative of the drain current with respect to the drain to source voltage Vds, we will have linear conductance.

Let the gate-to-source voltage include a portion of the drain-to-source voltage by having:

$Vgs \rightarrow Vct + K\,Vds$ where the scaling factor K has a range of $0 < K < 1$, and Vct is a DC bias voltage to control the FET's drain to source resistance.

Equation (1-AP) becomes by substitution of $Vgs \rightarrow Vct + K\,Vds$:

$$I_d = \frac{k'}{2}\frac{W}{L}\,[\,2(Vct + K\,Vds - V_{th})Vds - (Vds)(Vds)] \qquad \text{(2-AP)}$$

$$I_d = \frac{k'}{2}\frac{W}{L}\,[2(Vct + K\,Vds - V_{th})Vds\,] - \frac{k'}{2}\frac{W}{L}\,[(Vds)(Vds)]$$

$$I_d = \frac{k'}{2}\frac{W}{L}\,[2(Vct - V_{th})Vds\,] + \frac{k'}{2}\frac{W}{L}\,[\,2(K\,Vds)\,Vds] - \frac{k'}{2}\frac{W}{L}\,[(Vds)(Vds)] \qquad \text{(3-AP)}$$

To cancel out the $(Vds)(Vds)$ term, we equate:

$$\frac{k'}{2}\frac{W}{L}\,[\,2(K\,Vds)\,Vds] - \frac{k'}{2}\frac{W}{L}\,[(Vds)(Vds)] = 0$$

This then leads to:

$$\frac{k'}{2}\frac{W}{L}\,[\,2(K\,Vds)\,Vds] = \frac{k'}{2}\frac{W}{L}\,[(Vds)(Vds)]$$

Now let's divide both sides by $\frac{k'}{2}\frac{W}{L}$, which results in

$[\,2(K\,Vds)\,Vds] = [(Vds)(Vds)]$

And if we further divide both sides by $(Vds)(Vds)$, then that gives us:

$2(K) = 1$

We can now divide by 2 on both sides which yields:

$$K = \frac{1}{2}$$

With $K = \frac{1}{2}$, and referring back to equation (3-AP)

$$I_d = \frac{k'}{2}\frac{W}{L}[2(Vct - V_{th})Vds] + \frac{k'}{2}\frac{W}{L}[2(\frac{1}{2}Vds)Vds] - \frac{k'}{2}\frac{W}{L}[(Vds)(Vds)]$$

We see that the last two terms cancel and we are left with:

$$I_d = \frac{k'}{2}\frac{W}{L}[2(Vct - V_{th})Vds]$$

The conductance from drain to source, g_{ds}, when $K = \frac{1}{2}$ is then

$$g_{ds} = \frac{d}{dVds} I_d = \frac{d}{dVds}\left(\frac{k'}{2}\frac{W}{L}[2(Vct - V_{th})Vds]\right) = \frac{k'}{2}\frac{W}{L}[2(Vct - V_{th})]$$

$$g_{ds} = \frac{k'}{2}\frac{W}{L}[2(Vct - V_{th})]$$

And the resistance from drain to source, R_{ds} is the reciprocal of the conductance, g_{ds}

$$R_{ds} = 1/g_{ds} = 1/\left(\frac{k'}{2}\frac{W}{L}[2(Vct - V_{th})]\right)$$

$$R_{ds} = 1/\left(\frac{k'}{2}\frac{W}{L}[2(Vct - V_{th})]\right) \text{ when } K = \frac{1}{2}$$

Figure AP-A-1 shows an example circuit.

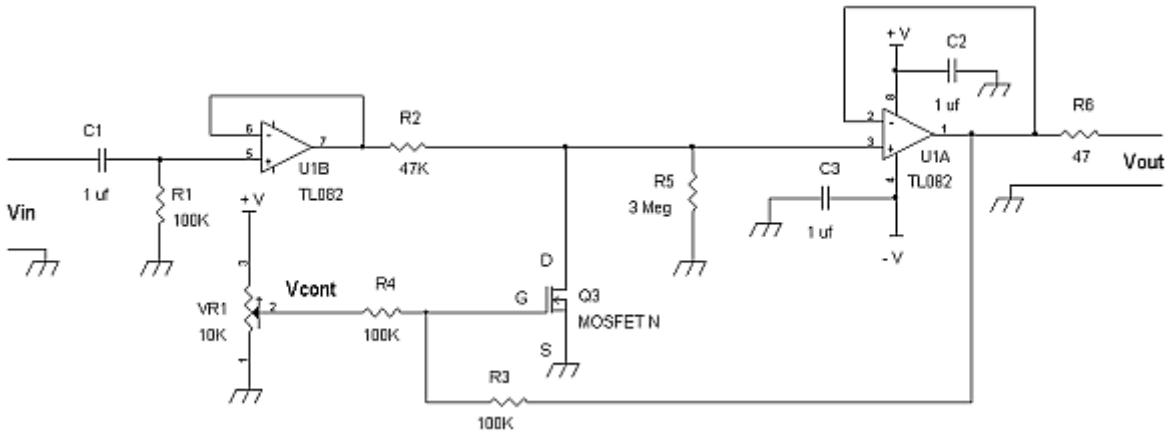

Figure AP-A-1 A MOSFET voltage controlled resistance.

Voltage follower U1A provides *Vds* to the resistive divider network R3 and R4. Since R3 = R4, the MOSFET Q3's gate to source voltage receives half or 0.5 of *Vds*. DC control voltage Vcont also is fed

to Q3's gate via R3 and R4, that delivers half of its voltage to the gate.

So *Vgs* = (1/2)Vcont + (1/2)*Vds* in **Figure AP-A-1**.

Figure AP-A-2 shows an example of how well the distortion reduction works with an SD5000 series DMOS with the substrate voltage at – 4.5 volts DC via a 5.6KΩ series resistor to pin 2.

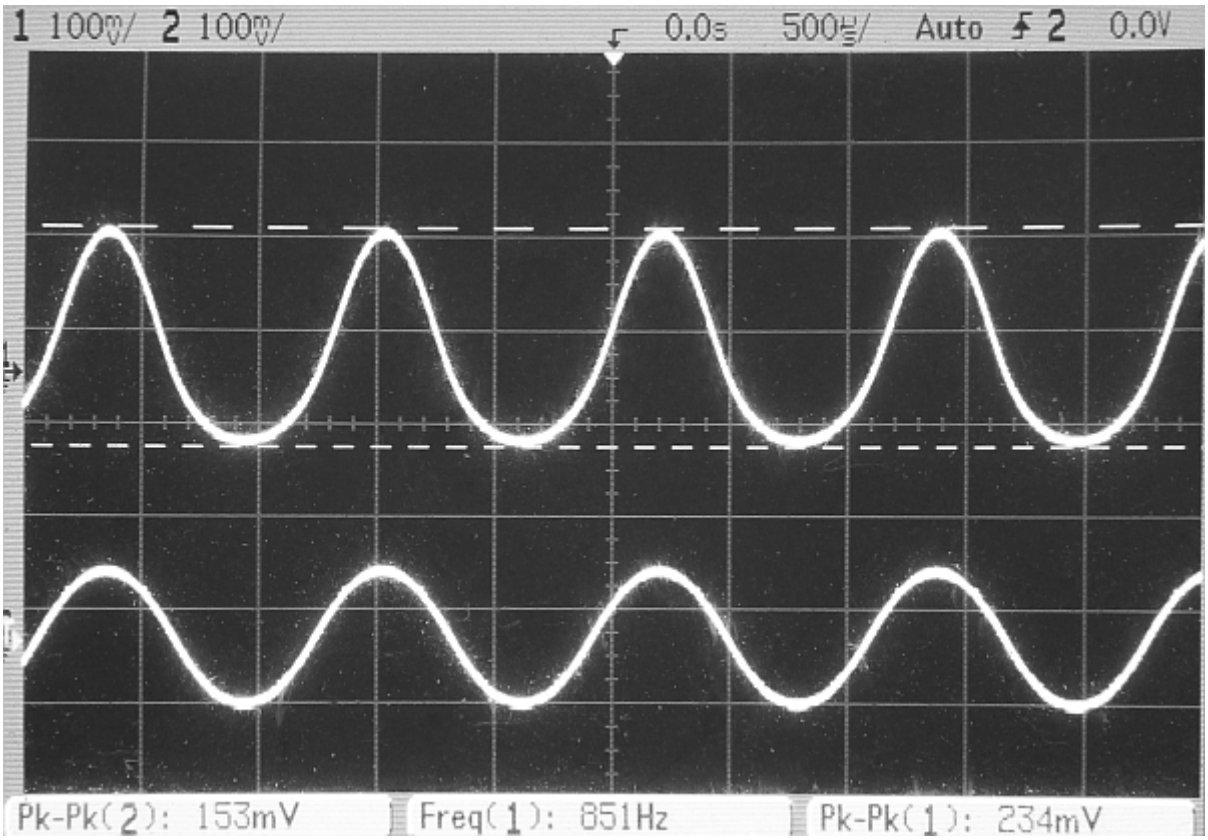

Figure AP-A-2 Top trace shows waveform without distortion reduction. Bottom trace shows cleaner waveform via the feedback network that reduces harmonic distortion.

As we can see the top trace shows a parabolic-like waveform that has about 35% second harmonic distortion. The bottom trace looks much closer to a sine wave and has about 2.5% second harmonic distortion. Vin = 500 mV peak-to-peak for an output of 234 mV peak-to-peak with distorted waveform (top trace), and 153 mV peak-to-peak output for the much less distorted waveform (bottom trace).

From **Figure AP-A-1**, the distorted waveform (top trace) was implemented by removing feedback resistor R3. The less distorted waveform shown on the bottom trace had R3 in the circuit.

Note also with distortion reduction on the bottom trace, the signal is slightly smaller due to the negative feedback via R3 and R4 that lowers the drain to source, R_{ds}, resistance.

Deriving equations for a gyrator circuit

Appendix B

Deriving equations for a gyrator (simulated inductor) circuit

Figure AP-B-1 below shows a lossy inductor that is equivalently implemented with a gyrator circuit

using two unity gain amplifiers Amp 1 and Amp 2.

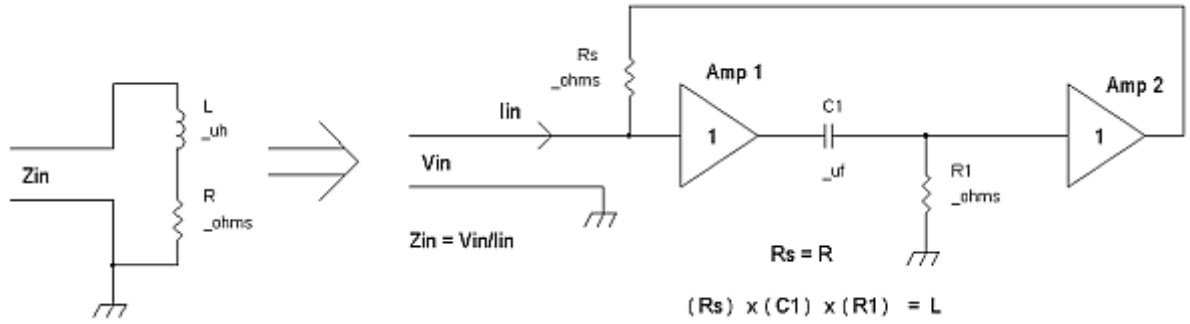

Fig AP-B-1 Lossy inductor on the left side with an equivalent active inductor (gyrator) on the right side.

A lossy inductor with a series resistor R and inductance L has an impedance

$Zin = R + j\omega L$, where $j = \sqrt{-1}$ and $j^2 = -1$

We can determine the gyrator's impedance by applying a test voltage at the input, Vin, and finding out its corresponding current flow, Iin. By taking the ratio, Vin/Iin, we can determine the gyrator's impedance that will be a function of the Rs, C1, and Rl.

The impedance of the capacitor = Zc = 1/ jωC1

Vin is connected to Amp 1's input. And because Amp 1 has unity gain, its output is also Vin, which drives a frequency dependent voltage divider, C1 and R1. For now we will just use Zc as the impedance of C1

Amp 2's input signal then is:

Vin [R1] / [R1 + Zc]

Because Amp 2's gain is unity, its output that drives the top terminal of Rs is also

Vin [R1] / [R1 + Zc]

We can now determine Iin via the current flowing through Rs since we know the voltages across Rs.

Iin = (Vin – Vin [R1] / [R1 + Zc])/Rs

Now we can find the gyrator's impedance, Zin, via Zin = Vin/Iin

Zin = Vin/Iin = Vin/(Vin – Vin [R1] / [R1 + Zc])/Rs

By factoring out Vin we have:

Zin = 1/ (1 - 1 [R1] / [R1 + Zc])/Rs

Multiply by 1 via by multiplying Rs at the numerator and denominator (e.g., $1 = R_S/R_S$) leads to:

Zin = Rs/ (1 - R1 / [R1 + Zc])

Note that 1 = [R1 + Zc] / [R1 + Zc]

Zin = Rs/ ([R1 + Zc] / [R1 + Zc] - R1 / [R1 + Zc])

Zin = Rs/[Zc] / [R1 + Zc]

Zin = [R1 + Zc] Rs / Zc

Recall Zc = (1/ jωC1)

Zin = [R1 + (1/ jωC1)] Rs / (1/ jωC1)

Multiply by 1 via multiplying numerator and denominator by jωC1

Zin = jωC1 [R1 + (1/ jωC1)] Rs = jωC1R1Rs + Rs

Zin = Rs + jωC1R1Rs

Since a lossy inductor has an impedance R + jωL, we can equate the real and imaginary parts:

R + jωL = Rs + jωC1R1Rs

R = Rs

jωL = jωC1R1Rs

Divide by jω on both sides we have

L = C1R1Rs = RsC1R1

Thus, the gyrator's inductance is the product of Rs, C1, and R1. Its equivalent series resistance is Rs.

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Ron Quan *is an author, design engineer, and inventor with over 75 US patents.*

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