A guide to using FETs for voltage controlled circuits, Part 3

Ron Quan - February 06, 2018

Read Part 1 and Part 2 of this series.

This article on FETs for voltage controlled circuits will cover FET modulator circuits and variable gain amplifier (VGA) design via reducing the drain-to-source voltage.

FET modulator circuits

In Part 1 and Part 2 of this series, a DC voltage from a potentiometer provided the control voltage. However, the control voltage can include a DC bias and an AC signal, which then provides a time varying gain signal such as an amplitude modulated signal.

If we replace the potentiometer VR1 with an AC signal plus DC bias signal in any of the previous Figures 3 to 17, the voltage controlled attenuators can become an amplitude modulator circuit instead. For example, in Figure 15 (P Channel MOSFET) if the input signal, Vin, is a high frequency carrier signal and VR1's signal, Vcont is replaced with a negative DC bias signal plus a low frequency sine wave signal, the output signal Vout will have an amplitude modulated carrier signal such as in **Figure 18**.

Note: The vertical axis denotes amplitude and horizontal axis denotes time in Figures 18, 19, 20, and 22.

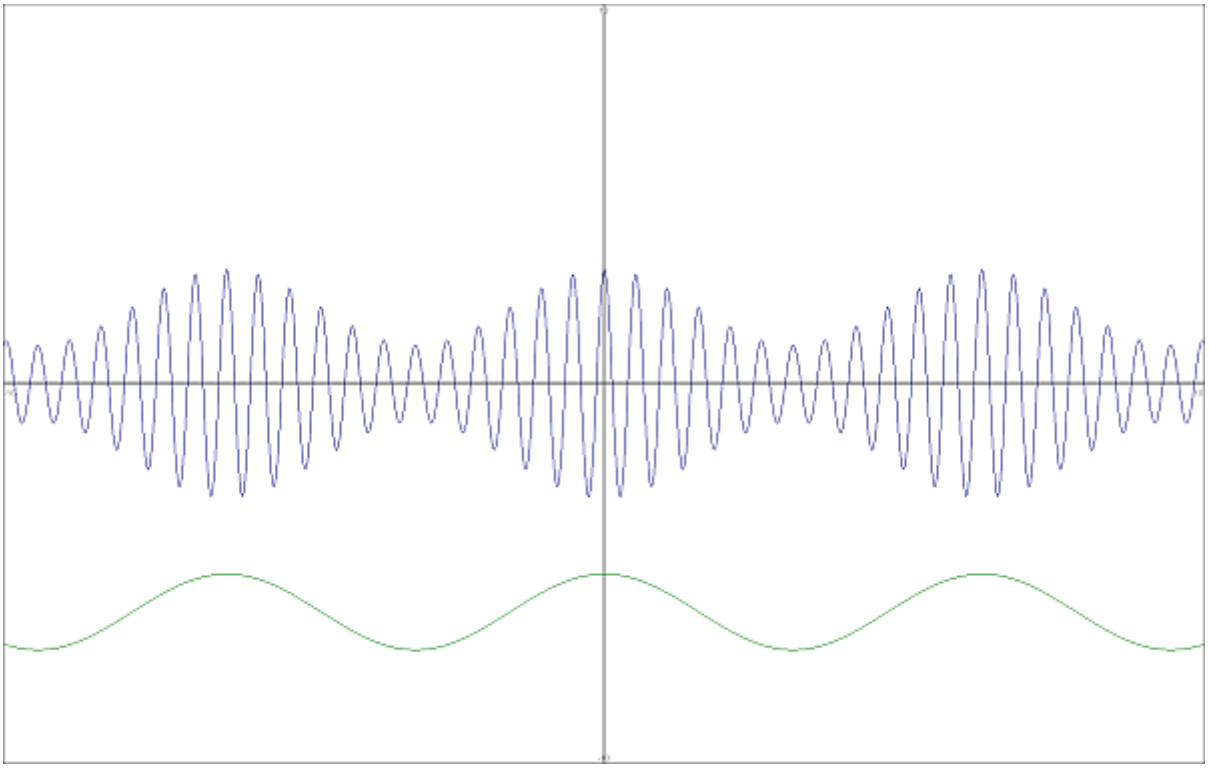

Figure 18 An amplitude modulated (high frequency) carrier signal and its low frequency sine wave modulating signal.

In Figure 15 with a P Channel MOSFET, as the gate voltage approaches 0 volts, the drain-to-source resistance increases, allowing the voltage-controlled attenuator to pass the input signal to its output with minimum attenuation. Note that in the positive peak of the sine wave, the amplitude modulation signal is at its greatest amplitude.

Conversely, if the P Channel MOSFET's gate voltage turns more negative, there is more conduction or less resistance across the drain and the source. Thus, there is a maximum attenuation that results in a minimum amplitude-modulated signal at the output. Now observe that the amplitude-modulated signal is at a minimum when the low frequency sine wave is at its negative peak.

We can describe the amplitude-modulated high frequency carrier, cos(2πft), signal as:

$$[1 + m(t)] \cos(2\pi ft) \quad = \text{AM signal} \qquad (12)$$

m(t) = modulating signal (e.g., a low frequency signal)

f = frequency of the "carrier" signal

Also, [1 + m(t)] ≥ 0 such that cos(2πft) is multiplied by a non-negative scalar or number to ensure that there is no phase reversal or inversion of the high frequency carrier signal.

For example, a standard broadcast amplitude modulation signal looks like **Figure 18** where the high frequency carrier signal always has an envelope that looks like the low frequency modulating signal.

In terms of standard types of amplitude modulation, there are other applications. These include a musical wavering effect for tremolo, and an automatic gain control amplifier for audio amplitude compression (not to be confused with data rate reduction via compression algorithms).

Now let's take a look another type of amplitude modulator, which is characterized by "pure" multiplication.

[m(t)] cos(2πft) = Double sideband suppressed carrier signal (13)

Figure 19 shows what a multiplied carrier signal or double sideband suppressed carrier amplitude modulated signal looks like.

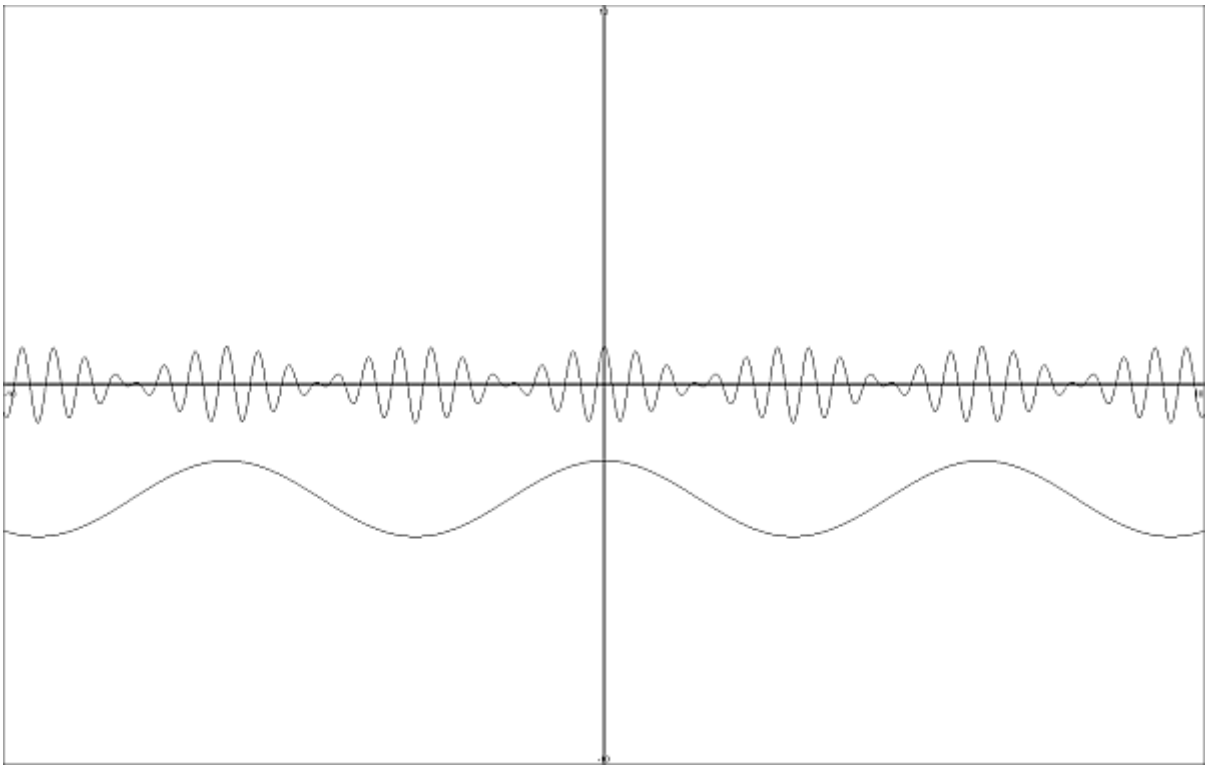

Figure 19 A multiplied carrier signal with its modulating sine wave below it.

Notice that the multiplied carrier signal does not exactly have a recognizable envelope like the one shown in Figure 18. **Figure 20** further shows the relationship of the carrier signal's phase.

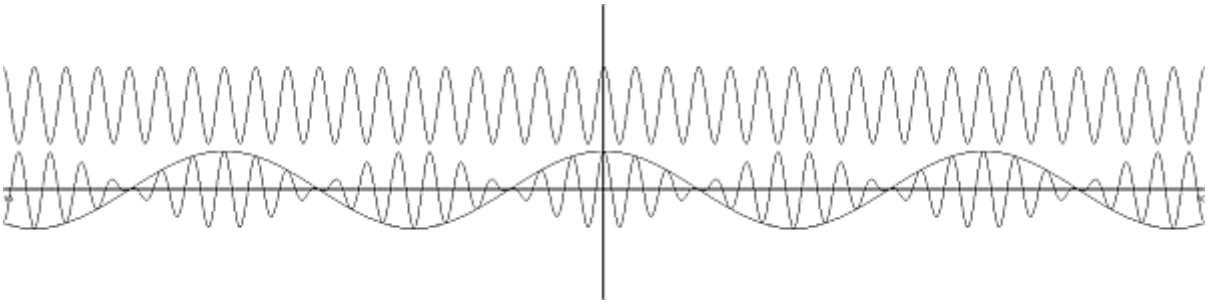

Figure 20 A constant amplitude carrier signal is above the multiplied carrier signal with its modulating low frequency sine wave superimposed.

If you notice very carefully the phase of the high frequency modulated carrier signal has its phase reversed when the low frequency modulating signal is at its negative cycle. At the origin axes, we see that the modulating signal is in the positive cycle, and the amplitude modulated waveform is in phase with the carrier signal above.

Making an analog multiplier circuit is a bit more complicated than a basic standard amplitude modulator circuit such as Figure 15 that includes a DC bias voltage with an AC modulating signal for Vcont. An analog multiplier circuit generally requires two basic standard modulator circuits with a twist … the second circuit requires an inversion of both its carrier and modulating signals.

Let's see how this is done:

[1 + m(t)] cos(2πft) = AM signal #1

For the second AM signal, let's invert the phase of both m(t) and carrier signal cos(2πft), such that:

[1 - m(t)](-1) cos(2πft) = AM signal #2 , but this is equivalent to:

[-1 + m(t)] cos(2πft) = AM signal #2

Let's now add the two signals:

AM signal # 1 + AM signal #2 = [1 + m(t)]cos(2πft) + [-1 + m(t)] cos(2πft)

= [1 + m(t) + -1 + m(t)] cos(2πft)

AM signal # 1 + AM signal #2 = [2m(t)] cos(2πft)]

From above, we now have a multiplier function or circuit when both AM signal #1 and AM signal #2 are added. **Figure 21** shows an example with two "standard" AM circuits summed to form a multiplier circuit.

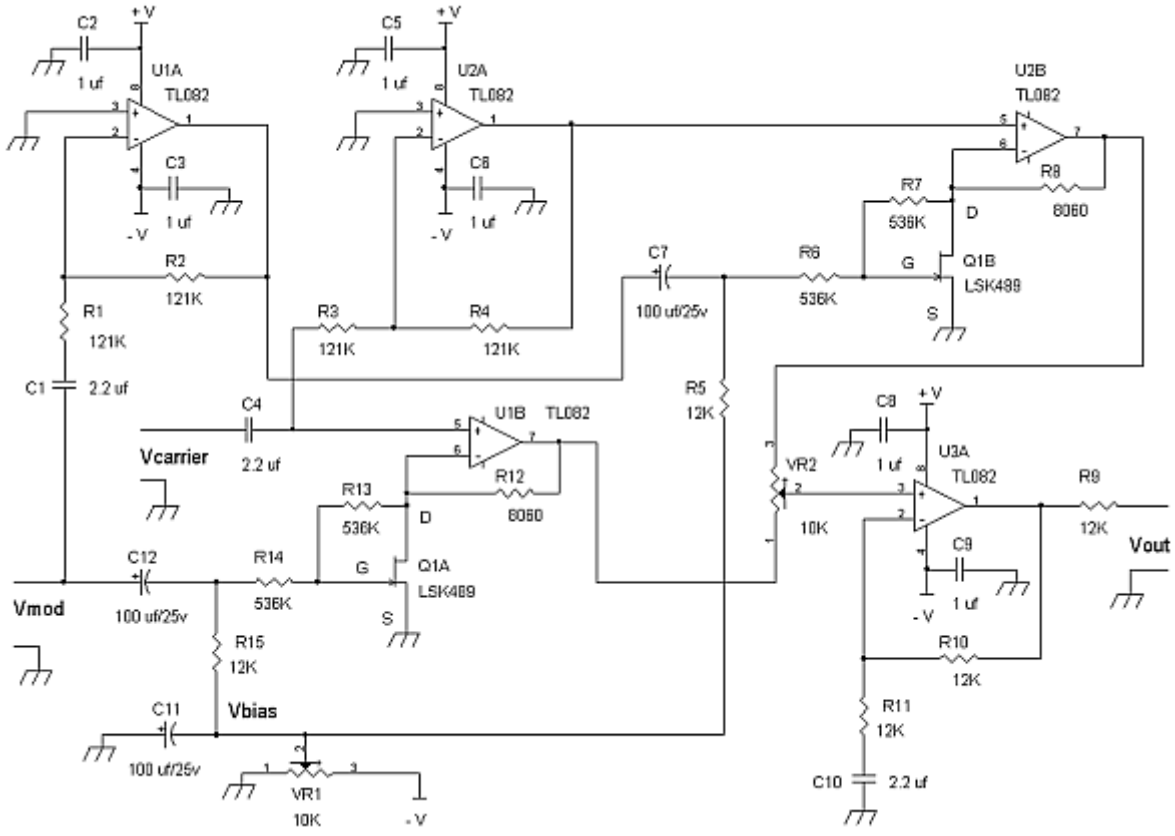

Figure 21 An example multiplier circuit using a dual N Channel JFET for generating AM double sideband suppressed carrier signals.

In **Figure 21**, the AM signal #1 is implemented by (N Channel JFET) voltage-controlled resistor Q1A and amplifier U1B. Q1A's drain-to-source resistance (Rds_Q1A) is lower when Vmod is at a positive peak compared to having its drain-to-source resistance being higher when Vmod is at a negative peak. Because with R13>> Rds_Q1A, U1B's closed loop gain = 1 + R12/Rds_Q1A, we see that the gain for the carrier signal increases when the modulation signal increases and vice versa. Signal output from U1B's pin 7 provides AM signal #1.

Implement AM signal #2

To implement AM signal #2, we need to invert the Vmod and Vcarrier signals. This is done via inverting amplifiers U1A and U2A. U1A inverts Vmod into the second modulator via voltage-controlled resistor Q1B connected to amplifier U2B. With the inverted Vcarrier signal into U2B's non-inverting input terminal, we have AM signal #2 from U2B's output terminal pin 7. Also note that R7>> Rds_Q1B.

The AM signals from both modulators are summed into VR2, which allow for matching the levels precisely to null out the carrier signal. To do this, turn Vmod off with the Vcarrier signal still on. Adjust VR2 until the carrier is at a minimum at Vout. Amplifier U3A has a gain of 2 to make up for the losses when summing the two signals at VR2.

VR1 sets the bias voltage for the FETs. In this example using an LSK489, the bias voltage was set to −3.25 volts DC, but you can try other bias settings. Also, a typical Vcarrier signal level was in the 200 mV peak-to-peak range, and a typical Vmod maximum level was about 550 mV peak-to-peak.

With TL082 op amps, the carrier frequencies should be < 100 kHz.

If higher carrier frequencies are used, the op amps can be changed to high speed ones such as the AD827 or LT1632. But be careful about layout when working with high frequency circuits. **Figure 22** shows the Vmod and Vout, where Vcarrier ~ 200 mV peak-to-peak and where Vmod ~ 180 mV peak-to-peak.

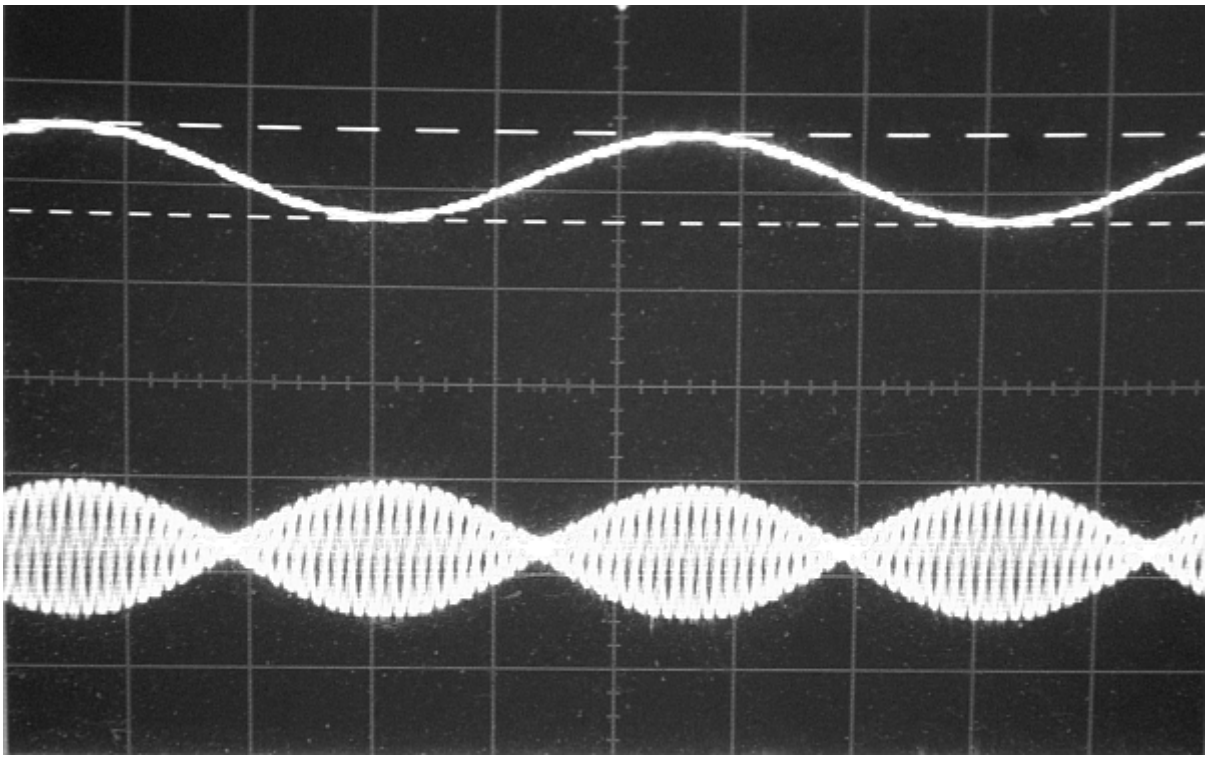

Figure 22 Waveforms Vmod and Vout from Figure 21.

FETs can also be configured as active multipliers. JFETs or MOSFETs can be used to build an analog balanced multiplier. For example, **Figure 23** is essentially a MOSFET version of the bipolar transistor MC1496 multiplier.

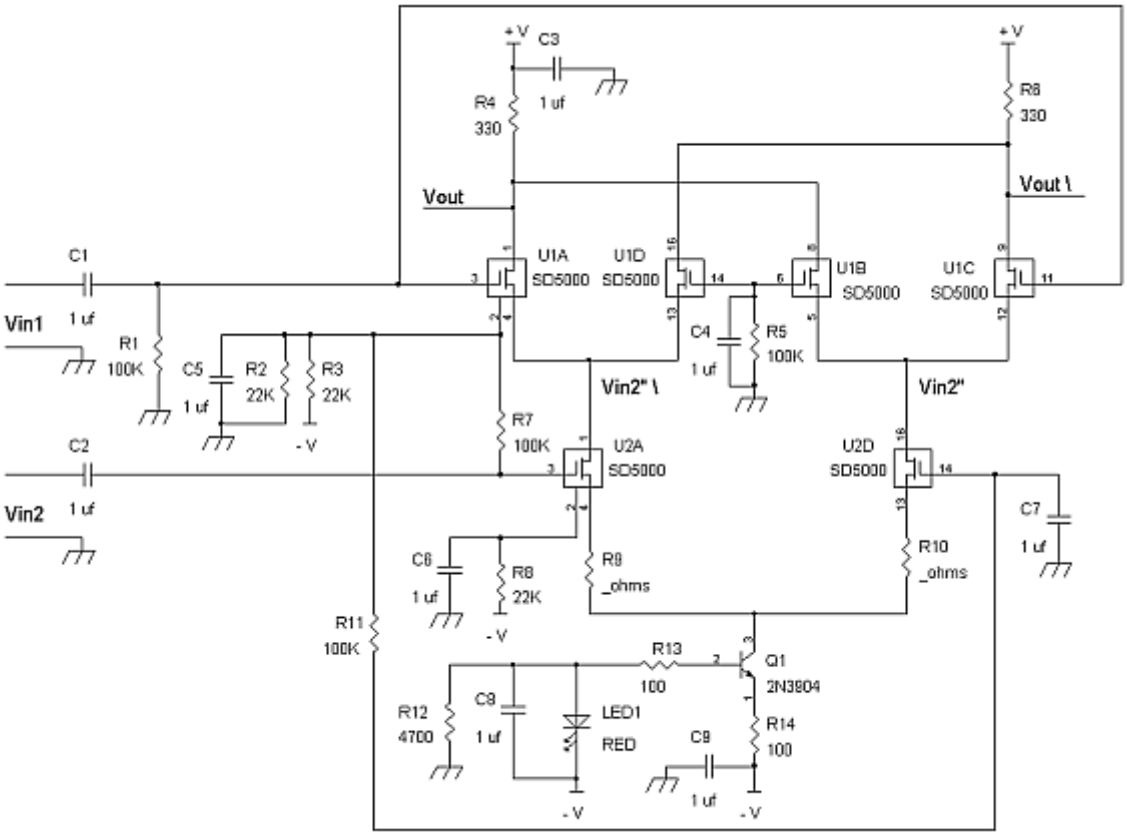

Figure 23 An FET version of the MC1496 balanced mixer circuit.

This circuit includes matched quad DMOS transistors for the upper differential pairs, U1A, U1D, and U1B, U1C. A second set of matched DMOS transistors form another differential pair on the both with U2A and U2D. Finally, we have a constant current source Q1, which is biased to about 10 mA DC, with about 1 volt DC across R14, 100Ω. Note: The supply voltages may be +/− 9 volts.

Using FETs for an analog multiplier in radio frequency (RF) applications has some advantages when the mixer's output is band-pass filtered to provide an intermediate frequency (IF) signal. Some advantages are:

1) High impedance at both Vin1 and Vin2 input terminals. This allows for using RF matching networks with a higher "step up" ratio.

2) FET's have higher dynamic range before limiting occurs compared to bipolar transistors.

3) Less sensitivity to external noise.

4) For DMOS transistors such as the SD5000, the high frequency cross-talk is minimized due to its low gate to drain capacitance, and more importantly the inputs' capacitances are low.

Local feedback resistors R9 and R10 lower the distortion on the bottom pair differential amplifier Q2A and Q2D. Typical R9 = R10 values can range from 0Ω to 1KΩ.

To understand this circuit, we can split it into two AM modulators. The first AM modulator includes U2A with U1A and U1D. The second AM modulator has U2D with U1B and U1C.

In a common configuration as a multiplier circuit, **Figure 23** has Vin2 as the modulating signal and Vin1 as the carrier signal.

We want to show that there are two AM modulators, where the second one has inverted modulating and carrier signals. The reason why is that we had shown that:

AM signal # 1 + AM signal #2 = [1 + m(t)]cos(2πft) + [1 - m(t)](-1) cos(2πft)

AM signal # 1 + AM signal #2 = 2[m(t)]cos(2πft)

For the first modulator with U2A, U1A and U1D, the bottom MOSFET, U2A provides an in-phase signal current from U2A's drain. That is if Vin2 goes positive or increases, U2A's drain current also increases. Now observe that U1A's drain current increases when Vin1 increases. So, in terms of drain currents both U2A's and U1A's drain currents are in phase with Vin2 and Vin1 respectively.

Now let's look at the second modulator's drain currents U2D and U1B in terms of Vin2 and Vin1. Note that the drains of U1B and U1A are summed or tied together to form an output current for Vout. If we first look at U1B, we see that it forms a differential pair U1B and U1C that is wired in opposite polarity compared to U1A and U1D relative to Vin1. That is, U1B's gate is grounded via R5 and C4. Put in another way, when Vin1 increases, it causes U1C's gate to source voltage (*Vgs*) to increase or become more positive. U1C's drain current then increases, but because the source of U1B is connected to U1C's source, which is going positive, U1B will start turning off. This means that U1B's current is decreasing when Vin1 is increasing.

Similarly, the bottom MOSFETs U2A and U2D has drain currents working in a complementary manner. Q1's collector supplies a constant current that is equal to the sum of the Q2A's and Q2D's drain currents. So, this means if one drain current increases, the other one decreases. For example, if the Q1 collector current is 10 mA, when Vin2 = 0, a no signal condition, then U2A's and U2D's drain current are both 5 mA. Now suppose U2A's drain current increases to 7 mA, then U2D's drain current decreases to 3 mA since the sum of the two drain currents is a constant 10 mA. Therefore, relative to an increasing Vin2, U2D's drain current is decreasing.

Relative to Vin2 and Vin1, the second modulator has an opposite phase relationship with its respective drain currents from U2D and U1B when compared to the first modulator.

Therefore, we indeed have two AM modulators, where the second one satisfies the constraint of providing opposite phase for both the modulator and carrier signal inputs, Vin2 and Vin1. With the drain currents of both modulators summed or added, Vout with load resistor R4 provides a voltage that includes the multiplication of Vin1 and Vin2.

VGA by reducing the drain-to-source voltage

VGA by reducing the drain-to-source voltage

If we closely look at an FET's characteristic drain current versus drain to source voltage curves, then we will notice that the transconductance, **ΔID/ΔVGS**, falls as the drain-to-source voltage decreases. See **Figure 24** where the change in gate-to-source voltage, **ΔVGS**, is fixed but the change in drain current, **ΔID**, varies depending on the drain to source voltage.

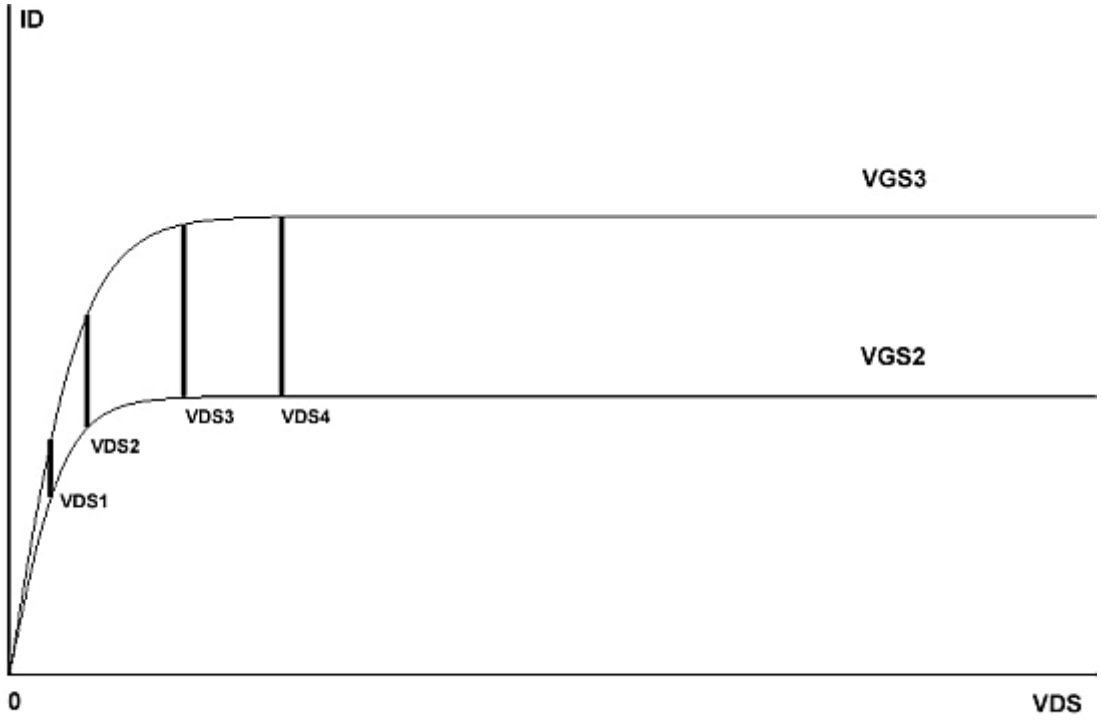

Figure 24 The I V characteristics of an FET where a smaller VDS results in smaller change in drain current ΔID (as denoted by the thick vertical segments above VDS1 and VDS2 compared to vertical segments above VDS3 and VDS4) for the same change in gate to source voltage.

With VDS1 < VDS4, note that ΔID @ VDS1 < ΔID @ VDS4.

Transconductance = ΔID/ΔVGS

And we can see that as the drain-to-source voltage, VDS → 0, ΔID → 0 also. This leads to

Transconductance = ΔID/ΔVGS → 0.

Thus, if we can change the drain-to-source voltage, then we can vary the transconductance, which is related to the gain.

One way to make a voltage controlled amplifier is to couple the drain to a low impedance point such as an inverting input of a transresistance op amp. By adjusting a control voltage at the non-inverting input of the op amp, the drain voltage is varied accordingly (**Figure 25**).

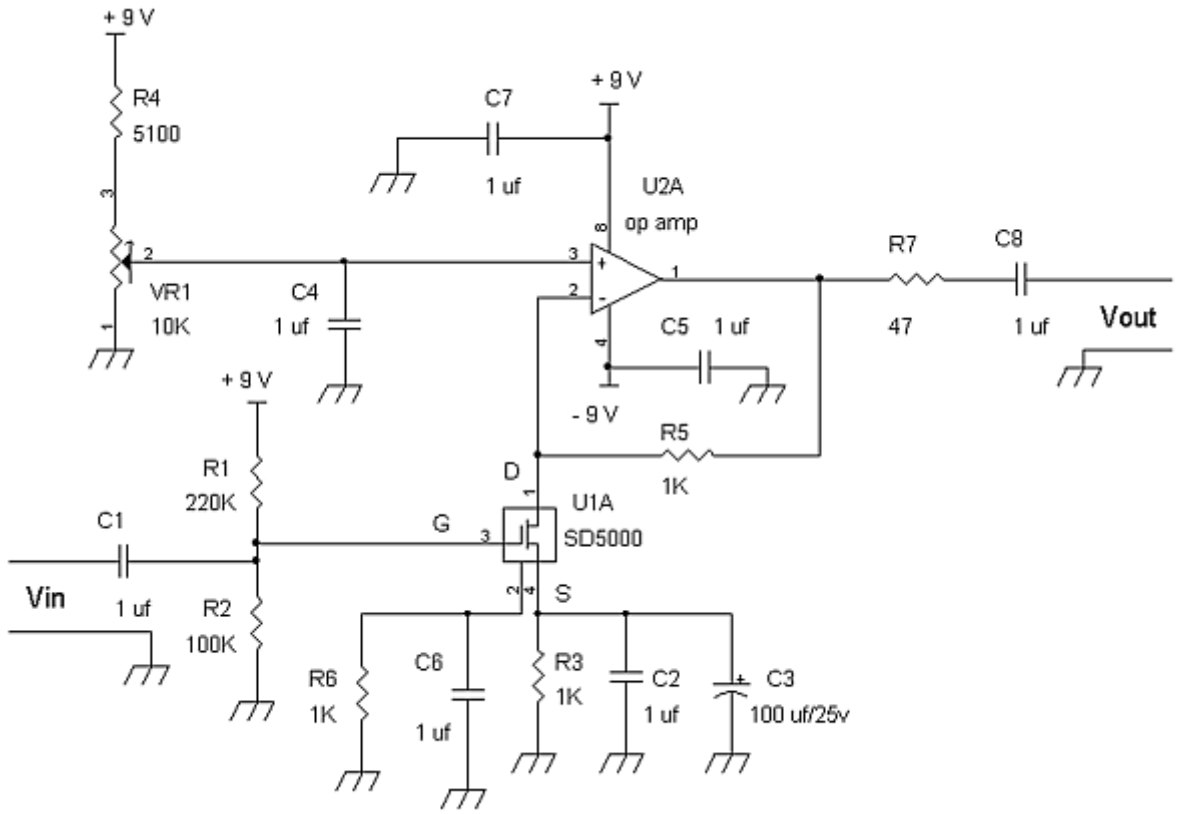

Figure 25 A voltage controlled amplifier by varying the drain voltage of U1A.

VR1 adjusts the control voltage at the non-inverting input of the op amp, U2A. Since the (control) voltage is approximately the same at U2A's inverting input terminal, the drain voltage follows the control voltage. By varying the control voltage at the drain of U1A, its transconductance varies, which in turn changes the magnitude of the gain, | Vout / Vin |.

For an enhancement mode FET shown in **Figure 25**, the gate to source voltage is forward biased, and thus the source voltage sits above ground. To turn off gain, we need to just set the voltage at VR1's slider to match the source voltage. Usually this is about +0.5 volts to about + 2.5 volts depending on the FET.

Figure 25 has an advantage that there is no Miller Multiplier capacitance effect since U1A's drain is coupled to a virtual AC ground via U2A's (-) input terminal.

For higher frequency performance, we can use the same principle and build a cascode circuit as shown in **Figure 26**.

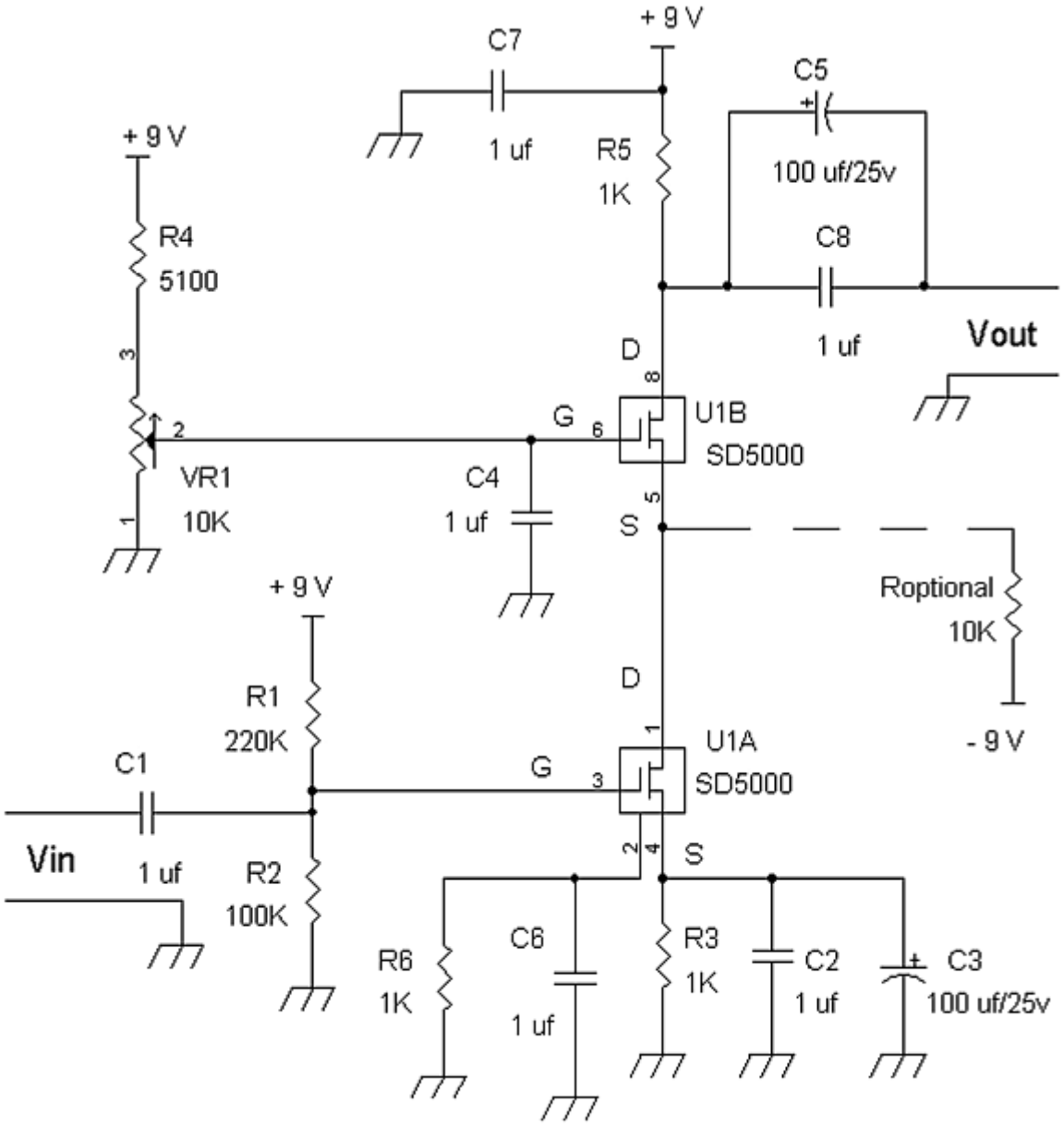

Figure 26 A cascode voltage controlled amplifier with enhancement FETs.

We have essentially the same circuit but have replaced the op amp with a second FET U1B, a common gate amplifier. Because the input resistance to U1B's source is low (e.g., $1/g_{m\_U1B}$), the voltage at U1A's drain is close to a constant voltage. You can also view that U1B's gate voltage is being source followed into U1A's drain.

An optional resistor, Roptional, is connected to U1B's source to ensure that it is always on. The actual value may vary, but about 1 mA quiescent source current for U1B is a starting point.

Because this circuit is a cascode amplifier, the Miller capacitance multiplier effect is minimized and this circuit is ideal for RF applications. For example, it can be used as part of an RF automatic or manual gain amplifier. Also, more than one of these can be cascaded.

VR1 may be replaced with an AGC (automatic gain control) voltage source. C4 can have a lower value such as 0.1 uf if faster AGC action is required.

Now let's look at a JFET approach in **Figure 27**.

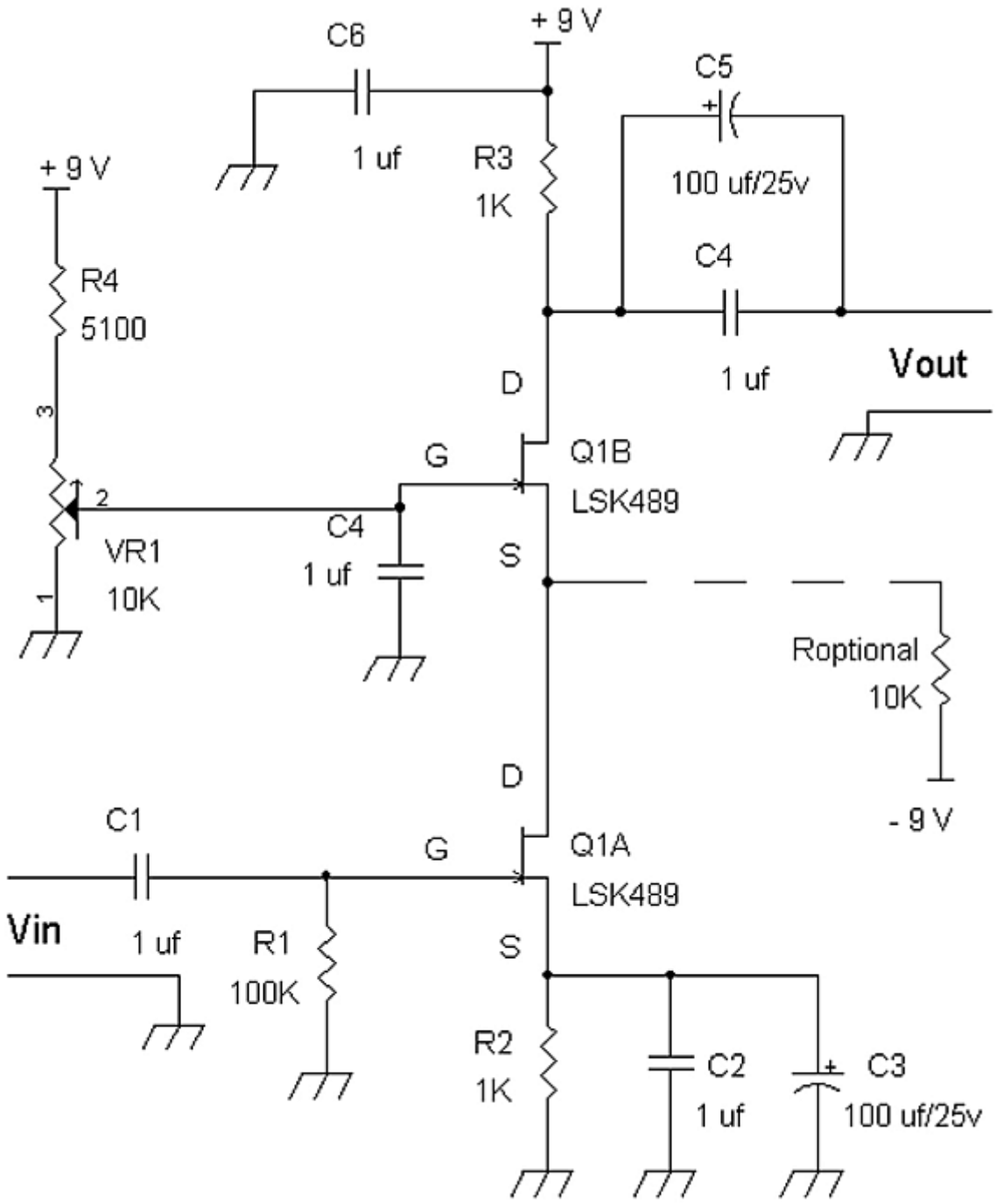

Figure 27 A cascode JFET VCA

Because the JFETs are depletion mode devices, it may not be possible to reduce the gain to zero even if the Q1B's gate voltage is zero. The reason is that Q1B's source voltage inherently will be a positive voltage with respect to its gate voltage. As a result of this, the control range may only be limited to about 20 dB or 30 dB that does not completely reduce the gain to zero. Recall that Q1B's source voltage must be low enough such that Q1A's drain-to-source voltage is zero volts for zero gain.

To better ensure that the gain can be reduced to zero, Q1B may be substituted with an enhancement MOSFET, or a bipolar device (e.g., 2N4124 where the base → gate, emitter → source, and collector → drain of Q1B).

However, if JFETs are used, one can add a level-shifting voltage source as shown in **Figure 28** to

ensure zero volts across the drain and source of the bottom JFET, Q1A when VR1 is adjusted to a low voltage.

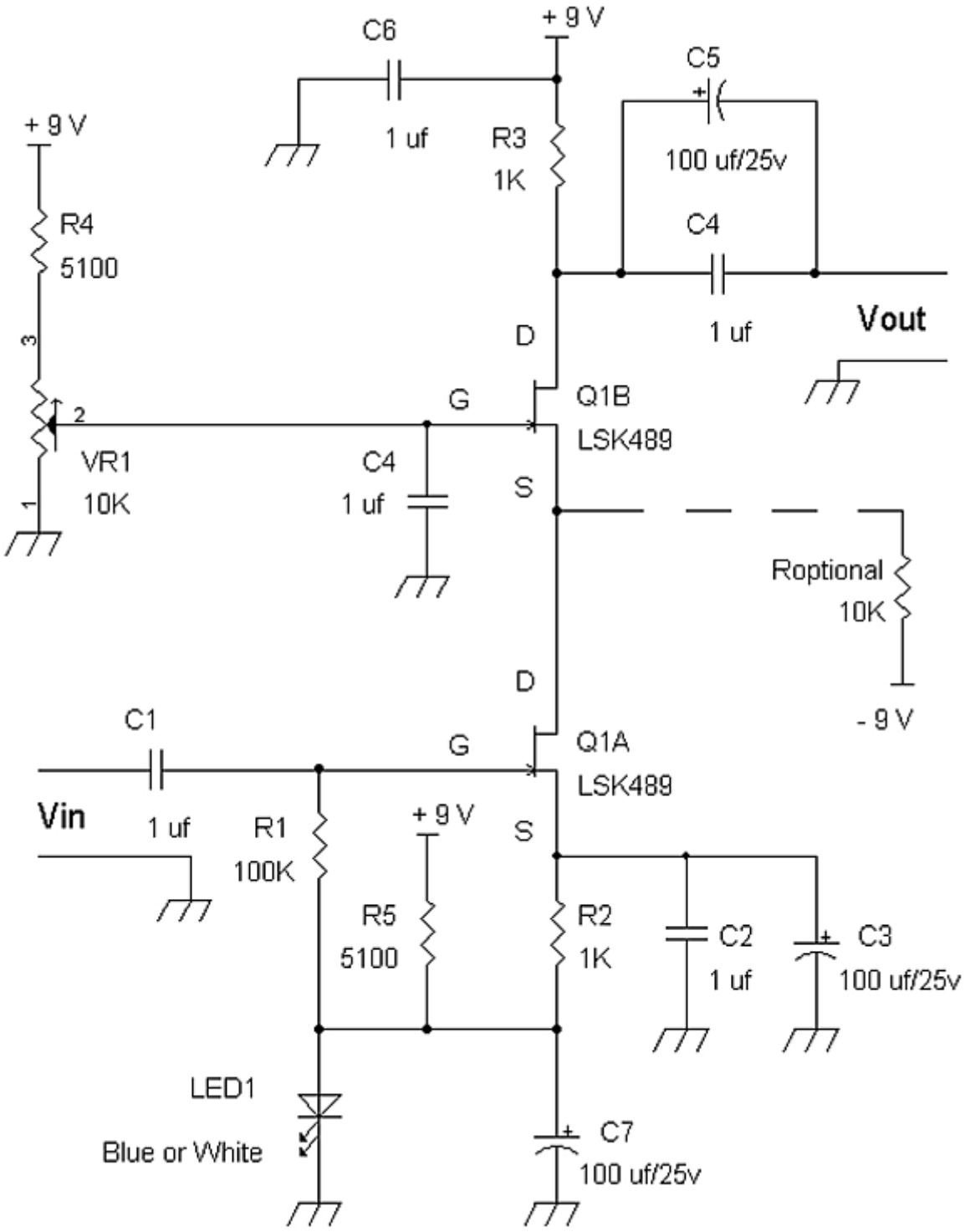

Figure 28 LED1 provides a DC level shifting voltage source to ensure that the gain can be reduced to zero.

By adding a positive bias voltage via LED1 to Q1A's source resistor, R2, the drain and source voltages referenced to ground for Q1A are shifted up. For example, if the voltage drop across R2 is about 1 volt, then Q1A's source voltage is about 3.7 volts, given a blue or white LED turns on at about 2.7 volts. This means if Q1A's drain voltage is set to 3.7 volts, the gain will go to zero.

We can now more easily set Q1B's source voltage to +3.7 volts such that Q1A's drain to source voltage → 0 volts.

Note: In Figures 25-28, VR1's voltage at the slider can be replaced with a modulating signal. This will provide a form of amplitude modulation on Vin. The modulating signal can be a used as an RF mixing signal to provide an IF signal. The load resistor R3 may be replaced with an IF band pass filter such as a parallel LC filter.

In Part 4 of this five-part series, we will discuss musical effects phasing circuits and musical effects with variable frequency gyrator bandpass filters.

Ron Quan is an author, design engineer, and inventor with over 75 US patents.

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