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**NORTH SOUTH UNIVERSITY**DEPARTMENT OF ELECTRICAL & COMPUTER ENGINEERING

**Assignment-5**

**Summer 2024**

**CSE332:** [Computer Organization and Architecture](https://northsouth.instructure.com/courses/37159)

**Section: 1**

**Group: 1**

|  |  |  |  |
| --- | --- | --- | --- |
| Name | ID | Work | Contributions |
| Labiba Faiza Karim | 2221454042 | OS incorporation, MIPS\_SCR and related codes (control.v, rom.v, etc,) and wave form | 25% |
| Arefin Amin | 2221766642 | Assembler and incorporated all codes together, MIPS\_SCR and wave form | 25% |
| Fatema Tabassum Elma | 2222904042 | OS(min, max, mean) | 20% |
| Ratul Hasan Ankon | 2222568042 | JAL, JR implementation | 15% |
| Raiyan Ahmed | 2221931042 | CPU\_mod, CPU\_tb | 15% |

**MIPS CPU and OS Project Report**

**Introduction**

This report documents the design and implementation of a custom MIPS-based CPU and operating system (OS) for the CSE332 course project. The goal was to design a working CPU, develop an assembler for instruction conversion, and simulate the design to demonstrate its functionality. The project adheres to the MIPS ISA (Instruction Set Architecture), ensuring clarity and simplicity while maintaining robust performance.

**ISA Design**

**Number of Operands**

Three operands for flexibility, following the MIPS approach. This allows instructions like ADD R1, R2, R3 to operate on three registers. Additionally, two-operand instructions like SW R1, R2 are included for memory operations.

**Types of Operands**

* Registers: For fast operations.
* Memory access: For load/store instructions.

**Operations**

**Arithmetic Operations**

* ADD: Add two registers and store the result in a third register.
* SUB: Subtract one register from another.
* MUL: Multiply two registers.
* DIV: Divide one register by another.

**Logical Operations**

* AND: Bitwise AND of two registers.
* OR: Bitwise OR of two registers.
* NOT: Bitwise NOT of a single register.
* XOR: Bitwise XOR of two registers.

**Branching Operations**

* BEQ: Branch if two registers are equal.
* BNE: Branch if two registers are not equal.
* JUMP: Jump to a specified address.

**Memory Access Operations**

* LW: Load a word from memory into a register.
* SW: Store a word from a register into memory.

**Miscellaneous Operations**

* NOP: No operation (useful for pipeline stalls).

**Instruction Formats**

1. **R-Type (Register)**
   * Used for arithmetic and logical operations.
   * Format: OPCODE (6 bits) | RS (5 bits) | RT (5 bits) | RD (5 bits) | SHAMT (5 bits) | FUNCT (6 bits)
   * Example: ADD R1, R2, R3 (Opcode: 0, Funct: 32).
2. **I-Type (Immediate)**
   * Used for memory access and immediate operations.
   * Format: OPCODE (6 bits) | RS (5 bits) | RT (5 bits) | IMMEDIATE (16 bits)
   * Example: LW R1, 100(R2) (Opcode: 35).
3. **J-Type (Jump)**
   * Used for jump instructions.
   * Format: OPCODE (6 bits) | ADDRESS (26 bits)
   * Example: J 0x1000 (Opcode: 2).

**Register Table**

|  |  |  |
| --- | --- | --- |
| Register Name | Purpose | Notes |
| $zero | Always 0 | Constant register |
| $t0-$t7 | Temporary Registers | General-purpose registers |
| $s0-$s7 | Saved Registers | Preserved across calls |
| $ra | Return Address | Stores return address |
| $sp | Stack Pointer | Points to stack memory |

**Design and Implementation**

1. Mips Code for the OS:

**Min.asm ----**

.data

array: .word 5

size: .word 5

.text

.globl main

main:

la $t0, array #loading the base address of the array

lw $t1, size #loading the base size of the array

lw $t2, 0($t0) #first element of the array

move $t3, $t2

li $t6, 0 #index

loop\_min:

beq $t6, $t1, end\_min #if index == size of array, the loop will end

lw $t7, 0($t0) #loading the current array element into $t7

blt $t7, $t3, update\_min #undating the min value

j skip\_min

update\_min:

move $t3, $t7 #keeping the min value in $t3

skip\_min: #moving to the next element

addi $t6, $t6, 1 #index += 1

addi $t0, $t0, 4 #moving to the next word in memory

j loop\_min

end\_min: #storing the min value to $a0 for output

move $a0, $t3

li $v0, 10 #syscall to exit

syscall

**Max.asm ---**

.data

array: .word 5

size: .word 5

.text

.globl main

main:

la $t0, array #loading the base address of the array

lw $t1, size #loading the base size of the array

lw $t2, 0($t0) #first element of the array

move $t4, $t2

li $t6, 0 #index

loop\_max:

beq $t6, $t1, end\_max #if index == size of array, the loop will end

lw $t7, 0($t0) #loading the current array element into $t7

bgt $t7, $t4, update\_max #undating the max value

j skip\_max

update\_max:

move $t4, $t7 #keeping the max value in $t3

skip\_max: #moving to the next element

addi $t6, $t6, 1 #index += 1

addi $t0, $t0, 4 #moving to the next word in memory

j loop\_max

end\_max: #storing the max value to $a0 for output

move $a0, $t4

li $v0, 10 #syscall to exit

syscall

**Mean.asm ---**

.data

array: .word 5

size: .word 5

.text

.globl main

main:

la $t0, array #loading the base address of the array

lw $t1, size #loading the base size of the array

move $t5, $zero #initializing sum to 0

li $t6, 0 #index

loop\_mean:

beq $t6, $t1, end\_mean #if index == size of array, the loop will end

lw $t7, 0($t0) #loading the current array element into $t7

add $t5, $t5, $t7 #sum += next\_value

addi $t6, $t6, 1 #index += 1

addi $t0, $t0, 4 #moving to the next word in memory

j loop\_mean

end\_mean: #calculating the mean: sum/size

div $t5, $t1 #mean = sum/size = $t5/$t1

mflo $a0 #storing the mean value to $a0 for output

li $v0, 10 #syscall to exit

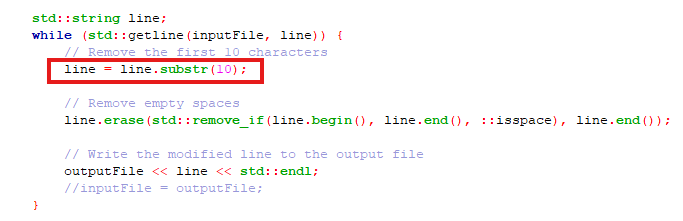
syscall

2. Assembler Development

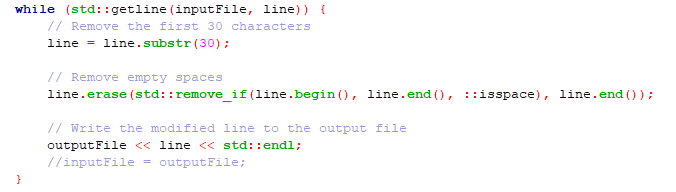
An assembler was developed to convert assembly language instructions into binary instructions readable by the CPU.

To make show only the binary values in the output, we had to change the finalassembler.cpp file.

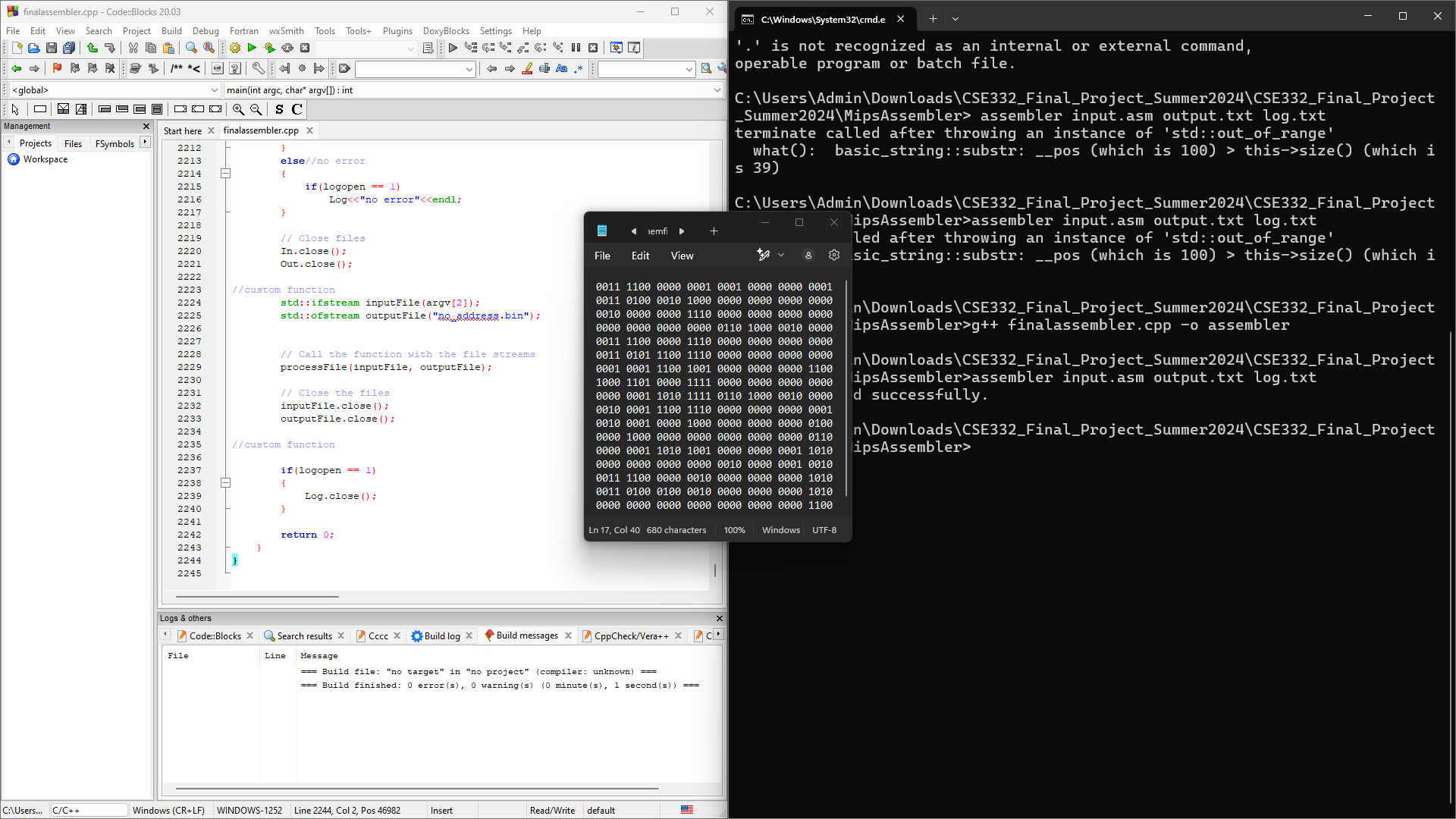
By changing this part of the code ---



to this ----



We got the expected binary values in the output.txt file

* Screenshot:
* 

To see the output here are the command we used.—

* g++ finalassembler.cpp -o assembler
* assembler input.asm output.txt log.txt

We will see the compilation error or the message in the log.txt file and we will get the expected binary values in the output.txt file.

2. CPU Simulation in ModelSim

The CPU design was simulated using ModelSim to verify its correctness and functionality.

Here are the Verilog codes we used / modified for the simulation----

CPU\_mod.v

`timescale 1ns/1ns

module CPU\_mod(

input clk,

input reset,

output [31:0] PC,

output [31:0] Instr,

output [31:0] ALUResult,

output ZeroFlag

);

// Internal wires

wire [31:0] ReadData, datatwo;

wire MemWrite, MemtoReg, ALUSrc, RegDst, RegWrite, Jump, PCSrc;

wire [3:0] ALUControl;

// Instantiate the control unit

Controlunit control\_unit (

.Opcode(Instr[31:26]),

.Func(Instr[5:0]),

.Zero(ZeroFlag),

.MemtoReg(MemtoReg),

.MemWrite(MemWrite),

.ALUSrc(ALUSrc),

.RegDst(RegDst),

.RegWrite(RegWrite),

.Jump(Jump),

.PCSrc(PCSrc),

.ALUControl(ALUControl)

);

// Instantiate the datapath

Datapath datapath (

.clk(clk),

.reset(reset),

.RegDst(RegDst),

.RegWrite(RegWrite),

.ALUSrc(ALUSrc),

.Jump(Jump),

.MemtoReg(MemtoReg),

.PCSrc(PCSrc),

.ALUControl(ALUControl),

.ReadData(ReadData),

.Instr(Instr),

.PC(PC),

.ZeroFlag(ZeroFlag),

.datatwo(datatwo),

.ALUResult(ALUResult)

);

// Instantiate instruction memory

InstMemory inst\_mem (

.a(PC[7:2]), // Address

.rd(Instr) // Read Data

);

// Instantiate data memory

DataMemory data\_mem (

.clk(clk),

.we(MemWrite),

.a(ALUResult),

.wd(datatwo),

.rd(ReadData)

);

Endmodule

**CPU\_tb.v ---**

`timescale 1ns/1ns

module CPU\_tb;

// Inputs

reg clk;

reg reset;

// Outputs

wire [31:0] PC;

wire [31:0] Instr;

wire [31:0] ALUResult;

wire ZeroFlag;

// Instantiate the CPU module

CPU\_mod uut (

.clk(clk),

.reset(reset),

.PC(PC),

.Instr(Instr),

.ALUResult(ALUResult),

.ZeroFlag(ZeroFlag)

);

// Clock generation

initial begin

clk = 0;

forever #5 clk = ~clk; // 10 ns clock period

end

// Test procedure

initial begin

// Dump waveforms

$dumpfile("CPU\_tb.vcd"); // VCD file for waveform

$dumpvars(0, CPU\_tb);

// Initialize reset

reset = 1;

#10;

reset = 0;

// Let the CPU run for some cycles

#1000; // Adjust based on the number of cycles you want to observe

// Finish simulation

$finish;

end

endmodule

**Instruction\_Memory.v**

`timescale 1ns/1ps

module InstructionMemory (

input [31:0] address,

output [31:0] instruction

);

reg [31:0] memory [0:255];

initial begin

$readmemb("instructions.mem", memory);

end

assign instruction = memory[address >> 2];

// Dump instruction memory contents at the end of the simulation

integer j;

initial begin

#1000; // Wait for the simulation to finish

$display("Final Instruction Memory Contents:");

for (j = 0; j < 256; j = j + 1) begin

$display("Memory[%0d] = %h", j, memory[j]);

end

end

endmodule

**Register\_File.v ----**

`timescale 1ns/1ps

module RegisterFile (

input clk,

input regWrite,

input [4:0] readReg1,

input [4:0] readReg2,

input [4:0] writeReg,

input [31:0] writeData,

output [31:0] readData1,

output [31:0] readData2

);

reg [31:0] registers [31:0];

assign readData1 = registers[readReg1];

assign readData2 = registers[readReg2];

always @(posedge clk) begin

if (regWrite)

registers[writeReg] <= writeData;

end

/\*

// Monitor and dump register contents to a file after simulation

initial begin

$dumpfile("register\_dump.vcd");

$dumpvars(0, RegisterFile);

end

\*/

// Dump register contents at the end of the simulation

integer i;

initial begin

#1000; // Wait for the simulation to finish

$display("Final Register File Contents:");

for (i = 0; i < 32; i = i + 1) begin

$display("Register[%0d] = %h", i, registers[i]);

end

end

endmodule

**MIPS\_SCP.v ---**

`timescale 1ns/1ns

module MIPS\_SCP (

input clk,

input reset,

output [31:0] PC, // Program Counter output

output [31:0] Instr // Instruction output

);

// Internal signals

wire [31:0] pc\_next;

wire [31:0] pc\_current;

wire [31:0] instruction;

// Instantiate PC register

flopr\_param #(32) pc\_register (

.clk(clk),

.reset(reset),

.d(pc\_next),

.q(pc\_current)

);

// Instantiate Instruction ROM

rom instruction\_memory (

.addr(pc\_current),

.data(instruction)

);

// Assign outputs

assign PC = pc\_current; // Expose Program Counter

assign Instr = instruction; // Expose fetched instruction

// Simple logic to compute next PC (can be replaced with actual control logic)

assign pc\_next = pc\_current + 4;

endmodule

**MIPS\_SCP\_tb.v ----**

`timescale 1ns/1ns

module MIPS\_SCP\_tb();

// Inputs to MUT (MIPS\_SCP)

reg clk;

reg reset;

// Outputs from MUT

wire [31:0] PC;

wire [31:0] Instr;

// Instantiate the MIPS\_SCP module

MIPS\_SCP mips\_inst (

.clk(clk),

.reset(reset),

.PC(PC),

.Instr(Instr)

);

// Clock generation

initial begin

clk = 0;

forever #5 clk = ~clk; // Generate a clock with 10ns period

end

// Test stimulus

initial begin

reset = 1; // Apply reset

#10; // Hold reset for 10ns

reset = 0; // De-assert reset

// Simulation end after 200ns

#200;

$stop;

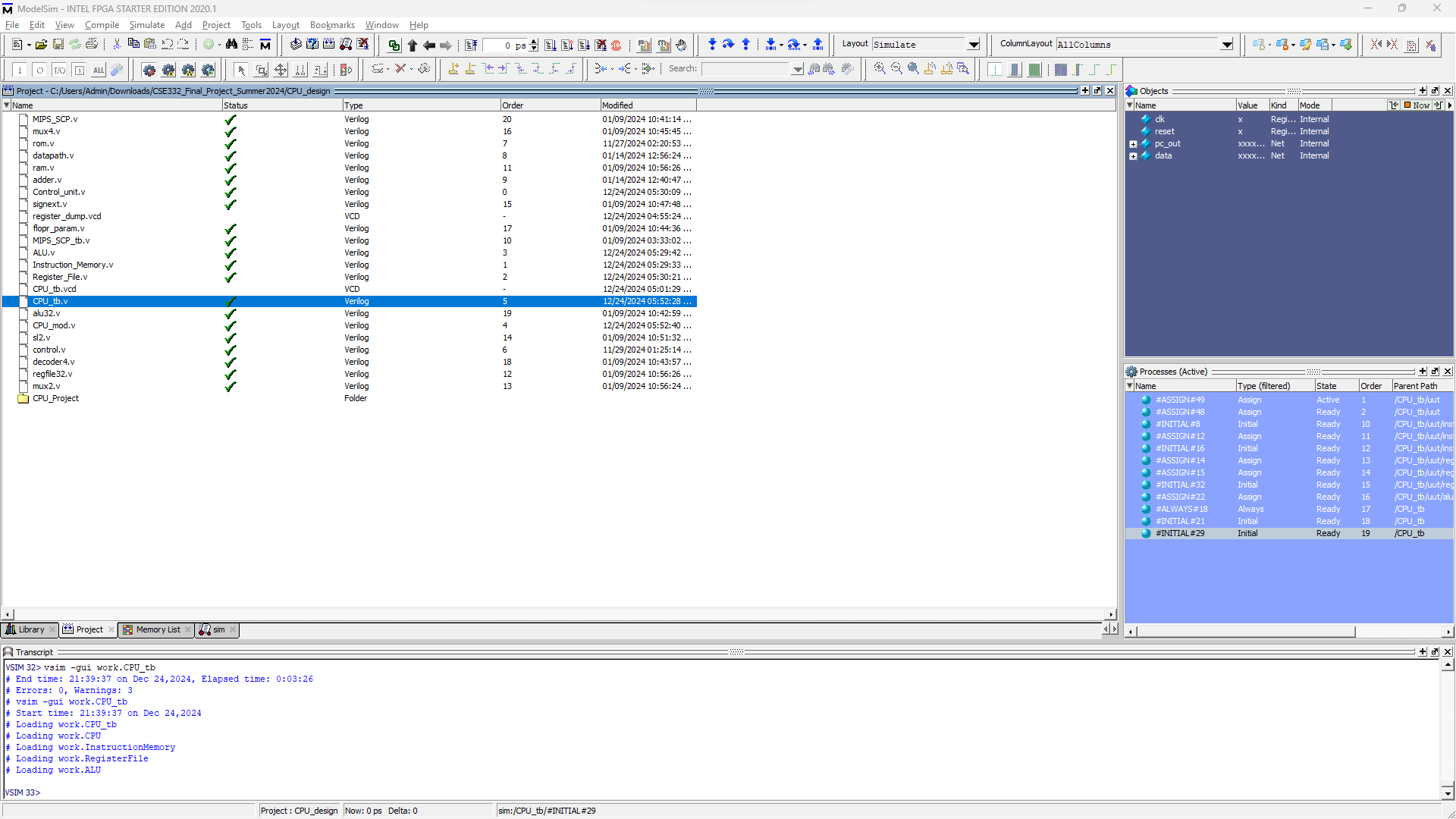
end

endmodule

to simulate the model we used the following commands ---

* vlog -work work "C:/Users/Admin/Downloads/CSE332\_Final\_Project\_Summer2024/Verilog/CPU\_tb.v"
* vsim -gui work.MIPS\_SCP\_tb

Screenshot:

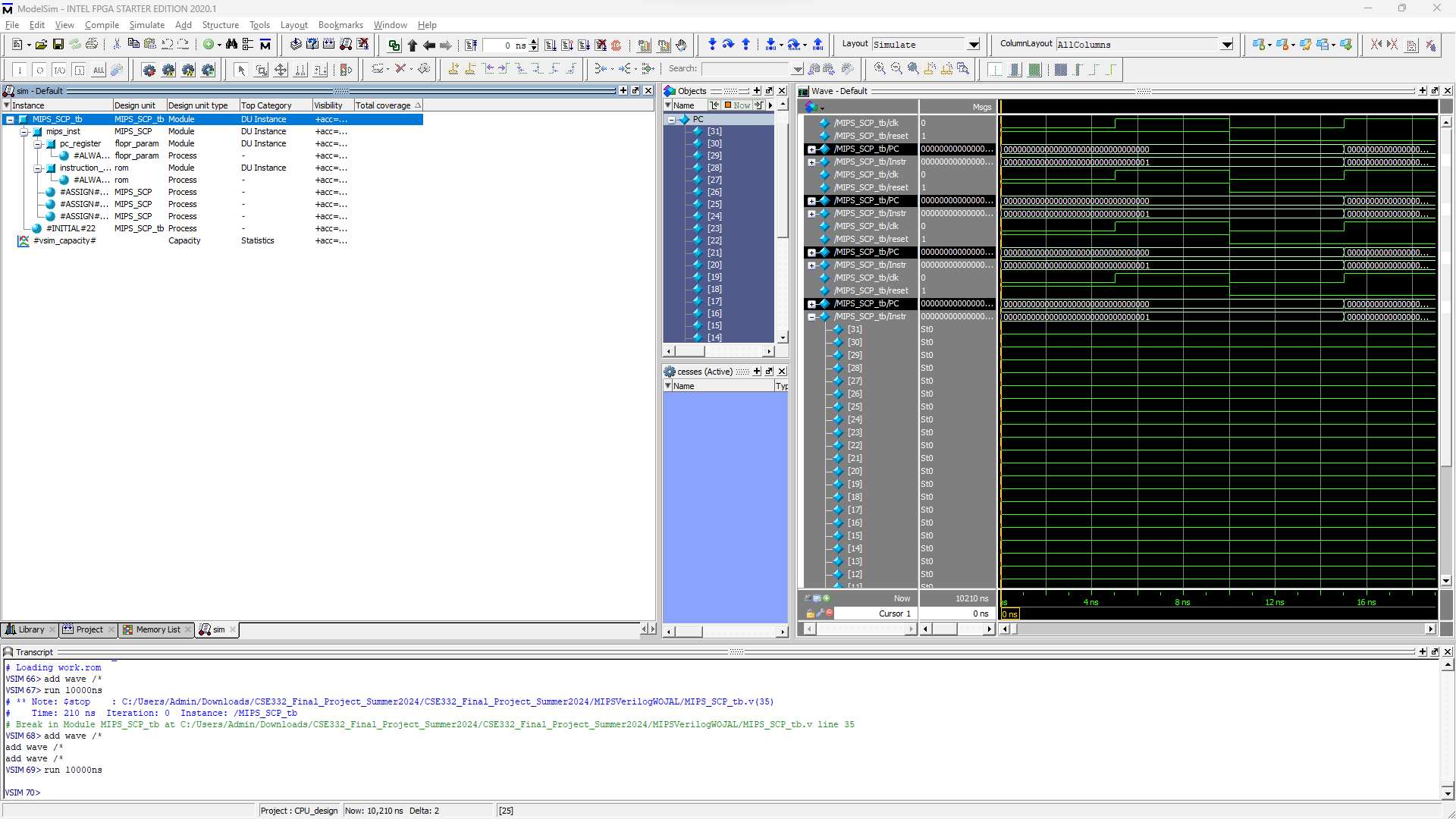


3. Waveform Analysis

Waveform analysis was performed to debug and verify signal behavior during execution.

To see the wave form in the modelSim we used the following commands ----

* add wave /\*
* run 1000ns
* Screenshot:



**Verilog Codes:**

As for the Verilog code we did change some of the existing files and created some of our own files in order to simulate the program.

**Benchmark Program:**

To test the CPU, the following benchmark programs were executed:

`timescale 1ns/1ps

module CPU\_tb;

reg clk;

reg reset;

wire [31:0] pc\_out;

wire [31:0] data;

// Instantiate the CPU

CPU uut (

.clk(clk), // Correct port name and connection

.reset(reset), // Correct port name and connection

.pc\_out(pc\_out), // Correct port name and connection

.data(data) // Correct port name and connection

);

// Clock generation

always #5 clk = ~clk;

// Stimulus

initial begin

clk = 0;

reset = 1;

#10 reset = 0;

#1000 $finish;

end

// Monitor Outputs

initial begin

$monitor("Time: %t | PC: %h | Data: %h", $time, pc\_out, data);

end

endmoduleScreenshot: [Add screenshots showing assembly program execution results here.]

**Results and Observations**

1. Instruction Conversion: The assembler correctly converted assembly instructions into binary, adhering to the MIPS instruction format.
2. Simulation Output: The ModelSim simulation validated the execution of instructions, as evident from the output and waveform analysis.
3. Waveform Behavior: The waveform confirmed proper synchronization of signals and data flow.

**Conclusion**

This project demonstrated the successful design and simulation of a custom MIPS-based CPU. By implementing an assembler, simulating the design, and verifying results with waveform analysis, the objectives were achieved.

**Citation:**

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[4] OpenAI, ChatGPT, "CPU Module Testbench," private communication, Dec. 2024.

[5] OpenAI, ChatGPT, "Verilog Simulation Warnings," private communication, Dec. 2024.

[6] OpenAI, ChatGPT, "View waveform in model sim" private communication, Dec. 2024.

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[13] Intel FPGA, "Introduction to ModelSim Simulation," [Online]. Available: <https://www.intel.com/content/www/us/en/software/programmable/quartus-prime/model-sim.html>. [Accessed: Dec. 24, 2024].

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