Lab01 hw 進階題

Problems (10%)

1. 為什麼要加入 blinky.xdc 這個 Constraint ?

> Hint、 Hint too

2. 承上題，若沒有加入這個 Constraint，可能會發生什麼事?

blinky.xdc

```
1  create_clock -period 8.000 -name sys_clk_pin -waveform {0.000 4.000} -add [get_ports clk]
2  create_generated_clock -name clk_div -divide_by 125000000 -source [get_ports clk] [get_pins div_0/clk_div_reg/Q];
```

■ create_generated_clock -name<generated clock name>
-source <master clock source pin or port>
-divide_by <div_factor> <pin_or_port>

(1) 時序約束，Clocks must be properly defined in order to get the maximum timing path coverage with the best accuracy.

The primary clock *sys_clk_pin* has a period of 8 ns. It is divided by 125000000 by the register *clk_div_reg* which drives other registers clock pin.
The corresponding generated clock is called *clk_div*.

#1 create_clock 定義的 primary clock waveforms 如下圖，

#2 generated clock waveforms 如下圖，

8*10^(-9)s*125000000=1s

(2) The Vivado IDE ignores all clock tree delays coming from cells located upstream from the point at which the primary clock is defined. If you define a primary clock on a pin in the middle of the design, **only part of its latency is used for timing analysis.**

This can be a problem if this clock communicates with other related clocks in the design, because the skew, and consequently the slack, value between the clocks can be inaccurate.