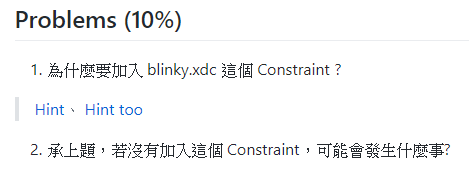
**Lab01 hw進階題**

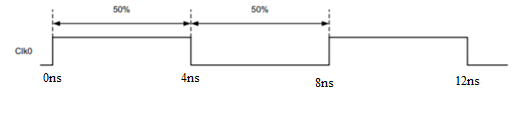


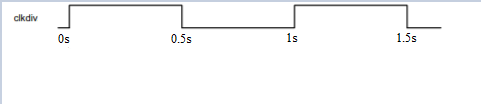
|  |
| --- |
| blinky.xdc     * create\_generated\_clock -name<generated clock name>   -source <master clock source pin or port>  -divide\_by <div\_factor> <pin\_or\_port> |

(1) 時序約束，Clocks must be properly defined in order to get the maximum timing path coverage with the best accuracy.

The primary clock *sys\_clk\_pin* has a period of 8 ns. It is divided by 125000000 by the register *clk\_div\_reg* which drives other registers clock pin.

The corresponding generated clock is called *clk\_div*.

#1 create\_clock定義的primary clock waveforms如下圖，

#2 generated clock waveforms 如下圖，

8\*10^(-9)s\*125000000=1s

(2) The Vivado IDE ignores all clock tree delays coming from cells located

upstream from the point at which the primary clock is defined. If you define a

primary clock on a pin in the middle of the design, **only part of its latency is**

**used for timing analysis.**

**This can be a problem if this clock communicates with other**

**related clocks in the design, because the skew, and consequently the slack,**

**value between the clocks can be inaccurate.**