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Research Experience

- **Heterogeneous Architectures / eFPGA**
  - Designing custom primitives for the SPAR-2 Array Processor implemented in FPGA utilizing a processing in-memoory architecture. Standard BRAMs are replaced with PiM blocks to better match the memory requirements of machine-learning algorithms.
- **Embedded Systems / IoT**
  - Prototyped a consumer-facing module for interfacing with a car's OBD-II port to retrieve diagnostic information.
  - Helped develop an RTOS for the OBD-II module using industry-standard tools such as CCS.

Education

- **University of Arkansas** — Fayetteville, AR
  B.S. in Computer Engineering — *Expected May 2023*
  - GPA: 4.0
  - Honor's Thesis: Custom Processing In-Memory BRAMs for the SPAR-2 Array Processor

Employment

- **University of Arkansas** — Fayetteville, AR
  Research/Teaching Assistant — *Summer 2021 - Spring 2022, Fall 2022 - Spring 2023*
  - Designed hardware for an OBD-II interface device and assisted in implementing an RTOS for this device.
- **Phillips 66** — Houston, TX
  IT Intern — *Summer 2022*
  - Identified communication and reporting issues in diagnostic software and architected a holistic dashboarding solution for reporting these issues in third-party software. This solution provides a usable problem notification and identification mechanism to Analysts with non-technical backgrounds.
  - Implemented a stop-gap solution for catching these problems until the long-term solution is able to be implemented by the development teams.

Selected Engineering Projects

- **RTOS Driven Autonomous Vehicle** — Fall 2022

  Developed an autonomous vehicle capable of navigating around a track of reflective tape using two simple light sensors using an FPGA board. The system implemented a MicroBlaze SoC on the FPGA and utilized the FreeRTOS Kernel for scheduling.

- **Exploration of Rowhammering Techniques** — Spring 2022

  Conducted a survey of various techniques for rowhammering and their implementation schemes, then produced a report on how a synthesis of new techniques may be capable of breaking some of the finalists in the NIST PQC Standardization Process by serving as the fault-injection mechanism.

- **Power Usage of AES Power Analysis Attack Mitigation Strategies** — Spring 2022

  Analyzed the power usage characteristics of a michrontoller performing AES encryptions across a variety of AES implementations. These utilizations used many variations and combinations of masking and hiding techniques to improve their resiliency against power analysis attacks.

Selected Professional Activities

Societies:

- **2022 - Present** President of Arkansas UARK AISES Chapter
- **2021 - Present** Member of IEEE
- **2021 - Present** Member Tau Beta Pi

Awards

- **2019 - 2022** University of Arkansas Chancellor's List
- **2021** University of Arkansas Honors College Undergraduate Research Grant
- **2019** University of Arkansas National Merit Scholar