The University of Alabama in Huntsville
Electrical & Computer Engineering
CPE 426/526
Spring 2017
Homework #4

Due April 14, 2017

Take the VHDL model of the tape player provided and instantiate it in a SystemVerilog top module that also contains an interface and a testbench. A skeletal testbench is provided that reads inputs from a text file that is also provided. In the testbench, use an integer random variable to vary the time it takes for M to become '0' after the state is reached where the state machine is waiting for it. Also, use an integer random variable to vary the time it takes for STOP to become '1'. When STOP = '1'or M = '0' are read from the file, delay the application of these values for the correct number of cycles. Constrain the random variables to be less than or equal to 50 and greater than or equal to 20. Use the following weights for distributions.

Time to M = '0',	Values	Weight
Time to STOP = '0'	20:25	10 each
	26:39	20 each
	40:50	15 each

Run 200 different test cases for your testbench.

Turn in your VHDL and SystemVerilog source files.